

74HC1G14-Q100; 74HCT1G14-Q100

Inverting Schmitt trigger

Rev. 3 — 17 January 2022

Product data sheet

1. General description

The 74HC1G14-Q100; 74HCT1G14-Q100 is a single inverter with Schmitt-trigger input. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} . Schmitt trigger inputs transform slowly changing input signals into sharply defined jitter-free output signals.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to $+85\text{ °C}$ and from -40 °C to $+125\text{ °C}$
- Wide supply voltage range from 2.0 V to 6.0 V
- Symmetrical output impedance
- High noise immunity
- CMOS low power dissipation
- Unlimited input rise and fall times
- Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
 - For 74HC1G14-Q100: CMOS level
 - For 74HCT1G14-Q100: TTL level
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)

3. Applications

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC1G14GW-Q100	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74HCT1G14GW-Q100				
74HC1G14GV-Q100	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74HCT1G14GV-Q100				

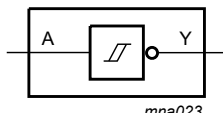
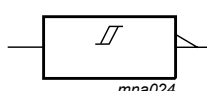
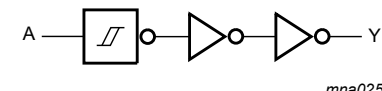
5. Marking

Table 2. Marking codes

Type number	Marking code [1]
74HC1G14GW-Q100	HF
74HCT1G14GW-Q100	TF
74HC1G14GV-Q100	H14
74HCT1G14GV-Q100	T14

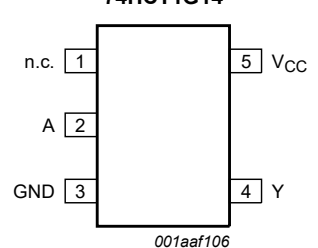
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

 <p><i>mna023</i></p>	 <p><i>mna024</i></p>	 <p><i>mna025</i></p>
Fig. 1. Logic symbol	Fig. 2. IEC logic symbol	Fig. 3. Logic diagram

7. Pinning information

7.1. Pinning

<p>74HC1G14 74HCT1G14</p>  <p><i>001aaf106</i></p>	
Fig. 4. Pin configuration SOT353-1 (TSSOP5) and SOT753 (SC-74A)	

7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
A	Y
L	H
H	L

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V [1]	-	±12.5	mA
I _{CC}	supply current		-	25	mA
I _{GND}	ground current		-25	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC1G14-Q100			74HCT1G14-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

11. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC1G14-Q100								
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}						
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I _O = -2.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
		I _O = -2.6 mA; V _{CC} = 6.0 V	5.63	5.81	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}						
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I _O = 2.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I _O = 2.6 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	1.0	-	1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	10	-	20	μA
C _I	input capacitance		-	1.5	-	-	-	pF
V _{T+}	positive-going threshold voltage	see Fig. 7 and Fig. 8						
		V _{CC} = 2.0 V	0.7	1.09	1.5	0.7	1.5	V
		V _{CC} = 4.5 V	1.7	2.36	3.15	1.7	3.15	V
		V _{CC} = 6.0 V	2.1	3.12	4.2	2.1	4.2	V
V _{T-}	negative-going threshold voltage	see Fig. 7 and Fig. 8						
		V _{CC} = 2.0 V	0.3	0.60	0.9	0.3	0.9	V
		V _{CC} = 4.5 V	0.9	1.53	2.0	0.9	2.0	V
		V _{CC} = 6.0 V	1.2	2.08	2.6	1.2	2.6	V
V _H	hysteresis voltage	see Fig. 7 and Fig. 8						
		V _{CC} = 2.0 V	0.2	0.48	1.0	0.2	1.0	V
		V _{CC} = 4.5 V	0.4	0.83	1.4	0.4	1.4	V
		V _{CC} = 6.0 V	0.6	1.04	1.6	0.6	1.6	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT1G14-Q100								
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}						
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -2.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}						
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 2.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	1.0	-	1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	10	-	20	μA
ΔI _{CC}	additional supply current	per input; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A	-	-	500	-	850	μA
C _I	input capacitance		-	1.5	-	-	-	pF
V _{T+}	positive-going threshold voltage	see Fig. 7 and Fig. 8						
		V _{CC} = 4.5 V	1.2	1.55	1.9	1.2	1.9	V
		V _{CC} = 5.5 V	1.4	1.80	2.1	1.4	2.1	V
V _{T-}	negative-going threshold voltage	see Fig. 7 and Fig. 8						
		V _{CC} = 4.5 V	0.5	0.76	1.2	0.5	1.2	V
		V _{CC} = 5.5 V	0.6	0.90	1.4	0.6	1.4	V
V _H	hysteresis voltage	see Fig. 7 and Fig. 8						
		V _{CC} = 4.5 V	0.4	0.80	-	0.4	-	V
		V _{CC} = 5.5 V	0.4	0.90	-	0.4	-	V

12. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f \leq 6.0\text{ ns}$; All typical values are measured at $T_{amb} = 25\text{ }^\circ\text{C}$. For test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC1G14-Q100								
t_{pd}	propagation delay	A to Y; see Fig. 5 [1]						
		$V_{CC} = 2.0\text{ V}$; $C_L = 50\text{ pF}$	-	25	155	-	190	ns
		$V_{CC} = 4.5\text{ V}$; $C_L = 50\text{ pF}$	-	12	31	-	38	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	10	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$; $C_L = 50\text{ pF}$	-	11	26	-	32	ns
C_{PD}	power dissipation capacitance	$V_I = GND\text{ to }V_{CC}$ [2]	-	20	-	-	-	pF
74HCT1G14-Q100								
t_{pd}	propagation delay	A to Y; see Fig. 5 [1]						
		$V_{CC} = 4.5\text{ V}$; $C_L = 50\text{ pF}$	-	17	43	-	51	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	15	-	-	-	ns
C_{PD}	power dissipation capacitance	$V_I = GND\text{ to }V_{CC} - 1.5\text{ V}$ [2]	-	22	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF; V_{CC} = supply voltage in Volts

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

12.1. Waveforms and test circuit

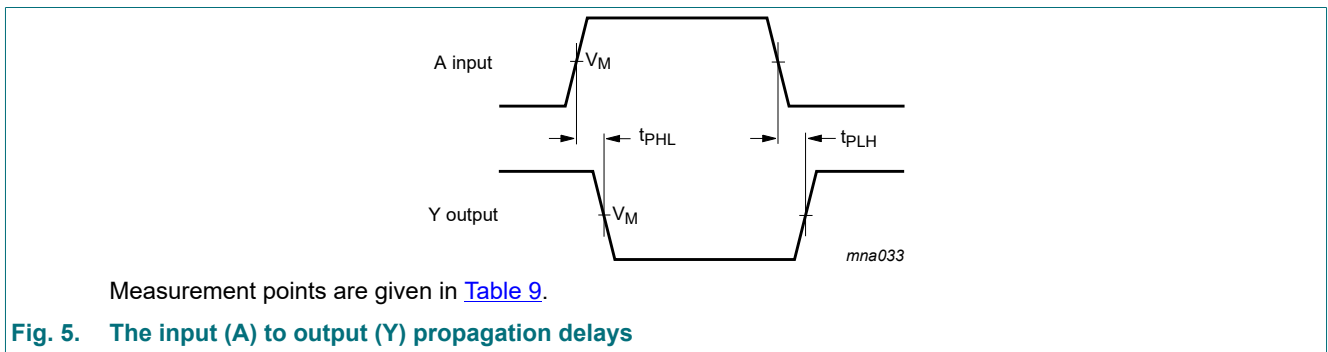
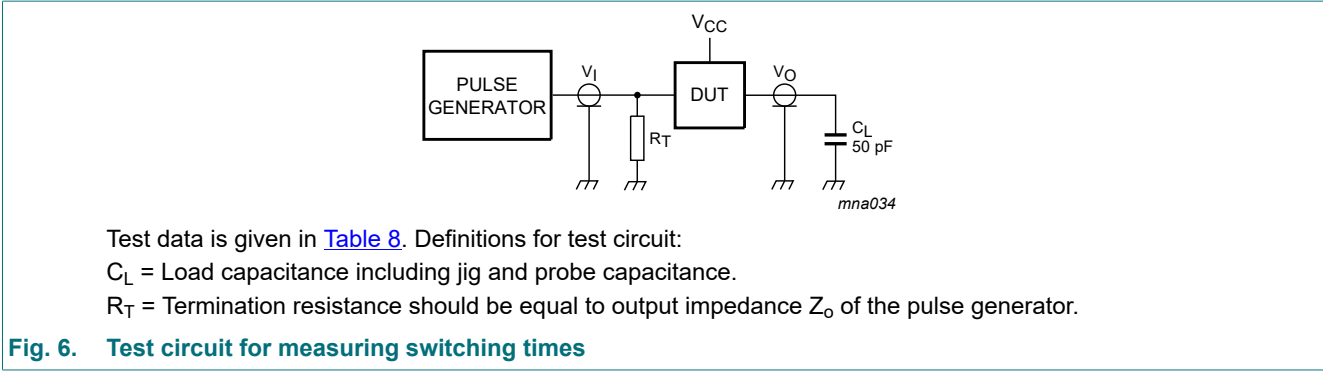
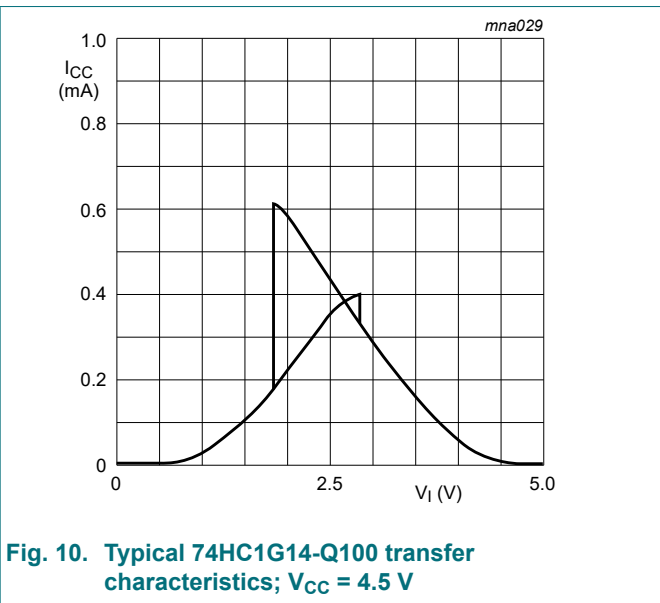
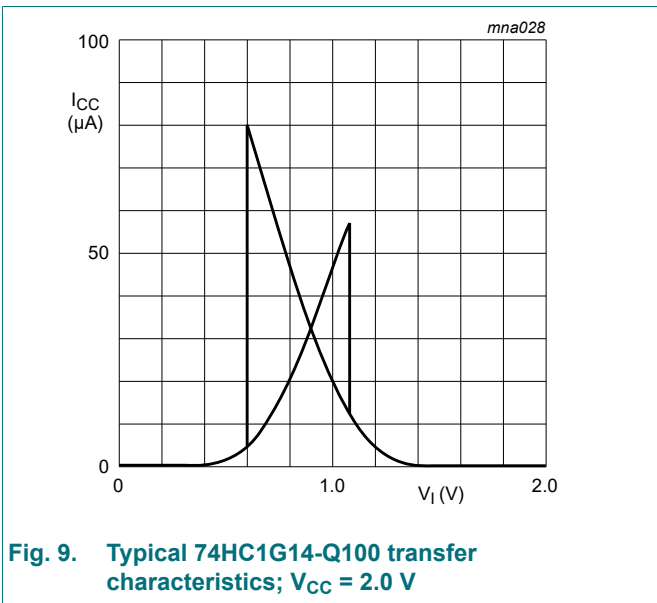
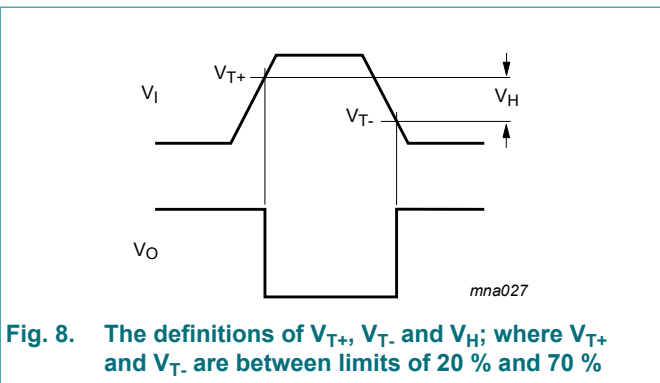
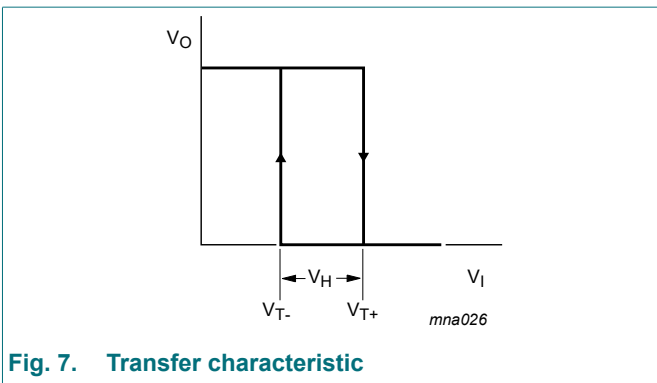


Table 9. Measurement points

Type number	Input		Output
	V_I	V_M	V_M
74HC1G14-Q100	GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT1G14-Q100	GND to 3.0 V	1.5 V	$0.5 \times V_{CC}$



12.2. Transfer characteristics waveforms



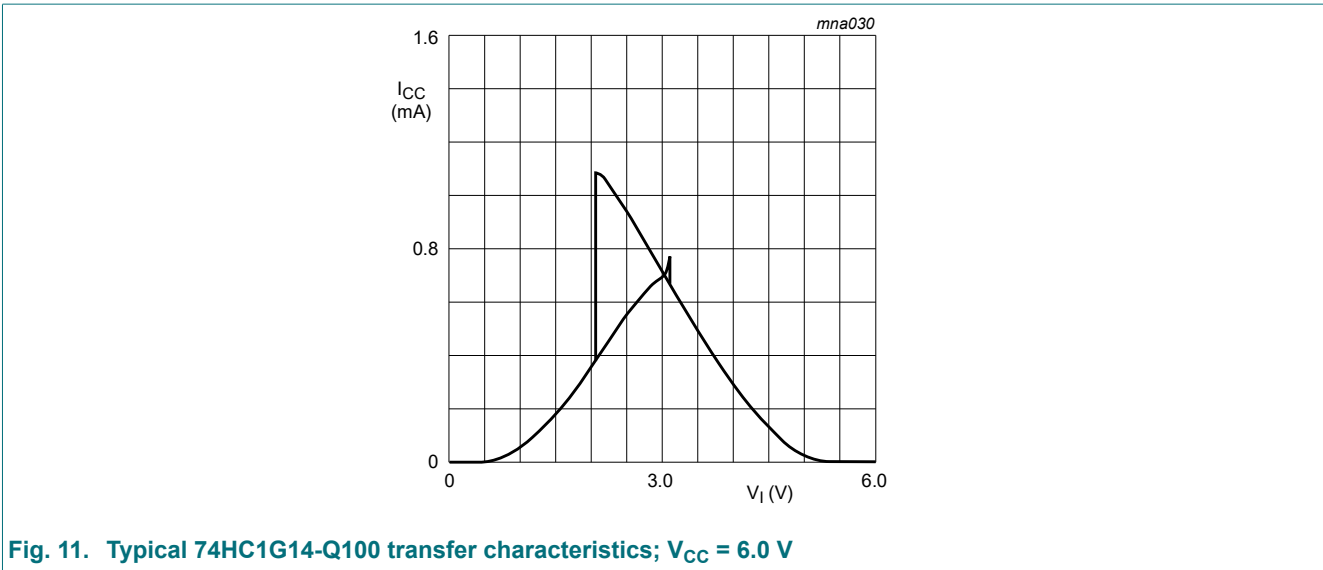


Fig. 11. Typical 74HC1G14-Q100 transfer characteristics; $V_{CC} = 6.0\text{ V}$

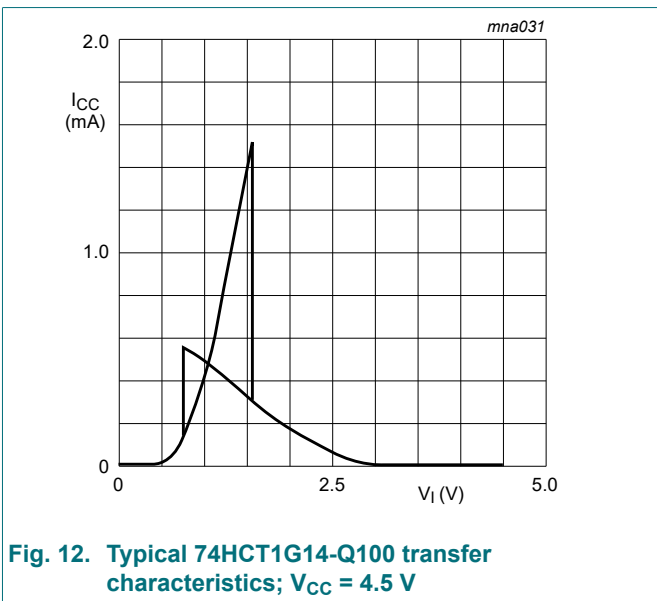


Fig. 12. Typical 74HCT1G14-Q100 transfer characteristics; $V_{CC} = 4.5\text{ V}$

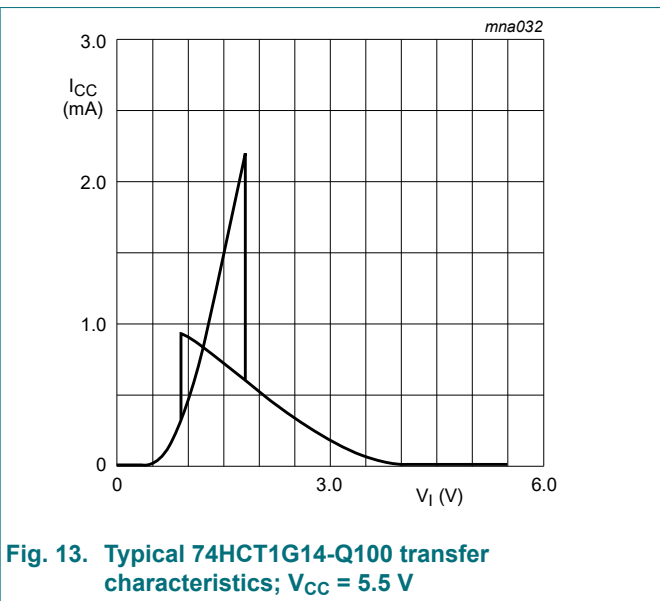


Fig. 13. Typical 74HCT1G14-Q100 transfer characteristics; $V_{CC} = 5.5\text{ V}$

13. Application information

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$$P_{\text{add}} = f_i \times (t_r \times \Delta I_{\text{CC(AV)}} + t_f \times \Delta I_{\text{CC(AV)}}) \times V_{\text{CC}}$$

Where:

P_{add} = additional power dissipation (μW)

f_i = input frequency (MHz)

t_r = rise time (ns); 10 % to 90 %

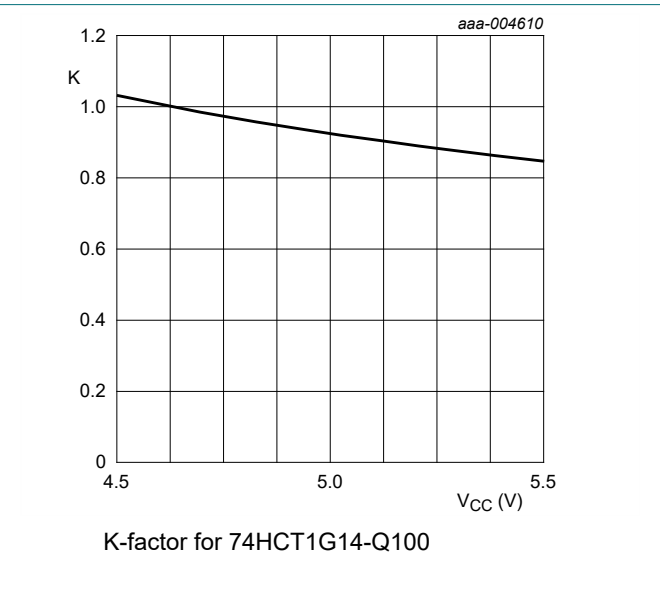
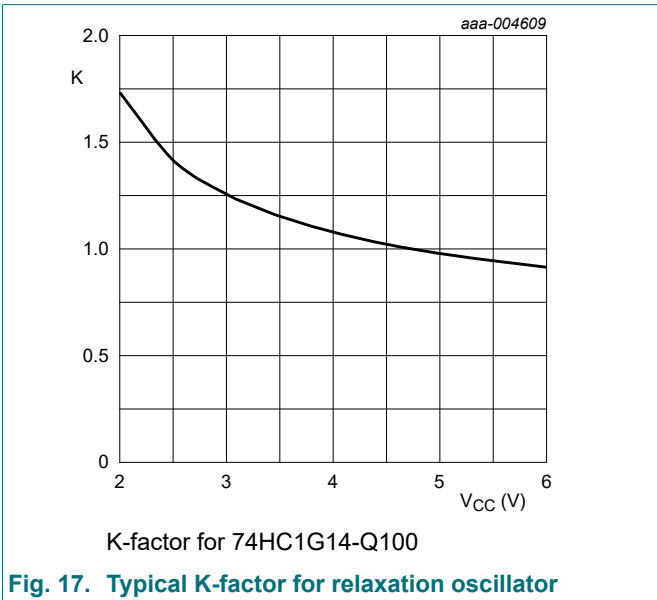
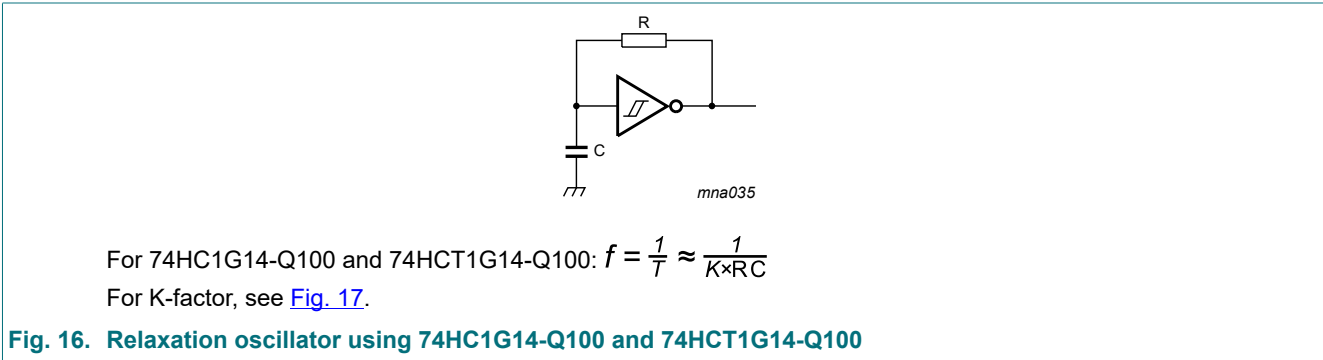
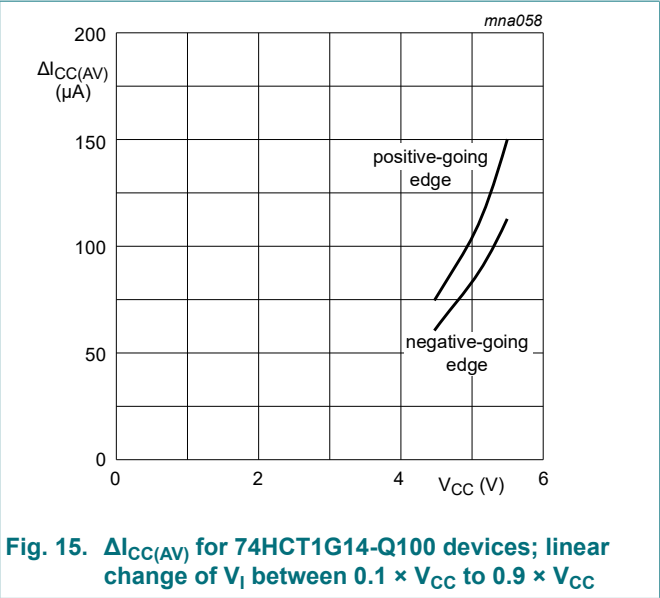
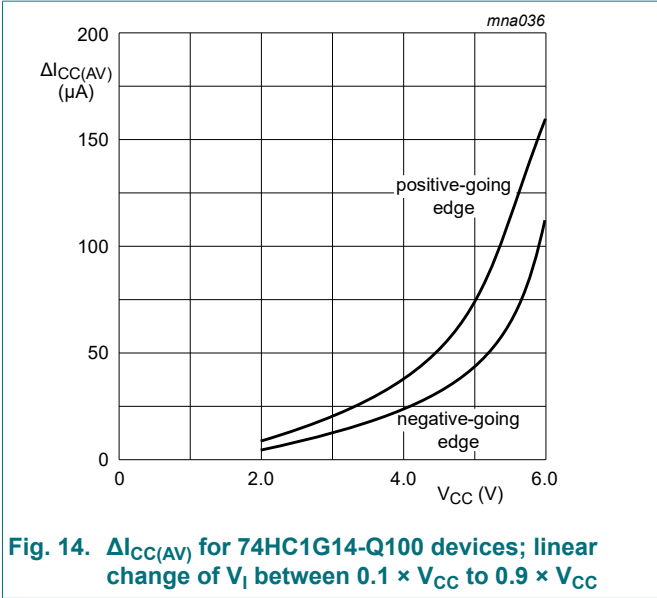
t_f = fall time (ns); 90 % to 10 %

$\Delta I_{\text{CC(AV)}}$ = average additional supply current (μA)

$\Delta I_{\text{CC(AV)}}$ differs with positive or negative input transitions, as shown in [Fig. 14](#) and [Fig. 15](#).

74HC1G14-Q100 and 74HCT1G14-Q100 used in relaxation oscillator circuit, see [Fig. 16](#).

Remark: All values given are typical unless otherwise specified.



14. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

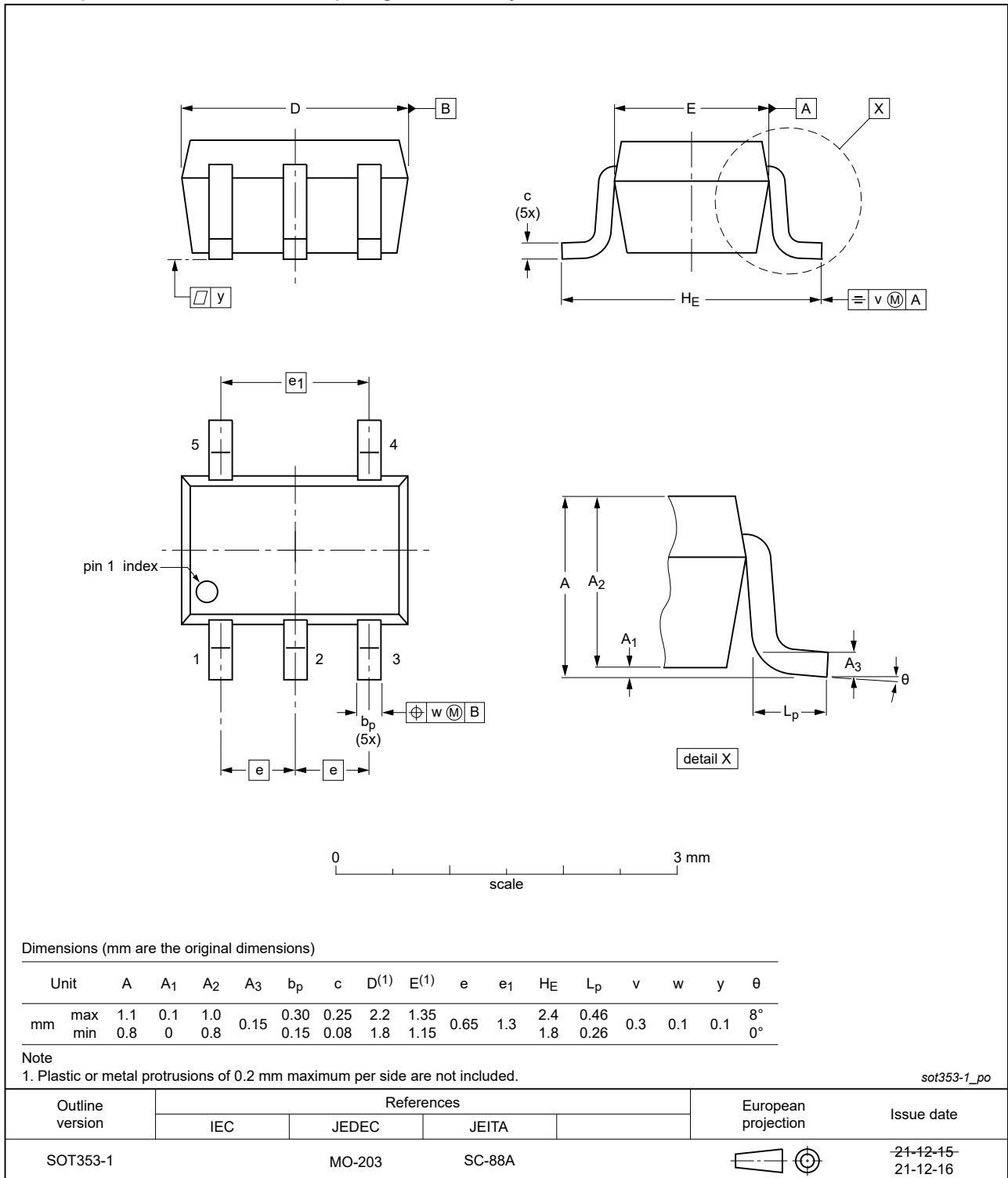


Fig. 18. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

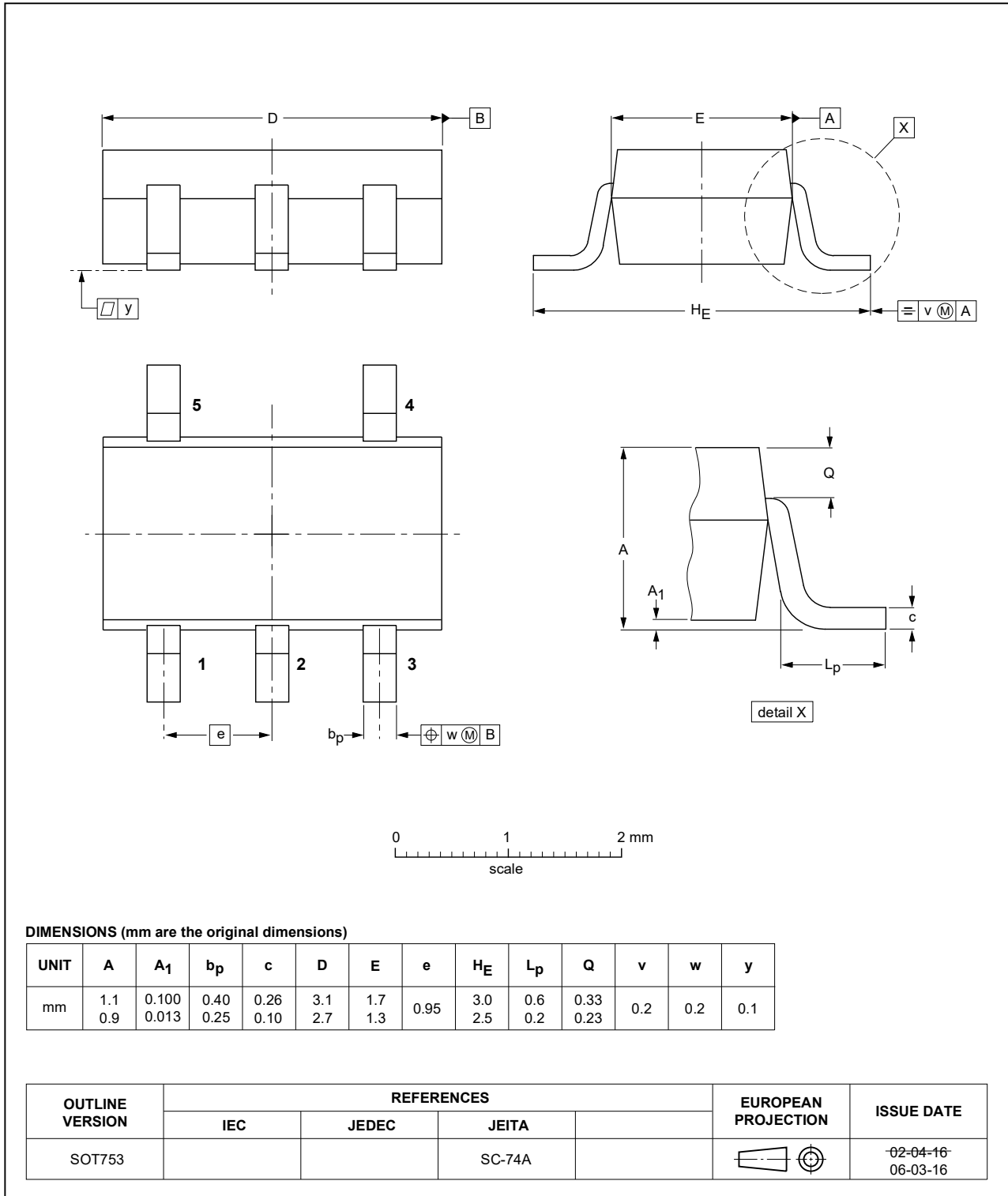


Fig. 19. Package outline SOT753 (SC-74A)

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT1G14_Q100 v.3	20220117	Product data sheet	-	74HC_HCT1G14_Q100 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 5: Derating values for P_{tot} total power dissipation updated. Fig. 18: Package outline drawing for SOT353-1 (TSSOP5) has changed 			
74HC_HCT1G14_Q100 v.2	20121227	Product data sheet	-	74HC_HCT1G14_Q100 v.1
Modifications:	<ul style="list-style-type: none"> Table 3: Pin number Y output changed from 5 to 4 (errata). 			
74HC_HCT1G14_Q100 v.1	20120820	Product data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 17 January 2022
