

## Design Note

### Precision Ultralow Power High Side Current Sense Catherine Chang

### Introduction

Precision high side measurement of microamp currents requires a small value sense resistor and a low offset voltage amplifier. The LTC®2063 zero-drift amplifier has a maximum input offset voltage of just  $5\mu V$  and draws just  $1.4\mu A$  making it a great choice for building a complete ultralow-power precision high side current sense circuit, as shown in Figure 1.

This circuit uses only  $2.3\mu A$  to  $280\mu A$  of supply current to sense currents over a wide  $100\mu A$  to 250mA dynamic range. The exceptionally low offset of the LTC2063 allows this circuit to work with only  $100m\Omega$  of shunt resistance, limiting the maximum shunt voltage to only 25mV. This minimizes power loss on the shunt resistor and maximizes power available to the load. The LTC2063's rail-to-rail input allows this circuit to operate with very small load current where input common mode is almost at the rail. The integrated EMI filter of the LTC2063 protects it from RF interference in noisy conditions.

The voltage output of this circuit for a given sense current is:

$$V_{OUT} = \frac{R_{DRIVE} \bullet R_{SENSE}}{R_{IN}} I_{SENSE} = 10 \bullet I_{SENSE}$$

### **Zero Point**

A critical specification for a current sense solution is the zero point, or equivalent error current at the input for the output produced when no sense current is present. The zero point is generally determined by the input offset voltage of the amplifier divided by  $R_{SENSE}$ . The LTC2063's low input offset voltage, of typical 1µV, maximum 5µV, and low typical input bias and offset currents of 1-3pA, allow for a zero point input-referred error current of only 10µA (1µV/0.1 $\Omega$ ) typically, or 50µA (5µV/0.1 $\Omega$ ) maximum. This low error allows the sense circuit to maintain its linearity down to the lowest current in its specified range (100µA), without plateauing due to loss of resolution, as seen in Figure 2. The resulting input current to output voltage plot is linear over the entire current sense range.

Another source of zero point error is the output PMOS's zero gate voltage drain current, or  $I_{DSS}$ , a parasitic current that is present for nonzero  $V_{DS}$  when the PMOS is nominally turned off ( $IV_{GS}I = 0$ ). A MOSFET with high  $I_{DSS}I$  leakage will produce a non-zero positive  $V_{OLIT}$  with no  $I_{SENSE}$ .

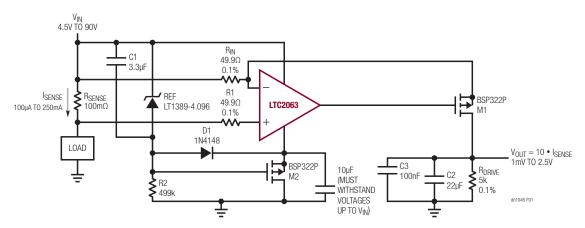


Figure 1. Precision High Side Current Sense Circuit Based on the LTC2063 Zero-Drift Amplifier

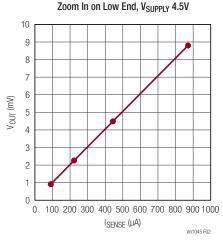


Figure 2. No Plateau at the Low End, Down to 100μΑ I<sub>SENSE</sub>

The transistor used in this design, Infineon's BSP322P, has an upper-bound  $I_{DSS}$  of  $1\mu A$  at  $|V_{DS}|=100V$ . As a good estimate for the typical  $I_{DSS}$  of the BSP322P in this application, at room temperature, with  $V_{DS}=-7.6V$ ,  $I_{DSS}$  is only 0.2nA, resulting in just  $1\mu V$  error output, or equivalent 100nA input current error, when measuring 0A input current.

### **Architecture**

The LT1389-4.096 reference, along with the bootstrap circuit composed of M2, R2, and D1, establishes a very low power isolated 3V rail (4.096V + V<sub>TH</sub> of M2, typically –1V) that protects the LTC2063 from seeing its absolute maximum supply voltage of 5.5V. Although a series resistance could suffice for establishing bias current, using transistor M2 allows for much higher overall supply voltages while also limiting current consumption to a mere  $280\mu\text{A}$  at the high end of the supply range.

### **Precision**

The LTC2063's input offset voltage contributes a fixed input-referred current error of  $10\mu A$  typical. Out of 250mA full-scale input, the offset results in only 0.004% error. At the low end,  $10\mu A$  out of  $100\mu A$  is 10% error. Since the offset is constant, it can be calibrated out. Figure 3 shows that total offset from LTC2063, unmatched parasitic thermocouples, and any parasitic series input resistances is only  $2\mu V$ .

The gain shown in Figure 3, 100.05V/V is 1.28V/V greater than the expected gain given by the actual values of  $R_{DRIVE}$  and  $R_{IN}$  when built, or 4.978k/50.4 = 98.77V/V. This error may be due to the different temperature coefficients of  $R_{DRIVE}$  and  $R_{IN}$ .



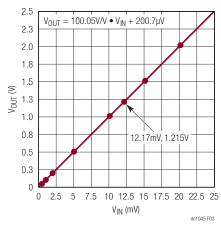


Figure 3.  $V_{IN}$  to  $V_{OUT}$  Conversion on Minimum Supply 4.5V for Entire I<sub>SENSE</sub> Range. Output Offset of 200.7 $\mu$ V, when Divided by 100.05V/V Voltage Gain, Implies RTI Input Offset of  $2\mu$ V

The main source of uncertainty in the output of this circuit is noise, so filtering with large parallel capacitors is crucial to reduce noise bandwidth and thus the total integrated noise. With a 1.5Hz output filter, the LTC2063 adds about  $2\mu V_{P-P}$  low frequency, input-referred noise. Averaging the output over the longest possible duration further reduces error due to noise.

Other sources of error in this current sense circuit are parasitic board resistance in series with the  $R_{SENSE}$  at the LTC2063 input, tolerance in resistance values of the gain-setting resistors  $R_{\text{IN}}$  and  $R_{DRIVE}$ , mismatched temperature coefficients in the gain-setting resistors, and error voltage at the op amp inputs due to parasitic thermocouples. The first three sources of error can be minimized by using Kelvin sense 4-lead sense resistors for  $R_{SENSE}$ , and using 0.1% resistance with similar or low temperature coefficients for the critical gain-set path of  $R_{\text{IN}}$  and  $R_{DRIVE}$ . To cancel out the parasitic thermocouples at the op amp inputs, R1 should have the same metal terminals as  $R_{\text{IN}}$ . Asymmetric thermal gradients should also be avoided as much as possible at the inputs.

The overall contribution of all the error sources discussed in this section is at most 1.4% when referenced against full-scale 2.5V output, as shown in Figure 4.

### **Supply Current**

The minimum supply current required by the LT1389 and LTC2063 is  $2.3\mu A$  at the minimum  $V_{SUPPLY}$  and  $I_{SENSE}$  (4.5V and  $100\mu A$ ), up to  $280\mu A$  at maximum  $V_{SUPPLY}$  and

# Percent Error In Output V<sub>SUPPLY</sub> 4.5V 2.0 1.8 MAX ERROR 1.3794% — MAX ERROR 1.3794%

Figure 4. Percent Error Remains Below 1.4% for Entire Range of Readings

I<sub>SENSE</sub> (90V and 250mA), as shown in Figure 5. In addition to the current consumed by the active components, an output current I<sub>DRIVE</sub> through M1 also supplied by V<sub>SUPPLY</sub> is required, proportional to the output voltage, ranging from 200nA for a 1.0mV output (for 100μA I<sub>SENSE</sub>) to 500μA for a 2.5V output (for 250mA I<sub>SENSE</sub>). Thus, the total supply current in addition to I<sub>SENSE</sub> ranges from 2.5μA to 780μA. R<sub>DRIVE</sub> is set at  $5k\Omega$  for a reasonable ADC drive value.

#### Quiescent ISUPPLY of Measurement Circuit, No I<sub>SENSE</sub> and I<sub>DRIVE</sub> 300 MAX: 279.1uA 270 240 210 180 SUPPLY (µA) 150 120 90 60 30 70 10 20 30 40 50 60 80 90 100 V<sub>SUPPLY</sub> (V)

Figure 5. Supply Current Increases with Supply Voltage but Never Surpasses 280µA

### **Input Voltage Range**

In this architecture, the maximum supply is set by the maximum  $|V_{DS}|$  that the PMOS output can withstand. The BSP322P is rated for 100V, so 90V is an appropriate operating limit.

### **Output Range**

This design can drive a  $5k\Omega$  load, which makes it a suitable stage for driving many ADCs. The output voltage range is 0V to 2.5V. Since the LTC2063 has rail-to-rail output, the maximum gate drive is only limited by the LTC2063's headroom. It is 3V typically in this design, set by the LT1389's 4.096V plus the -1V typical  $V_{TH}$  of M2.

Since the output of this circuit is a current, not a voltage, ground or lead offset does not affect accuracy. Thus, long leads can be used between the output PMOS M1 and  $R_{DRIVE}$ , allowing  $R_{SENSE}$  to be located near the current being sensed while  $R_{DRIVE}$  is near an ADC and other subsequent signal chain stages. The drawback of long leads is increased EMI susceptibility.  $100\text{nF}\,\text{C3}$  across  $R_{DRIVE}$  shunts away harmful EMI before it reaches the next stage's input.

### **Speed Limits**

Since the LTC2063's gain-bandwidth product is 20 kHz, it is recommended to use this circuit to measure signals 20 Hz or slower. The  $22 \mu \text{F}$  C2 in parallel with the load filters the output noise to 1.5Hz for improved accuracy and protects the subsequent stage from sudden current surges. The trade-off of this filtering is longer settling time, especially at the lowest end of the input current range.

### **Conclusion**

The LTC2063's ultralow input offset voltage, low  $I_{OFFSET}$  and  $I_{BIAS}$ , and rail-to-rail input, provide precise current measurements over the entire range of  $100\mu A$  to 250mA. Its  $2\mu A$  maximum supply current enables the circuit to run on far less than  $280\mu A$  supply current for most of its operating range. Along with LTC2063's low supply voltage requirements, the low supply current allows it to be powered from a voltage reference with headroom to spare.

**Data Sheet Download** www.linear.com/LTC2063

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