Universe IID/IIB™ Device Errata and Design Notes

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About this Document

This document describes device errata and design notes for the Universe IID/IIB.

Revision History

8091142_ER001_11, October 2009

This version of the document was rebranded as IDT. It does not include any technical changes.

8091142_ER001_10, June 2009

The following errata have been added to this document:

- "[VME9] VME IACKOUT* De-assertion Issue"
- "[VME10] Driving VME Data Bus Signals When Responding to an 8-bit IACK Cycle"

Device Errata

Device Errata[a]	Applicability	
	Universe IIB	Universe IID
"[VME1] Incorrect Propagation of IACKIN#/IACKOUT# in BIMODE"	Yes	Yes
"[VME2] Incorrect Negation of VOE During MBLT Slave Writes In a Heavily Loaded System"	Yes	Yes
"[VME3] Improper PCI Cycle Termination"	Yes	No
"[VME4] ESD Sensitivity"	Yes	No
"[VME5] DY4 AUTO-ID Incompatibility"	Yes	Yes
"[VME6] Incorrect Operation of Vown/Vack"	Yes	Yes
"[VME7] Incorrect De-assertion of LOCK# During Exclusive Accesses"	Yes	Yes
"[VME8] PCI REQ# Line Driven Incorrectly During Reset"	Yes	Yes
"[VME9] VME IACKOUT* De-assertion Issue"	Yes	Yes
"[VME10] Driving VME Data Bus Signals When Responding to an 8-bit IACK Cycle"	Yes	Yes

a. Errata numbers in brackets denote interface-specific or general device errata.

[VME1] Incorrect Propagation of IACKIN#/IACKOUT# in BIMODE

Description

When an interrupt is generated in a multiple board VME system, the interrupt handler initiates an IACK cycle to service this interrupt and generate IACKOUT# onto the daisy chain.

Impact

If the Universe IID/IIB is configured to be in BIMODE, it will not propagate the IACKOUT# signal through the daisy chain when it receives IACKIN*. As a result, the interrupter will not receive IACKIN# and DTACK# will not be generated. The IACK cycle will not terminate properly and a bus error (BERR#) will occur due to a VMEbus system time out.

Work Around

When generating interrupts in a multiple VME board based system, the Universe IID/IIB should not be configured in BIMODE.

Status

This issue is applicable to all Universe IID/IIB part numbers.

[VME2] Incorrect Negation of VOE During MBLT Slave Writes In a Heavily Loaded System

Description

When in external master initiates a VME MBLT coupled write cycle through the VME slave channel in a heavily loaded system, the Universe IID/IIB negates its VOE# signal prematurely (disabling all the buffers) if the VME Master negates the write signal without enough hold time on the last data phase.

After the premature negation of VOE#, any subsequent VME cycles to the Universe IID/IIB will have a VME bus error, because the Universe IID/IIB will not respond to any cycle. The VOE# signal is negated when a cycle is generated to the Universe IID/IIB with both data strobes (DS0#, DS1#) asserted.

Impact

The Universe IID/IIB requires a 5ns hold time from DS1# negation to WRITE# negation in violation of the *VME64 Specification* (Rule 2.49). The specification states, a VME master is supposed to provide 10ns hold time from the negation of DS1# to the negation of the write signal, whereas the VME slave should expect 0ns hold for the negation of the write signal to the negation of DS1#.

Work Around

Enabling the Universe IID/IIBs internal DSx# filter aggravate delays the internal DSx# signals further from the external DSx# signals.

Status

This issue is applicable to all Universe IID/IIB part numbers.

[VME3] Improper PCI Cycle Termination

Description

In 64-bit PCI bus applications the Universe IIB may exhibit incorrectly terminated cycles on the PCI bus when the Universe IIB is acting as a PCI initiator (master). The incorrect PCI bus termination is logged as a Master Abort in the PCI_CSR of the Universe IIB This errata is isolated to 64 bit PCI bus applications.

Impact

The issue is aggravated by elevated ambient temperature (above 40C), reduced 5V supply voltage (approximately 4.75 V), PCI clock speed of 33MHz, increased PCI bus loading and specific data patterns. The worst case pattern has been identified as alternating F's and 0's

This errata can be captured on an analyzer as follows:

- Trigger the scope from the output trigger of the analyzer
- Set the trigger for the analyzer to be the following:
- LEVEL 1: Find Frame Low 1 Time Else on Not Frame go to Level 1
- LEVEL 2: Find rising edge of TRDY
- LEVEL 3: Find (Frame =1, IRDY=0 DEVSEL=1 TRDY=1 STOP=1) nine times else go to Level 1.

You may need to change the number of times to find the pattern in Level 3.

Work Around

Please contact IDT if you observe this errata.

Status

This issue is applicable to all Universe IIB part numbers. This issue is corrected in Universe IID part numbers.

[VME4] ESD Sensitivity

Description

The Universe IIB does not meet 2000V ESD tolerance as per MIL STD 883 Method 3015 Human Body Model test. The most sensitive ESD tolerance is 500V HBM seen on the AVDD and AVSS pins.

Impact

The following precautions are recommended when handling the Universe IIB devices to reduce ESD exposure:

- Wear wrist straps while seated.
- Wear footwear or heel straps while standing.
- Wear ESD smocks.
- Regularly check wrist straps and footwear.
- Ensure ESD dissipative flooring and work surfaces.
- Ensure work surfaces and equipment connected to electrical ground.
- Use ESD compliant chairs and carts, or “drag-chain” to the floor.
- Ensure humidity in all inspection and assembly areas maintained between 30% and 70%.
- Minimize inspection and handling.
- If inspection is required, keep parts within trays (if possible).
- No conductive or electrostatic generating materials in close proximity to unprotected product, e.g. shop travelers, labels, cardboard, Plexiglas, wood, CRT screens, etc.
- Ionization systems should be in place to help dissipate residual charge built up on any material that is static generating and in close proximity to Universe IIB devices.
- A field strength meter can be used to check items that come into contact with the Universe IIB; this tool may be very useful in confirming safe surfaces and those that contain residual charges that may need neutralizing ionizers.

Work Around

Use the Universe IID for ESD sensitive designs.

Status

This issue is applicable to all Universe IIB part numbers. This issue is corrected in Universe IID part numbers. Universe IID ESD sensitivity meets, or exceeds, 2000 V HBM

[VME5] DY4 AUTO-ID Incompatibility

Description

When the Universe IID/IIB is the system controller (syscon), IACKOUT is asserted on the 5th SYSCLK clock edge instead of the 7th SYSCLK clock edge. This early assertion causes subsequent cards to come up at one slot address too low.

Impact

The incorrect count may cause problems in software, if not taken into account when DY4 Auto-ID is used.

Work Around

None.

Status

This issue is applicable to all Universe IID/IIB part numbers.

[VME6] Incorrect Operation of Vown/Vack

Description

When setting the VOWN bit and changing the request level by modifying the VRL bits in the MAST_CTL register simultaneously, there is approximately a 40ns delay of the assertion of the new VRL value. The VMEbus arbiter will see the Universe request on the 'old' request level, and if the bus is not busy, the arbiter will immediately issue a bus grant which will be acknowledged by the Universe on the 'old' request level. If the bus is busy, or the grant comes back after the delay in the assertion of the VRL bits, the UNIVERSE will have switched to the 'new' request level.

Impact

Adhering to the VMEbus specification, the Universe will not acknowledge bus grants on any other level than the one it is on; the Universe will propagate the bus grant coming in on the 'old' bus request level down the bus grant daisy-chain. Also, the UNIVERSE will not release the BR [old]* line because it has not received a grant from the arbiter on its current request level yet. The Universe will continue to request the bus on the 'old' level indefinitely, and the arbiter will continue to issue grants on the 'old' request level, which will either time out, or be acknowledged by a Master further down the daisy-chain.

Work Around

To avoid this situation, set the VRL bits in MAST_CTL register in the first of two writes. This will allow time for the Universe to change bus request levels before requesting the VMEbus. On the second write to MAST_CTL, set the VOWN bit.

Status

This issue is applicable to all Universe IID/IIB part numbers.

[VME7] Incorrect De-assertion of LOCK# During Exclusive Accesses

Description

The Universe IID/IIB may de-assert PCI LOCK# incorrectly during exclusive accesses initiated from the VMEbus.

This errata occurs when a read modify write cycle is initiated by a VMEbus master to the Universe IID/IIB, and PCI agent simultaneously accesses the Universe IID/IIB as a PCI target to perform a read/write cycle to the VMEbus. The Universe IID/IIB acquires the PCI bus to complete the RMW cycle before the PCI agent is granted the PCI bus.

When these conditions occur, and the Universe IID/IIB is retried on the PCI bus by the PCI target long enough to cause a VMEbus time-out during the read modify write cycle, then any subsequent attempts to complete the VMEbus RMW read while the PCI agent attempts to complete the PCI read/write cycle will cause the Universe IID/IIB to assert LOCK# and de-assert it within 1 PCI clock cycle.

Impact

This is behavior is in violation with the *PCI 2.1 Specification* which states that LOCK# must be asserted the clock following the address phase and kept asserted to maintain control. LOCK# must be released only if the initial transaction of the LOCK# is terminated with Retry, Target-Abort, or Master-Abort.

Work Around

There are two possible solutions to avoid the above situation. The first is to ensure that the PCI target does not retry the VME Read Modify Write long enough to cause a VMEbus time-out error.

The second is to program the Universe IID/IIB 's PCI master interface to generate a Master Abort prior to a bus error time-out occurring on the VMEbus. This is done by programming the MAXRTRY field in the MAST_CTL register (offset 0x400).

Status

This issue is applicable to all Universe IID/IIB part numbers.

[VME8] PCI REQ# Line Driven Incorrectly During Reset

Description

During a PCI Reset (RST# asserted) or power on reset (PWRRST#), the Universe will incorrectly drive the REQ# signal high.

Impact

This is behavior is in violation of the *PCI 2.1 Specification* which states this signal must be tristated during reset.

Work Around

None.

Status

This issue is applicable to all Universe IID/IIB part numbers.

[VME9] VME IACKOUT* De-assertion Issue

Description

When the Universe II is configured as the system controller, it incorrectly negates the VME IACKOUT (VIACKO) signal off the de-assertion of the VME data strobe signals. Rule 4.47 of the *VME Specification* states that IACKOUT must be driven high after the rising edge of the VME address strobe signal.

Impact

No system level issues have been encountered.

Work Around

None.

Status

This issue is applicable to all Universe IID/IIB part numbers.

[VME10] Driving VME Data Bus Signals When Responding to an 8-bit IACK Cycle

Description

The Universe II drives the VME Data bus lines [31:08] low during an 8-bit IACK cycle. Rule 4.14 of the *VME Specification* indicates that the interrupter must not drive these unused VME data signals low during a D08(O) IACK cycle.

Impact

None. No system level issues have been encountered.

Work-around

None

Status

This issue is applicable to all Universe IID/IIB part numbers.

Design Notes

[DES1] Maximum Junction Temperature

IDT recommends that the maximum junction temperature of the Universe IID/IIB devices not exceed 150 C by using adequate heat dissipation techniques such as heat sinks and forced airflows. Long term reliability with operation at a junction temperatures above 150 C has not been characterized.

[DES2] Power Sequencing Guidelines

When designing with the Universe IID/IIB devices, care should be taken when powering the device to ensure proper operation. Designers should make sure that no signals are applied to any Universe IID/IIB signal pins prior to stable power being applied to the device.

In a mixed 3.3V and 5V design, it is recommended that 5V power be stable prior to other devices coming out reset. Should other devices come out of reset before the 5V power is stable, designers should make certain that no signals are driven to the Universe IID/IIB signal pins, including possible signals from the VME backplane.

[DES3] Behavior During BERR# Terminations

When a VME master read or write access (single, BLT, or MBLT) to the Universe IID/IIB is terminated with BERR# prior to the MAXRTRY counter expiring, and prior to the PCI access receiving TRDY#, the Universe IID/IIB's PCI master interface continues to issue the cycle (FRAME# asserted) until the counter expires. When the counter expires in this situation any subsequent accesses through the Universe IID/IIB VMEbus slave channel are no longer possible until the device is reset. However, register and VMEbus accesses are still operational.

IDT recommends that no VMEbus BERR# time-outs or BERR# terminations occur before the MAXRTRY counter in the Universe IID/IIB expires. Disabling the VMEbus time-out counter within the system effectively prevents this behavior.