

## GPIO ICs Series

# GPIO Expander IC


**BU1850MUV**

No.09098EAT02

**●Description**

GPIO expander is useful especially for the application that is in short of IO ports.

It can

1. Control GPIO output states by I<sup>2</sup>C write protocol.
2. Know GPIO input states by I<sup>2</sup>C read protocol.

Furthermore, it has the interrupt function that can release CPU from polling the registers in the GPIO expander. GPIO expander are also equipped with Built-in power on reset, 3V tolerant input, and NMOS open-drain output.

**●Features**

- 1) An 8-Port General purpose input/output interface 150kΩ Pull-down resistance.
- 2) NMOS Open-drain output interrupt controller with up to 1us pulse noise filter and bit mask function for individual GPIO port.
- 3) 3volt tolerant Input
- 4) Built-in Power On Reset
- 5) 3mmx3mm small package

**●Absolute maximum ratings**

(Ta=25 °C)

| Parameter                    | Symbol | Rating                        | Unit | comment                   |
|------------------------------|--------|-------------------------------|------|---------------------------|
| Supply Voltage <sup>*1</sup> | VDD    | -0.3 ~ +4.5                   | V    | VDD ≤ VDDIO               |
|                              | VDDIO  | -0.3 ~ +4.5                   | V    |                           |
| Input voltage                | VI     | -0.3 ~ VDD +0.3 <sup>*1</sup> | V    | XRST, ADR                 |
|                              | VIT    | -0.3 ~ 4.5                    | V    | XINT, SCL, SDA, GPIO[7:0] |
| Storage temperature range    | Tstg   | -55 ~ +125                    | °C   |                           |
| Package power                | PD     | 272 <sup>*2</sup>             | mW   |                           |

This IC is not designed to be X-ray proof.

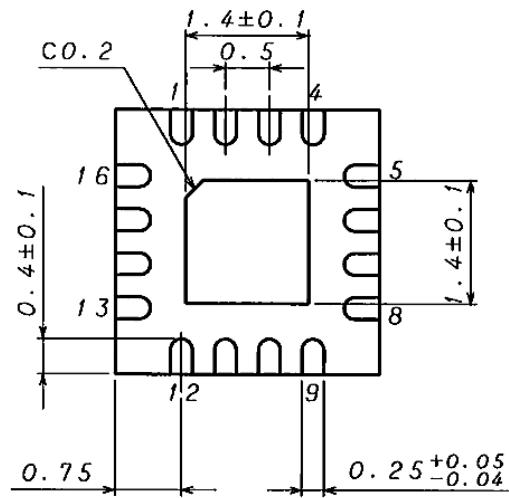
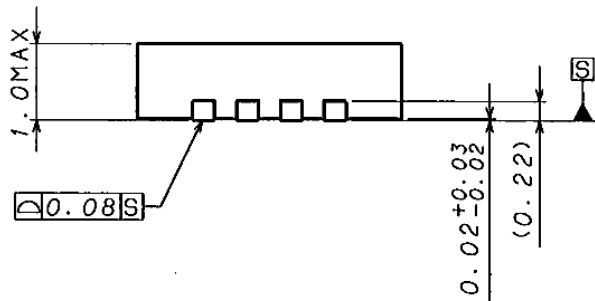
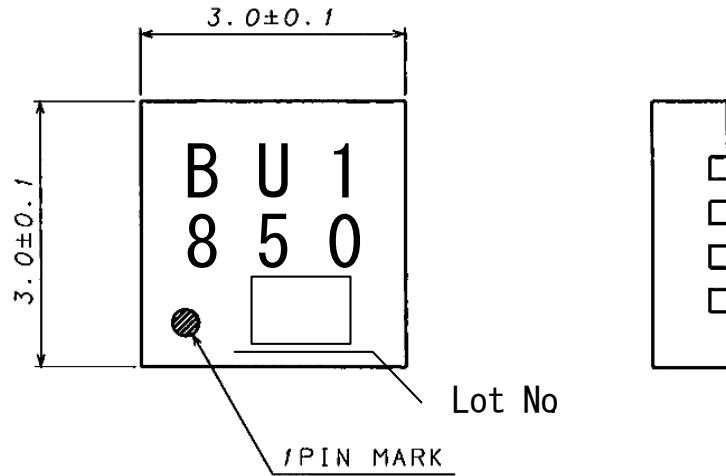
\*1 It is prohibited to exceed the absolute maximum ratings even including +0.3 V.

\*2 Package dissipation will be reduced each 2.72mW/°C when the ambient temperature increases beyond 25 °C.

**●Operating conditions**

| Parameter                            | Symbol             | Min  | Typ  | Max                   | Unit | Conditions                                      |
|--------------------------------------|--------------------|------|------|-----------------------|------|---|
| Supply voltage range (VDD)           | V <sub>VDD</sub>   | 1.65 | 1.80 | 3.6                   | V    | Core, XINT, XRST, SCL, SDA, ADR, Power On Reset |
| Supply voltage range (VDDIO)         | V <sub>VDDIO</sub> | 1.65 | 1.80 | 3.6                   | V    | GPIO[7:0]                                       |
| Input voltage range                  | V <sub>IN</sub>    | -0.2 | -    | V <sub>VDD</sub> +0.2 | V    | XRST, ADR                                       |
|                                      | V <sub>INT</sub>   | -0.2 | -    | 3.6                   | V    | XINT, SCL, SDA, GPIO[7:0]                       |
| Operating temperature range          | Topr               | -30  | -    | +85                   | °C   |   |
| I <sup>2</sup> C operating frequency | F <sub>I2C</sub>   | -    | -    | 400                   | kHz  | Slave   |

● Package Specification



(UNIT: mm)

Fig.1 Package Specification (VQFN016V3030)

● Pin Assignment

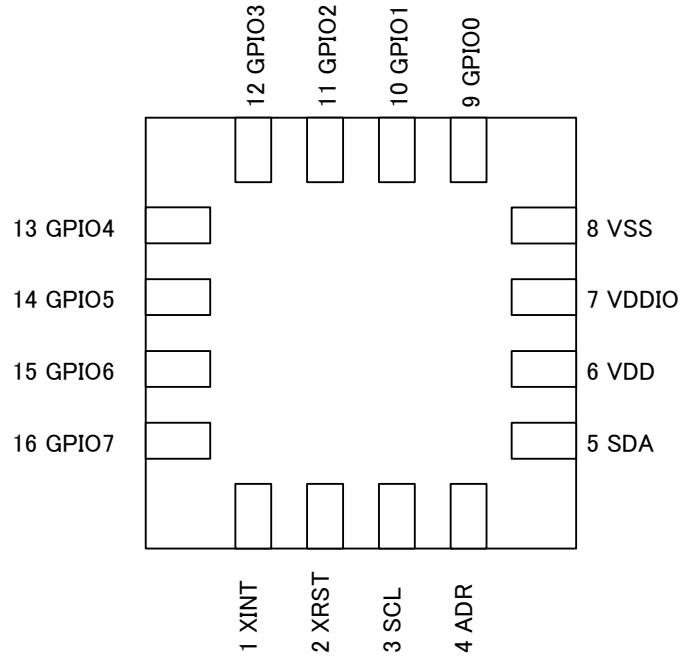


Fig.2 Pin Diagram (Top View)

● Block Diagram

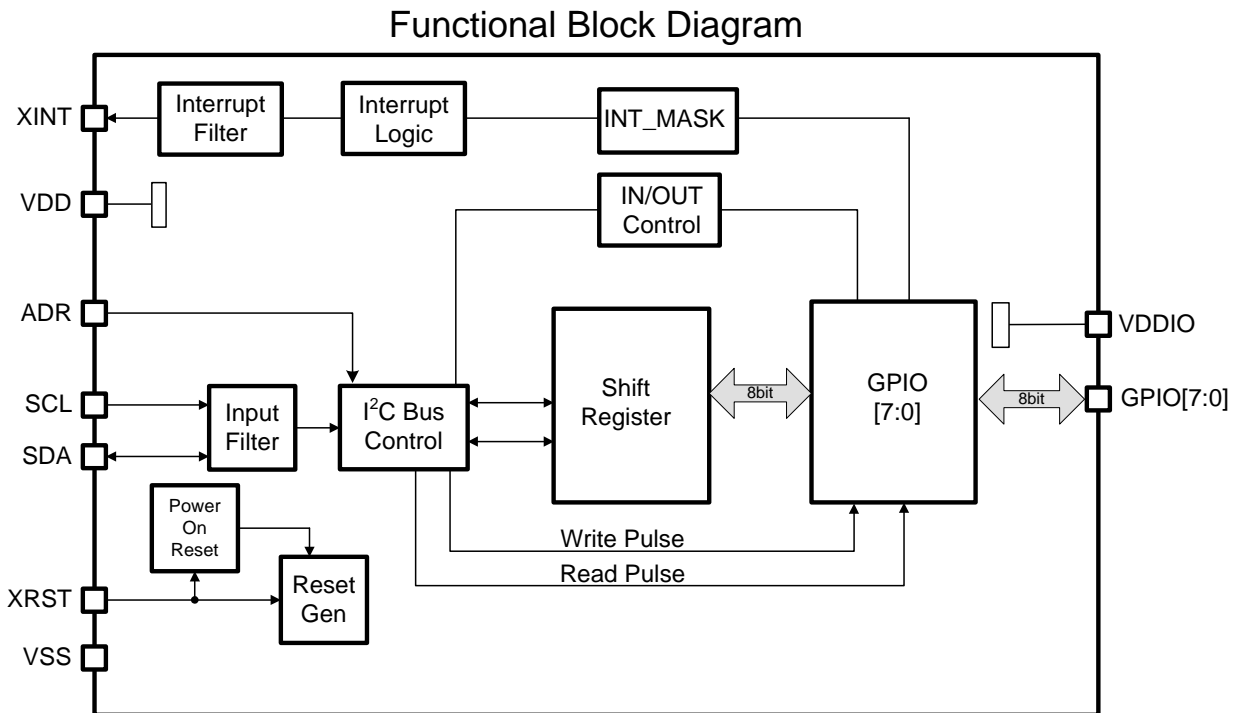


Fig.3 Functional Block Diagram

● Pin-out Functional Descriptions

| PIN No. | PIN name | I/O | Power source system | Function   | Init           | Cell Type |
|---------|----------|-----|---------------------|--|----------------|-----------|
| 1       | XINT     | O   | VDD                 | Interrupt signal (1 $\mu$ s pulse cut) <sup>*1</sup><br>(NMOS Open-drain)  | Hi-Z           | B         |
| 2       | XRST     | I   | VDD                 | Reset (Low Active)   | I              | E         |
| 3       | SCL      | I   | VDD                 | Clock for I <sup>2</sup> C   | I              | A         |
| 4       | ADR      | I   | VDD                 | Select device address of I <sup>2</sup> C  | I              | E         |
| 5       | SDA      | I/O | VDD                 | Serial data inout for I <sup>2</sup> C<br>(NMOS Open-drain)  | Hi-Z           | C         |
| 6       | VDD      | -   | -                   | Power supply (Core, I/O, Power On Reset)   | -              | -         |
| 7       | VDDIO    | -   | -                   | Power supply (I/O)   | -              | -         |
| 8       | VSS      | -   | -                   | GND  | -              | -         |
| 9       | GPIO0    | I/O | VDDIO               | General purpose input/output.<br>(NMOS Open-drain <sup>*2</sup> /CMOS Output,<br>150k $\Omega$ Pull-down <sup>*3</sup> ) | I<br>Pull-down | D         |
| 10      | GPIO1    | I/O | VDDIO               |  |                |           |
| 11      | GPIO2    | I/O | VDDIO               |  |                |           |
| 12      | GPIO3    | I/O | VDDIO               |  |                |           |
| 13      | GPIO4    | I/O | VDDIO               |  |                |           |
| 14      | GPIO5    | I/O | VDDIO               |  |                |           |
| 15      | GPIO6    | I/O | VDDIO               |  |                |           |
| 16      | GPIO7    | I/O | VDDIO               |  |                |           |

\*1 Specific bit mask control is decided by internal register value.  
 \*2 Pull-up more than VDDIO voltage.  
 \*3 It is possible to select Pull-down ON or OFF with register.

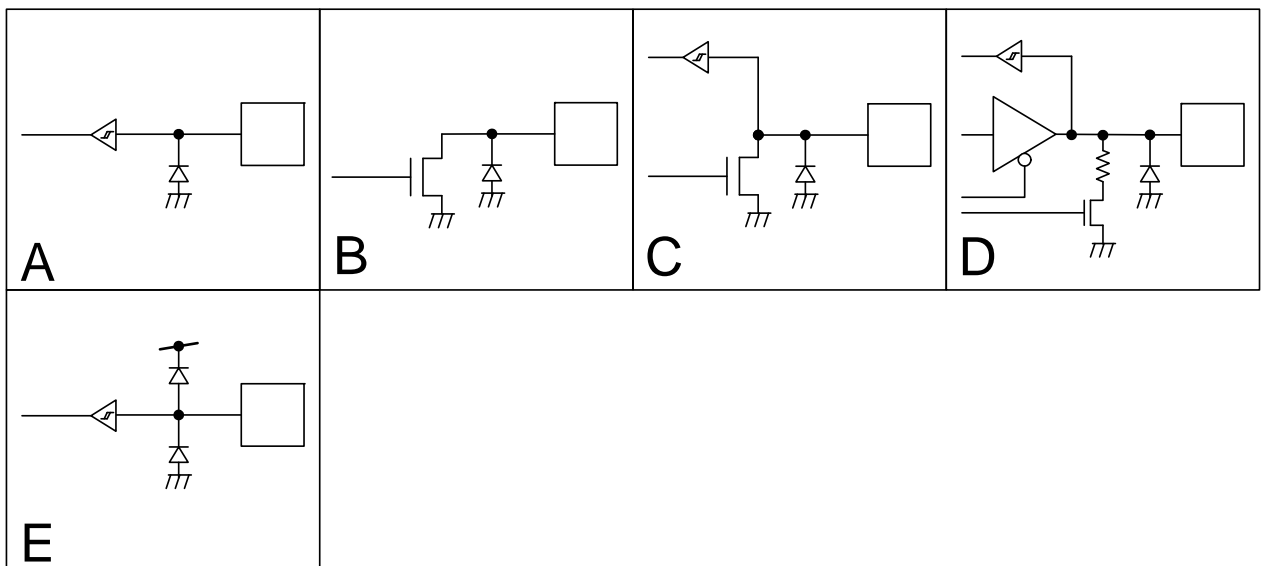


Fig.4 Equivalent IO circuit diagram

**●Functional Description**

## 1. Power Modes

The device enters the state of Power Down when XRST="Low" or enters the operation state when XRST=High after powered.

Refer to "Electrical Specification" section 5 for a detailed startup sequence.

## 1-1 Power supply

A single supply to Core power supply (VDD) and IO power supply (VDDIO) is prohibited.

Supply the power supply to the Core power supply and the IO power supply at the same time.

## 1-2 Power On Reset

A Power On Reset logic is implemented in this device. Therefore, it will operate correctly even if the XRST port is not used. In this case, the XRST port must be connected to high(VDD).

## 1-3 State of Power Down

The device enters the state of Power Down by XRST="Low". An internal circuit is initialized and I<sup>2</sup>C interface is invalid is input. Power On Reset becomes inactive during this state.

## 1-4 State of operation

The device enters the operation state by setting XRST to "High". The I<sup>2</sup>C interface starts communication is the START condition. It becomes standby by the STOP condition. Power On Reset is active in this state.

2. I<sup>2</sup>C Bus Interface

Each function of GPIO is controlled by an internal register. The I<sup>2</sup>C Slave interface is used to write or read this internal register. The device supports up to 400kHz Fast-mode data transfer rate.

2-1 Slave address

Two device addresses (Slave address) can be selected by ADR port.

|       | A7 | A6 | A5 | A4 | A3 | A2 | A1 | R/W |
|-------|----|----|----|----|----|----|----|-----|
| ADR=0 | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 1/0 |
| ADR=1 | 0  | 0  | 0  | 1  | 1  | 1  | 0  |     |

2-2 Data transfer

One bit of data is transferred during SCL = "1". During the bit transfer SCL = "1" cycle, the signal SDA should keep the value. If SDA changes during SCL = "1", a START condition or STOP condition occur and it is interpreted as a control signal.

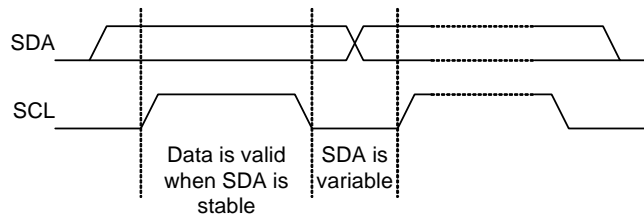


Fig.5 Data transfer

2-3 START-STOP-Repeated START conditions

When SDA and SCL are "1", the data isn't transferred on the 2-wire bus. If SCL remains "1" and SDA transfers from "1" to "0", it means a "Start condition" is occurred and access is started.

If SCL remains "1" and SDA transfers from "0" to "1", it means a "Stop condition" is occurred and access is stopped.

It becomes repeated START condition (Sr) the START condition enters again although the STOP condition is not done.

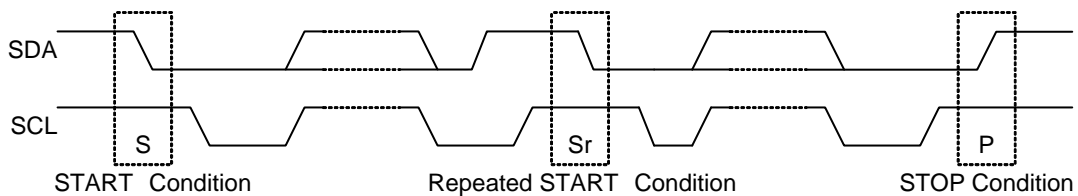


Fig.6 START-STOP-Repeated START conditions

2-4 Acknowledge

After start condition is occurred, 8 bits data will be transferred. SDA is latched by the rising edge of SCL. Then the "Master" opens SDA to "1" and "Slave" de-asserts SDA to "0" as an "Acknowledge" returned.

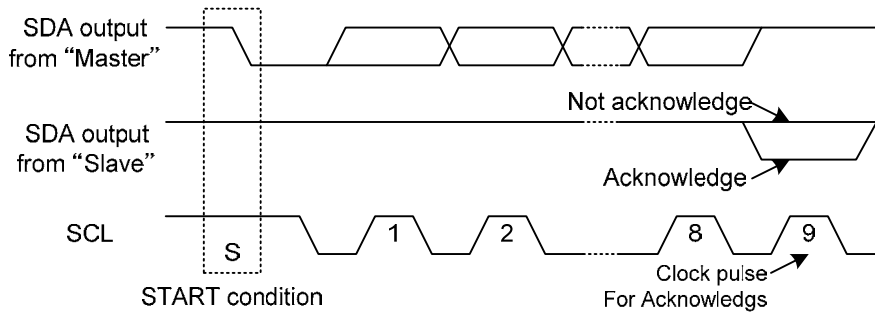


Fig.7 Acknowledge

2-5 Writing protocol

Register address is transferred after one byte of slave address with R/W bit. The 3<sup>rd</sup> byte data is written to internal register which defined by the 2<sup>nd</sup> byte. However, when the register address increased to the final address (13h), it will be reset to (00h) after the byte transfer.

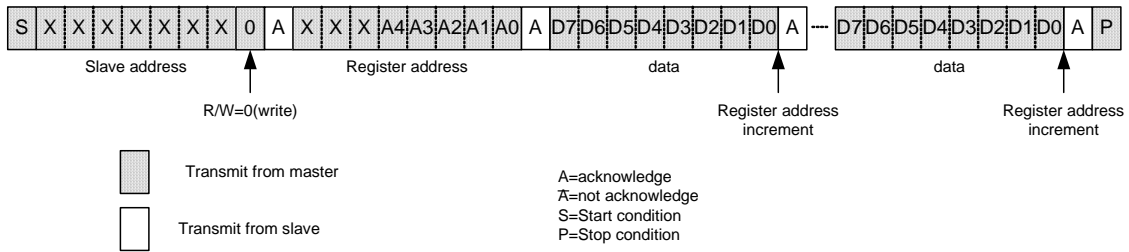


Fig.8 Writing protocol

2-6 Reading protocol

After Writing the slave address and Read/Write command bits, the next byte is read. The reading register address is next of previous accessed address. Therefore, the data is read with address increment. When the address is increased to the last, the following read address will be reset to (00h).

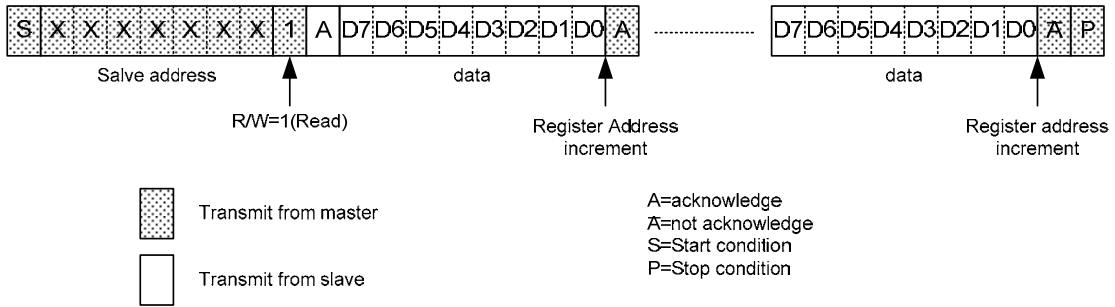


Fig.9 Readout protocol

2-7 Complex reading protocol

After the specifying the internal register address, a repeated START condition occurs and the direction of data transfer is changed then reading access is done. Therefore, the data is read followed by address increment. If the address is increased to the last, it will be reset to (00h).

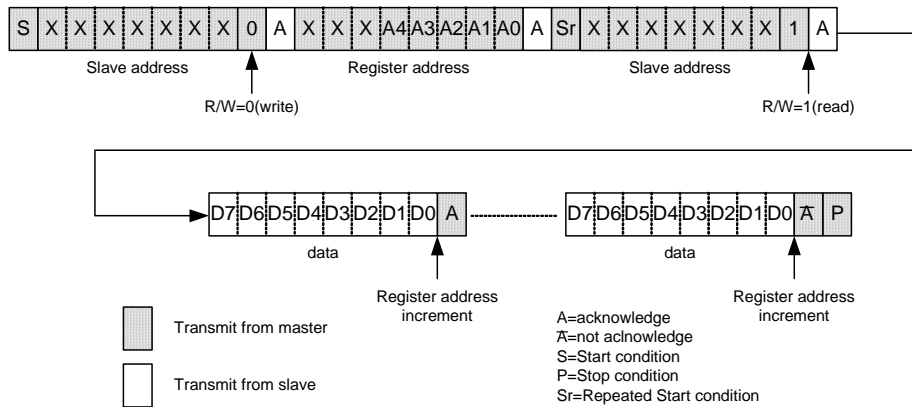


Fig.10 Complex reading protocol

2-8 Illegal access of I<sup>2</sup>C

The data accessed at that time is annulled, and access it again.

The illegal accesses are as follows.

- The START condition and the STOP condition are continuously generated.
- When the Slave address and the R/W bit is written, repeated START condition and the STOP condition are generated.
- Repeated START condition and the STOP condition are generated while writing data.



## 3. Register configuration

The address is increased one by one when data is continuously written.

When the final address is set to 13h, then the next address 00h will be written.

By making XRST "Low", the setting register value will be initialed shown in following register map.

## 3-1 Register map

| Addr | Init | Type | D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       |
|------|------|------|----------|----------|----------|----------|----------|----------|----------|----------|
| 00h  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 01h  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 02h  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 03h  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 04h  | 00h  | R/W  | RESET    | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 05h  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 06h  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 07h  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 08h  | 00h  | R/W  | INTEN7   | INTEN6   | INTEN5   | INTEN4   | INTEN3   | INTEN2   | INTEN1   | INTEN0   |
| 09h  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 0Ah  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 0Bh  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 0Ch  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 0Dh  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 0Eh  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 0Fh  | -    | -    | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
| 10h  | 00h  | R    | GPI7     | GPI6     | GPI5     | GPI4     | GPI3     | GPI2     | GPI1     | GPI0     |
| 11h  | 00h  | R/W  | GPO7     | GPO6     | GPO5     | GPO4     | GPO3     | GPO2     | GPO1     | GPO0     |
| 12h  | 00h  | R/W  | WRSEL7   | WRSEL6   | WRSEL5   | WRSEL4   | WRSEL3   | WRSEL2   | WRSEL1   | WRSEL0   |
| 13h  | 00h  | R/W  | XPD7     | XPD6     | XPD5     | XPD4     | XPD3     | XPD2     | XPD1     | XPD0     |

※ Do not write reserved registers excluding "0". 10h address register is disregarded even if it is written.

## 3-2 Register function

※ n is the number of GPIO[7:0] ports.

| Symbol             | Addr | Description  |
|--------------------|------|--|
| RESET              | 04h  | The register is returned to an initial value by writing "1". This register value is returned to "0". GPI <sub>n</sub> register is not initialized. |
| INTEN <sub>n</sub> | 08h  | Interrupt of GPI <sub>n</sub> port is enabled by "1". It is masked by "0".   |
| GPI <sub>n</sub>   | 10h  | Read GPI <sub>n</sub> port. Writing is disregarded.  |
| GPO <sub>n</sub>   | 11h  | Output value of GPI <sub>n</sub> port.   |
| WRSEL <sub>n</sub> | 12h  | GPI <sub>n</sub> port is input by "0" and output by "1".   |
| XPD <sub>n</sub>   | 13h  | Pull-down of GPI <sub>n</sub> port is on by "0" and off by "1". GPI <sub>n</sub> should be input.  |

4. GPIO-Interrupt

4-1 GPIO configuration

As the default value, GPIO[7:0] ports are input and Pull-down.

At this time, WRSELn is "0" and XPDn is "0". (n is the number of GPIO[7:0] ports.)

Refer to the following for the configuration of GPIO.

| State of GPIO                 | Register |        |      |
|-------------------------------|----------|--------|------|
|                               | GPOn     | WRSELn | XPDn |
| Input, Pull-down ON           | *        | 0      | 0    |
| Input, Pull-down OFF          | *        | 0      | 1    |
| Output, H drive               | 1        | 1      | *    |
| Output, L drive               | 0        | 1      | *    |
| Output, Hi-Z -1※ <sup>1</sup> | 0        | 0      | 1    |

※<sup>1</sup> Make external Pull-up the terminal potential which is the potential of V<sub>VDDIO</sub> or more.

- About GPIO port not used  
 When making it to the output, open it.  
 When making it to the input, do not open it. It is forced by "0" or Pull-down on.  
 When interrupt is enabled, mask INTEN register in which the port is not used to "0".

4-2 Interrupt configuration

When interrupt is generated, L is output from XINT port. The default value is Hi-Z. Make it Pull-up.

For the default value, interrupt is masked with INTEN register "0".

The bit to be used is made "1", and the mask is released. WRSEL register should be "0"(input).

4-3 Write to GPIO port

After setting the internal register address, the data from master is written from MSB.

After Acknowledge is returned, the value of each GPIO port will be changed.

When the register is written, Write Configuration Pulse is generated according to the timing of Acknowledge.

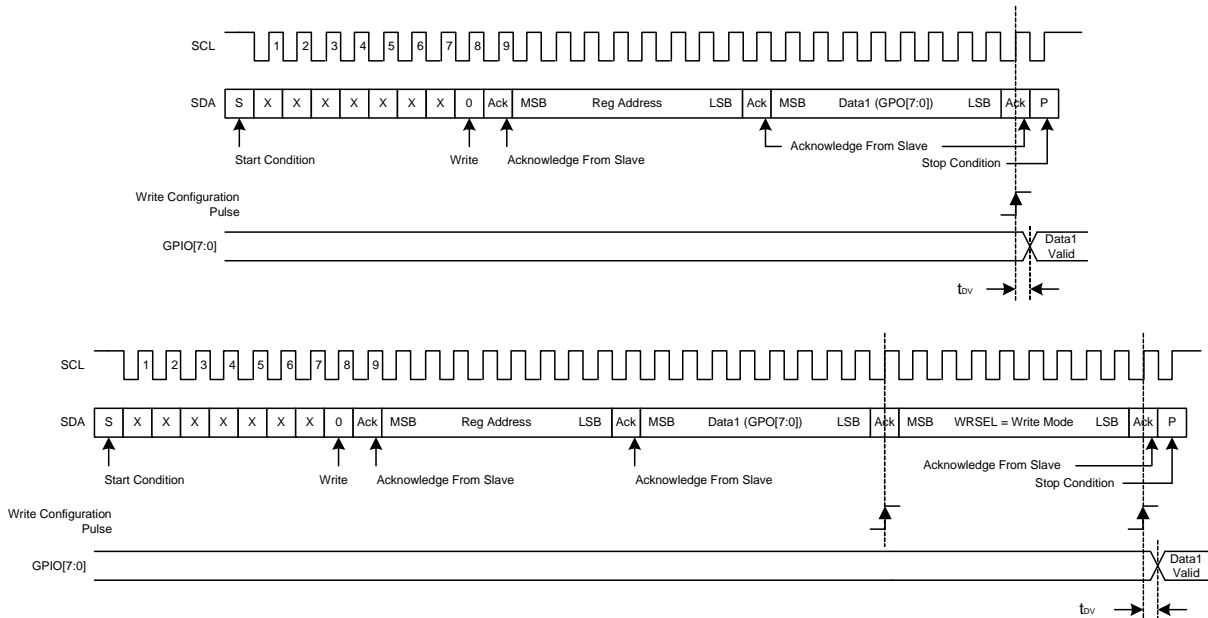


Fig.11 Write to GPIO port

4-4 Read from GPIO port

After writing of the Slave address and R/W bits, reading GPIO port is begun from the following byte.

The data that had been being fixed between the following Acknowledge after Acknowledge is taken into the GPI register, and it is transmitted to Master.

All ports that are the input by WRSEL register are read to the GPI register according to the timing of Read Configuration Pulse. Therefore, the data of each bit that SDA transmits is the GPI register value taken immediately before that.

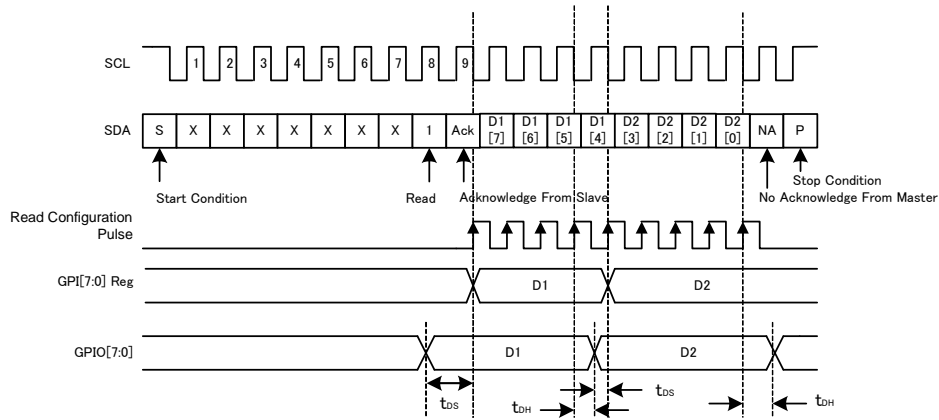


Fig.12 Read from GPIO port

4-5 Interrupt Valid/Reset

If GPIO port becomes different from the GPIIn register (default is "0"), XINT port is changed from "1" into "0".

It becomes "1" to release "0" of XINT port after acknowledge by reading GPI register. Because the value of GPIO port is reflected in the output as it is and is not latched, XINT becomes "1" again if the port returns to the same value.

If the ports with INTEN register "1" are different even by one, XINT becomes "0".

If it is distinguished which GPIO port changes, it is necessary to keep the GPI register value on the master side and compare with the value that is read after XINT is asserted.

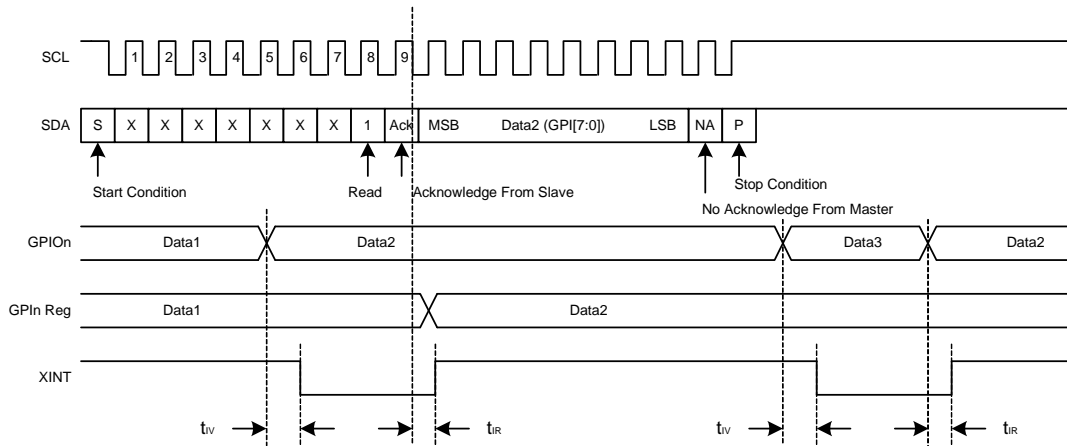


Fig.13 Interrupt Valid/Reset

## ●Electrical Specification

## 1. DC characteristics

 $V_{VDD}=1.8V$ ,  $V_{VDDIO}=1.8V$ ,  $T_{opr}=25^{\circ}C$ 

| Parameter                         | Symbol    | Specification           |     |                         | Unit    | Conditions                  |
|-----------------------------------|-----------|-------------------------|-----|-------------------------|---------|-----------------------------|
|                                   |           | Min                     | Typ | Max                     |         |                             |
| Input H Voltage1                  | $V_{IH1}$ | $0.7 \times V_{VDDIO}$  | -   | 3.6                     | V       | GPIO[7:0]                   |
| Input L Voltage1                  | $V_{IL1}$ | -0.2                    | -   | $0.3 \times V_{VDDIO}$  | V       |                             |
| Input H Voltage2                  | $V_{IH2}$ | $0.7 \times V_{VDD}$    | -   | 3.6                     | V       | SCL, SDA,                   |
| Input L Voltage2                  | $V_{IL2}$ | -0.2                    | -   | $0.3 \times V_{VDD}$    | V       | SCL, SDA, XRST, ADR         |
| Input H Voltage3                  | $V_{IH3}$ | $0.7 \times V_{VDD}$    | -   | $V_{VDD}+0.2$           | V       | XRST, ADR                   |
| Input H Current1<br>(3V Tolerant) | $I_{IH1}$ | -1                      | -   | 1                       | $\mu A$ | $V_{IN}=3.6V^{*1}$          |
| Input H Current2                  | $I_{IH2}$ | -1                      | -   | 1                       | $\mu A$ | $V_{IN}=1.8V$ , XRST,ADR    |
| Input L Current                   | $I_{IL}$  | -1                      | -   | 1                       | $\mu A$ | $V_{IN}=0V^{*1}$ , XRST,ADR |
| Output H Voltage1                 | $V_{OH1}$ | $0.75 \times V_{VDDIO}$ | -   | -                       | V       | $I_{OH}=-2mA$ , GPIO[7:0]   |
| Output L Voltage1                 | $V_{OL1}$ | -                       | -   | $0.25 \times V_{VDDIO}$ | V       | $I_{OL}=2mA$ , GPIO[7:0]    |
| Output H Voltage2                 | $V_{OH2}$ | $V_{VDDIO}-0.25$        | -   | -                       | V       | $I_{OH}=-0.2mA$ , GPIO[7:0] |
| Output L Voltage2                 | $V_{OL2}$ | -                       | -   | 0.25                    | V       | $I_{OL}=0.2mA$ , GPIO[7:0]  |
| Output L Voltage3                 | $V_{OL3}$ | -                       | -   | 0.3                     | V       | $I_{OL}=3mA$ , SDA, XINT    |

\*1 XINT(HI-Z), XRST, SCL, SDA(IN), ADR, GPIO[7:0](IN, Pull-down OFF)

## 2. Circuit Current

 $V_{VDD}=1.8V$ ,  $V_{VDDIO}=1.8V$ ,  $T_{opr}=25^{\circ}C$ 

| Parameter                     | Symbol      | Specification |     |     | Unit    | Condition   |
|-------------------------------|-------------|---------------|-----|-----|---------|---|
|                               |             | Min           | Typ | Max |         |   |
| Power Down Current<br>(VDD)   | $I_{PD1}$   | -             | -   | 1.0 | $\mu A$ | XRST=VSS  |
| Power Down Current<br>(VDDIO) | $I_{PD2}$   | -             | -   | 1.0 | $\mu A$ |   |
| Standby Current<br>(VDD)      | $I_{STBY1}$ | -             | -   | 3.0 | $\mu A$ | XRST=VDD,<br>SCL=VDD, SDA=VDD                                 |
| Standby Current<br>(VDDIO)    | $I_{STBY2}$ | -             | -   | 1.0 | $\mu A$ |   |
| Operating Current1<br>(VDD)   | $I_{OP1}$   | -             | 14  | 25  | $\mu A$ | I <sup>2</sup> C 400kHz<br>100% traffic density <sup>*1</sup> |
| Operating Current1<br>(VDD)   | $I_{OP2}$   | -             | 2   | 8   | $\mu A$ | I <sup>2</sup> C 400kHz<br>1% traffic density <sup>*2</sup>   |

\*1 All GPIO ports are output, and they repeat 01010101 and 10101010.

\*2 The period when I<sup>2</sup>C did not operate was inserted in \*1 pattern by 99%.

3. I<sup>2</sup>C AC characteristics

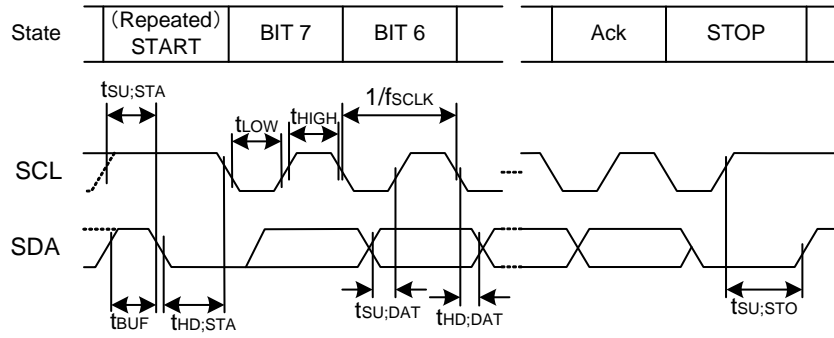


Fig.14 I<sup>2</sup>C AC Timing

V<sub>VDD</sub>=1.8V, V<sub>VDDIO</sub>=1.8V, Topr=25°C

| Parameter                            | Symbol              | Specification |     |     | Unit | Conditions |
|--------------------------------------|---------------------|---------------|-----|-----|------|------------|
|                                      |                     | Min           | Typ | Max |      |            |
| SCL Clock Frequency                  | f <sub>SCLK</sub>   | -             | -   | 400 | kHz  |            |
| Bus free time                        | t <sub>BUF</sub>    | 1.3           | -   | -   | μs   |            |
| (Repeated)START Condition Setup Time | t <sub>SU,STA</sub> | 0.6           | -   | -   | μs   |            |
| (Repeated)START Condition Hold Time  | t <sub>HD,STA</sub> | 0.6           | -   | -   | μs   |            |
| SCL Low Time                         | t <sub>LOW</sub>    | 1.3           | -   | -   | μs   |            |
| SCL High Time                        | t <sub>HIGH</sub>   | 0.6           | -   | -   | μs   |            |
| Data Setup Time                      | t <sub>SU,DAT</sub> | 100           | -   | -   | μs   |            |
| Data Hold Time                       | t <sub>HD,DAT</sub> | 0             | -   | -   | ns   |            |
| STOP Condition Setup Time            | t <sub>SU,STO</sub> | 0.6           | -   | -   | μs   |            |

4. GPIO AC Characteristics

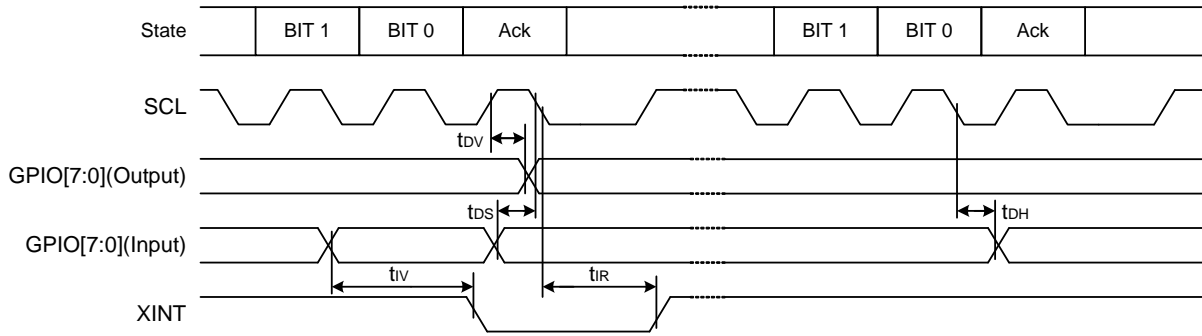


Fig.15 GPIO AC timing

$V_{VDD}=1.8V$ ,  $V_{VDDIO}=1.8V$ ,  $Topr=25^{\circ}C$

| Parameter              | Symbol   | Specification |     |     | Unit    | Conditions |
|------------------------|----------|---------------|-----|-----|---------|------------|
|                        |          | Min           | Typ | Max |         |            |
| Output Data Valid Time | $t_{DV}$ | -             | -   | 0.8 | $\mu s$ | See Fig.11 |
| Input Data Setup Time  | $t_{DS}$ | 100           | -   | -   | ns      | See Fig.12 |
| Input Data Hold Time   | $t_{DH}$ | 0.8           | -   | -   | $\mu s$ |            |
| Interrupt Valid Time   | $t_{IV}$ | -             | -   | 5   | $\mu s$ | See Fig.13 |
| Interrupt Reset Time   | $t_{IR}$ | -             | -   | 5   | $\mu s$ |            |

5. Startup sequence

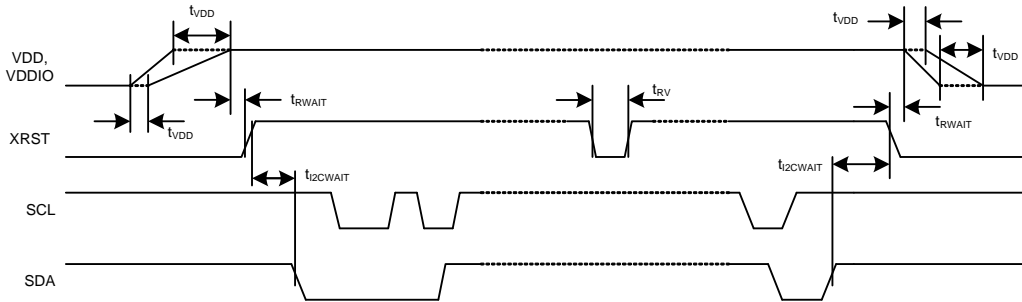


Fig.16 Start Sequence timing

V<sub>VDD</sub>=1.8V, V<sub>VDDIO</sub>=1.8V, T<sub>opr</sub>=25°C

| Parameter                  | Symbol               | Specification |     |     | Unit | Conditions                             |
|----------------------------|----------------------|---------------|-----|-----|------|--|
|                            |                      | Min           | Typ | Max |      |  |
| VDD Stable Time            | t <sub>VDD</sub>     | -             | -   | 5   | ms   | VDD and VDDIO are ON at the same time. |
| Reset Wait Time            | t <sub>RWAIT</sub>   | 0             | -   | -   | μs   | XRST controlling *1                    |
| Reset Valid Time           | t <sub>RV</sub>      | 10            | -   | -   | μs   |  |
| I <sup>2</sup> C Wait Time | t <sub>I2CWAIT</sub> | 10            | -   | -   | μs   |  |

\*1 Even if XRST port is not used, it operates because Power On Reset is built in. In this case, connect XRST port with VDD on the set PCB.

Note) At VDD=0V, when SCL port is changed from 0V to 0.5V or more, SCL port pulls the current. It is same in SDA, XINT, and GPIO[7:0] ports of 3V tolerant I/O. (VDDIO=0V in case of GPIO[7:0] ports)

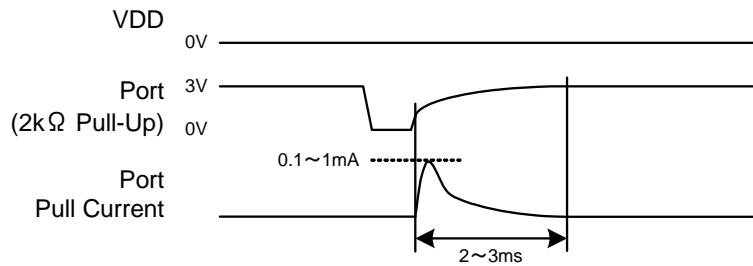


Fig.17 Port operating at VDD=0V

●Application circuit example

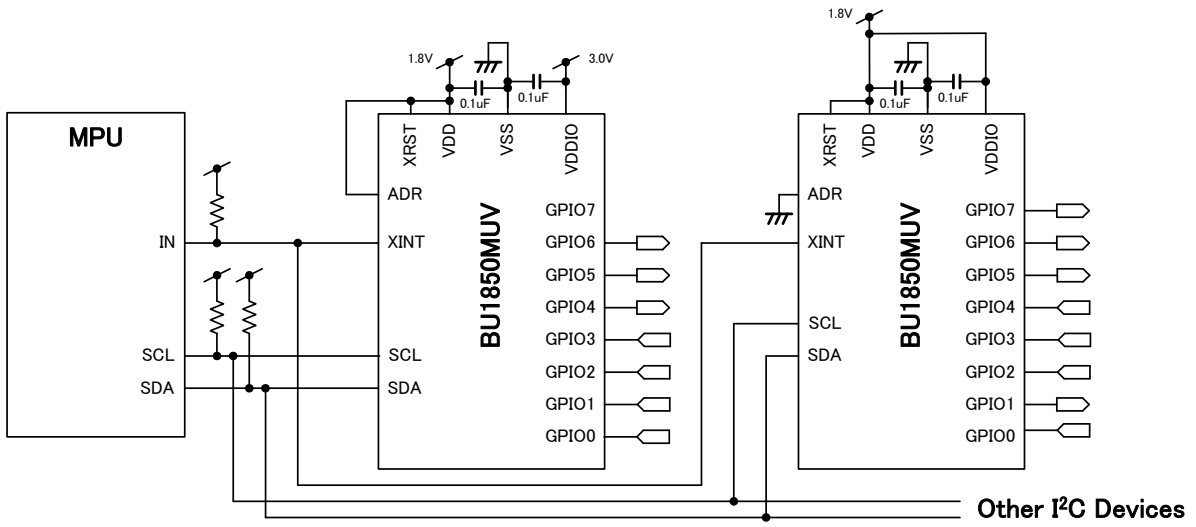


Fig.18 Application circuit example



●Ordering part number

|   |   |
|---|---|
| B | U |
|---|---|

Part No.

|   |   |   |   |
|---|---|---|---|
| 1 | 8 | 5 | 0 |
|---|---|---|---|

Part No.

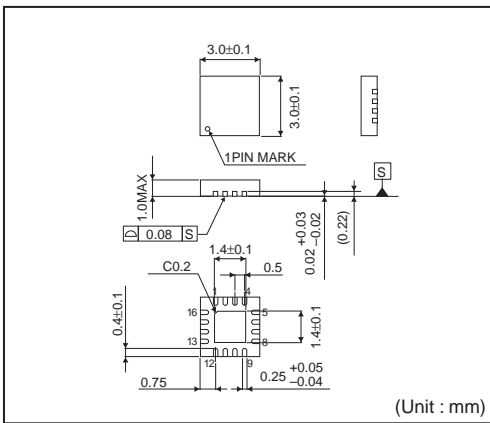
|   |   |   |
|---|---|---|
| M | U | V |
|---|---|---|

Package  
MUV:  
VQFN016V3030

|   |   |   |
|---|---|---|
| - | E | 2 |
|---|---|---|

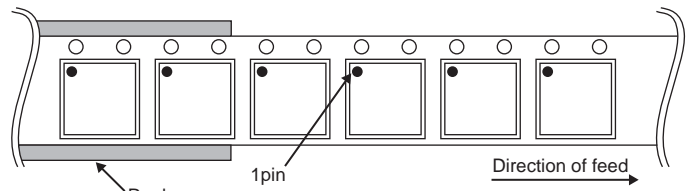
Packaging and forming specification  
E2: Embossed tape and reel

VQFN016V3030



<Tape and Reel information>

|                   |   |
|-------------------|---|
| Tape              | Embossed carrier tape   |
| Quantity          | 3000pcs   |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



\*Order quantity needs to be multiple of the minimum quantity.

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| JAPAN     | USA       | EU         | CHINA     |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV  |           | CLASS III  |           |

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  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - Sealing or coating our Products with resin or other coating materials
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  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
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3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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