# NCV7429

# System Basis Chip with LIN, LS and HS Switches

ON Semiconductor®

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**TSSOP−20 EP**
**CASE 948AB**

### Description

The NCV7429 is a monolithic LIN System-Basis-Chip with enhanced feature set useful in Automotive Body Control systems. Besides the LIN bus interface the IC features a 5 V voltage regulator, high-side and low-side switches to control LEDs and relays, and supervision functionality like a window watchdog. This allows a highly integrated solution by replacing external discrete components while maintaining the system flexibility. As a consequence, the board space and ECU weight can be minimized.

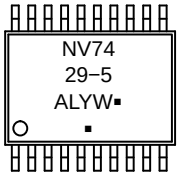
### Features

- Main Supply Functional Operating Range from 5 V to 28 V
- Main Supply Parametrical Operating Range 6 V to 18 V
- LIN Physical Layer According to ISO 17987−4 (backwards compatible to LIN 1.3, LIN 2.x) and SAE J2602
- Power Management Through Operating Modes: Normal, Standby, Sleep and Flash
- Software Development Mode for Software Debugging
- Low Drop Voltage Regulator VR1: 5 V/150 mA, 2%
- One Wake-up Input, e.g. for Contact Monitoring
- Wake-up Logic with Cyclic Contact Monitoring
- Wake-up Source Recognition
- Independent PWM Functionality for All Outputs (Integrated PWM Registers)
- Window Watchdog with Programmable Times
- 2x Low-side Driver (typ. 1.5 Ω) with Over-load Protection and Active Clamp; e.g. for Relays
- 3x High-side Driver (typ. 5 Ω) with Over- and Under-load Detection; e.g. for LED's and Switches
- 24-bit SPI Interface
- Protection against Short Circuit, Over-voltage and Over-temperature
- TSSOP−20 EP Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- De-centralized Door Electronic Systems

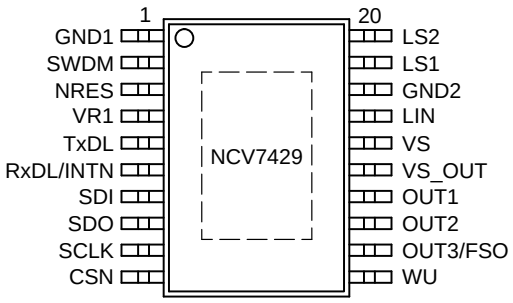
### MARKING DIAGRAM




| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb-Free Package |

(Note: Microdot may be in either location)

### PIN ASSIGNMENT




(Top View)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCV7429DE5R2G | TSSOP−20 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## BLOCK DIAGRAM

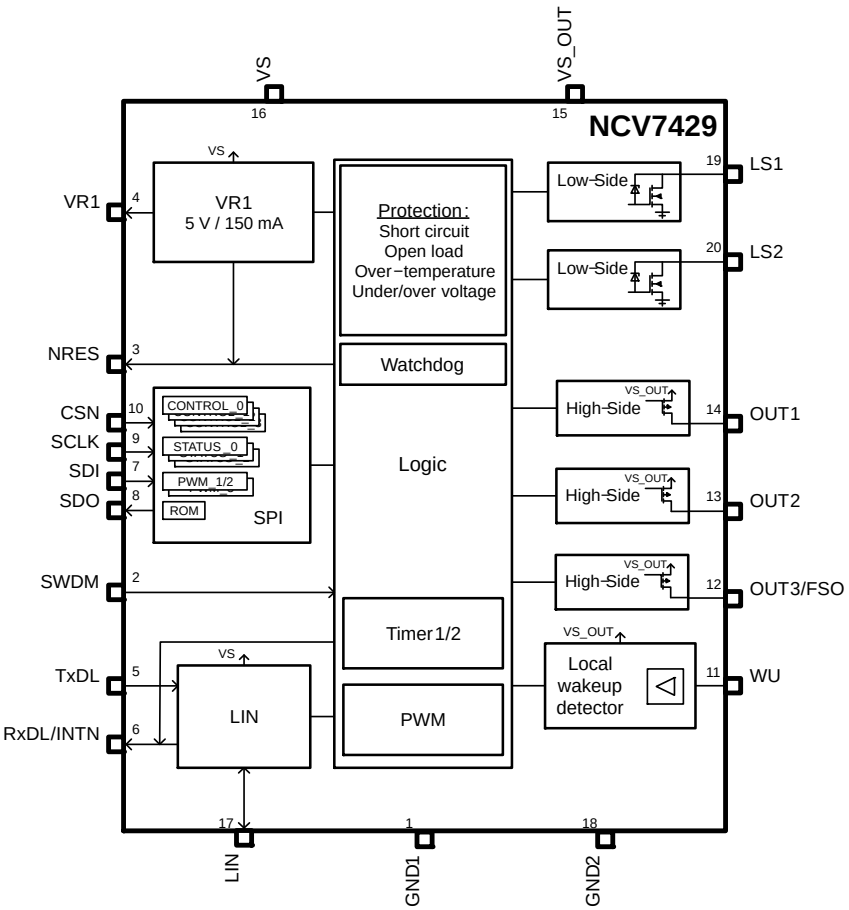



**Figure 1. Block Diagram**

**Table 1. PIN DESCRIPTION**

| Pin No. | Pin Name | Pin Type | Description |
|---|---|---|---|
| 1 | GND1 | Ground | Ground connection |
| 2 | SWDM | HV Digital Input with Pull-down | Software development mode entry input |
| 3 | NRES | Digital Open-drain Output with Internal Pull-up | Reset signal to the MCU |
| 4 | VR1 | 5 V Regulator Output | 2%, 150 mA |
| 5 | TxDL | Digital Input with Pull-up | Transmitter data input of the LIN transceiver |
| 6 | RxDL/INTN | Digital Push-pull Output | Receiver output of the LIN transceiver/Interrupt output |
| 7 | SDI | Digital Input with Pull-down | SPI data input |
| 8 | SDO | Digital Push-pull Output, Tristate | SPI data output |
| 9 | SCLK | Digital Input with Pull-down | SPI clock input |
| 10 | CSN | Digital Input with Pull-up | SPI chip select input |
| 11 | WU | HV Input | Voltage-sense input (threshold typ. VS_OUT/2), switched pull-up/down |
| 12 | OUT3/FSO | HS Driver | Resistive loads, Ron 5 Ω typ, Ilim > 140 mA / FSO output |
| 13 | OUT2 | HS Driver | Resistive loads, Ron 5 Ω typ, Ilim > 140 mA |

**Table 1. PIN DESCRIPTION** (continued)

| Pin No. | Pin Name | Pin Type | Description |
|---|---|---|---|
| 14 | OUT1 | HS Driver | Resistive loads, Ron 5/20 Ω typ, Ilim > 140/35 mA, two configurations |
| 15 | VS_OUT | Battery Supply Input | Power-supply of the high-side drivers OUT1−3 and WU input |
| 16 | VS | Battery Supply Input | Principle power-supply of the device |
| 17 | LIN | LIN Bus Interface | LIN bus pin, low in dominant state |
| 18 | GND2 | Ground | Ground connection |
| 19 | LS1 | LS Driver | Low-side Driver, Ron 1.5 Ω typ, Ilim > 250 mA, active clamp to ground |
| 20 | LS2 | LS Driver | Low-side Driver, Ron 1.5 Ω typ, Ilim > 250 mA, active clamp to ground |
| | Exposed Pad | Ground | Substrate; Exposed pad has to be connected to both GND pins |

## APPLICATION INFORMATION

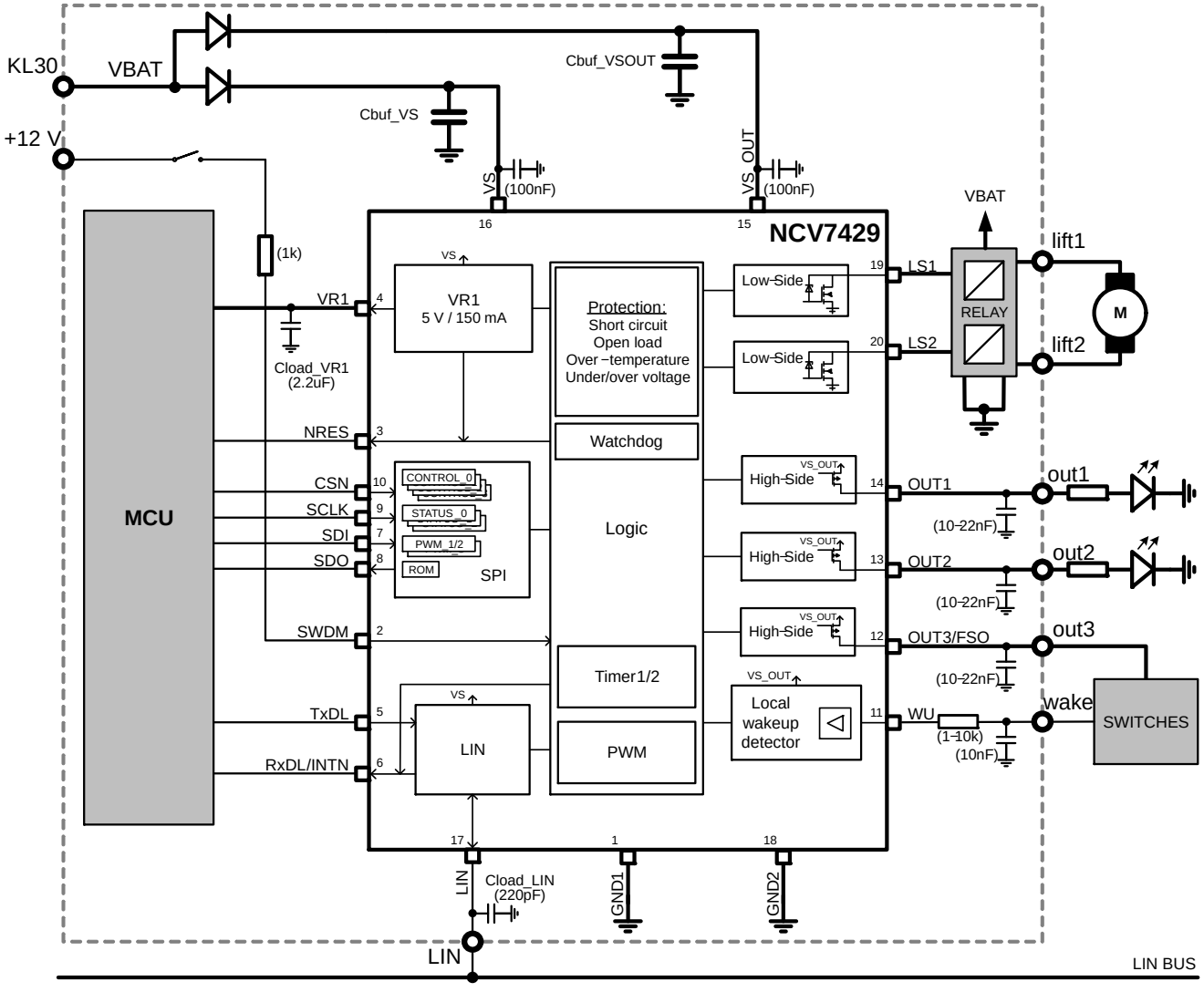



**Figure 2. Example Application Diagram**

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Vmax_VS, Vmax_VS_OUT | Power Supply Voltage | −0.3 | 40 | V |
| Vmax_WU | Wake Pin Voltage Range | −0.3 | VS_OUT + 0.3 | V |
| Vmax_OUT1−3 | High-side Output OUT1−3 Voltage Range | −0.3 | VS_OUT + 0.3 | V |
| Vmax_LS1/2 | LS1/2 Pin Voltage Range DC (Voltage Internally Limited during Flyback) | −0.3 | 40 | V |
| Wmax_LS1/2 | Maximum LS1/2 Clamping Energy | | 36 | mJ |
| Imax_LS1/2 | Maximum LS1/2 Pin Current | | 500 | mA |
| | Maximum LS1/2 Pin Current, Transient or without VS and VS_OUT Supply | −120 | | mA |
| Vmax_LIN | DC Voltage on LIN Pin | −40 | 40 | V |
| Vmax_VR1 | Stabilized Supply Voltage, Logic Supply | −0.3 | min(5.5, VS + 0.3) | V |
| Vmax_digIO | DC Voltage at Digital Pins (NRES, TxDL, RxDL/INTN, SDI, SDO, SCLK, CSN) | −0.3 | VR1 + 0.3 | V |
| Vmax_SWDM | DC Voltage at SWDM Input | −0.3 | 40 | V |
| ESD Human Body Model Following EIA−JESD22 (100 pF, 1500 Ω) | All Pins | −2 | +2 | kV |
| | Pin LIN to GND | −4 | +4 | |
| | Pins OUT1−3, LS1/2 to GND | −4 | +4 | |
| ESD Following IEC 61000−4−2 (150pF, 330Ω) | Valid for Pins VS, VS_OUT, LIN, OUT1−3, WU<br>− VS, VS_OUT pins with reverse-protection and filtering capacitor<br>− OUT1−3 pins with parallel capacitor 10 nF<br>− WU pin stressed through a serial resistor > 10 kΩ | −6 | +6 | kV |
| ESD Charged Device Model Following JESD22−C101/AEC−Q100−011 | All Pins | −500 | +500 | V |
| | Corner Pins | −750 | +750 | V |
| $T_{j\_mr}$ | Junction Temperature | −40 | +170 | °C |
| $T_{stg}$ | Storage Temperature Range | −55 | +150 | °C |
| MSL | Moisture Sensitivity Level (max. 260°C Processing) | 2 | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. THERMAL CHARACTERISTICS**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| | Thermal Characteristics | | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 8.3 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient, 1S0P PCB (Note 1) | 70 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient, 2S2P PCB (Note 2) | 40 | |

1. Value based on test board according to JESD51−3 standard, signal layer with 10% trace coverage.
2. Value based on test board according to JESD51−7 standard, signal layers with 20% trace coverage, inner planes with 90% coverage.

**Table 4. RECOMMENDED OPERATING RANGES**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Vop_VS_par, Vop_VS_OUT_par | Power Supply Voltage for Valid Parameter Specifications | 6 | 18 | V |
| Vop_VS_func, Vop_VS_OUT_func | Power Supply for Correct Functional Behavior | 5 | 28 | V |
| Vop_WU | Wake Pin Voltage Range | 0 | VS_OUT | V |
| Vop_OUT1−3 | High-side Output OUT1−3 Voltage Range | 0 | VS_OUT | V |
| Vop_LS1/2 | LS1/2 Pin Voltage Range DC (voltage internally limited during flyback) | 0 | VS_OUT | V |
| Vop_LIN | LIN Pin Voltage Range | 0 | VS | V |
| Vop_VR1 | Stabilized Supply Voltage, Logic Supply | 4.9 | 5.1 | V |
| Vop_digIO | DC Voltage at Digital Pins (NRES, TxDL, RxDL/INTN, SDI, SDO, SCLK, CSN) | 0 | VR1 | V |
| Vop_SWDM | DC Voltage at SWDM Input | 0 | VS | V |
| $T_{j\_op}$ | Junction Temperature | −40 | +150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 5. ELECTRICAL CHARACTERISTICS**

($6\ V \le V_S \le 18\ V$, $6\ V \le V_{S\_out} \le 18\ V$, $-40°C \le T_j \le 150°C$; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VS SUPPLY** | | | | | | |
| VS, VS_OUT | Supply Voltage | Functional, Voltage Regulators with Deteriorated Performance | 5 | | 28 | V |
| | | Parameter Specification | 6 | | 18 | |
| VS_PORH | VS POR Threshold | VS Rising | 3.4 | | 4.1 | V |
| VS_PORL | VS POR Threshold | VS Falling | 2.1 | | 3.0 | V |
| VS_OUT_UV | VS_OUT UV-threshold Voltage | VS Falling | 5.1 | | 5.8 | V |
| VS_OUT_UV_hyst | Undervoltage Hysteresis | | 0.1 | | 0.5 | V |
| VS_OUT_OV | VS_OUT OV-threshold Voltage | VS Rising | 20 | | 22 | V |
| VS_OUT_OV_hyst | Overvoltage Hysteresis | | 0.3 | 0.5 | 0.8 | V |
| I_VS_norm | VS Consumption in Normal Mode | Normal mode, VR1 on (not loaded), bus communication off, TxDL not active | | 0.6 | 1.1 | mA |
| I_VS_stby | VS Consumption in Standby Mode (Static Sense) | Standby mode, VS = 12 V, VR1 on (not loaded), no LIM bus communication, no wake-up request pending, WU wakeup disabled, $T_j$ = 85°C (Note 3) | | 28 | 60 | μA |
| I_VS_sleep | VS Consumption in Sleep Mode (Static Sense) | Sleep mode, VS = 12 V, VR1 off, no LIM bus communication, no wake-up request pending, WU wakeup disabled, $T_j$ = 85°C (Note 3) | | 15 | 30 | μA |
| I_VS_add_VR1 | VR1 Current Consumption from VS | Normal/Standby mode, VR1 loaded | | 0.005 · I_VR1 | | mA |
| I_VS_add_LS | Added LSx Drivers Current Consumption from VS | N = 1 – 2 … number of LSx drivers active | | 15 + 20·N | 110 | μA |

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
(6 V ≤ $V_S$ ≤ 18 V, 6 V ≤ $V_{S\_out}$ ≤ 18 V, −40°C ≤ $T_j$ ≤ 150°C; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VS SUPPLY** | | | | | | |
| I_VS_add_WU | Added WU Comparator Current Consumption from VS | | | 0.6 | 2 | μA |
| **VS_OUT SUPPLY** | | | | | | |
| I_VSOUT_norm | VS_OUT Consumption in Normal Mode | Normal mode, OUT1−3 off, floating | | 15 | 30 | μA |
| I_VSOUT_stby | VS_OUT Consumption in Standby Mode | Standby mode, OUT1−3 off, floating, WU wakeup disabled, WU pin floating | | 0 | 2 | μA |
| I_VSOUT_sleep | VS_OUT Consumption in Sleep Mode | Sleep mode, OUT1−3 off, floating, WU wakeup disabled, WU pin floating | | 0 | 2 | μA |
| I_VSOUT_add_OUT | Added OUTx Drivers Current Consumption from VS_OUT | Normal mode, OUTx = floating, N = 1 – 3 … number of OUTx drivers active | | 15 x N | 90 | μA |
| | | Standby/Sleep mode, OUTx = floating, N = 1 – 3 … number of OUTx drivers active | | 15 + 15 x N | 120 | μA |
| I_VSOUT_add_WU | Added WU Comparator Current Consumption from VS_OUT | WU pin floating | | 4 | 8 | μA |
| **VS + VS_OUT SUPPLY COMBINED CONSUMPTIONS** | | | | | | |
| I_stby_cs | VS + VS_OUT Consumption in Standby Mode (with Cyclic Sense) | Standby mode, VS = VS_OUT = 12 V, VR1 on (not loaded), OUTx floating, driven by Timer1/2, bus communication off, No wake-up request pending, $T_j$ = 25°C (Note 3) | | (Note 4) | | μA |
| I_sleep_cs | VS + VS_OUT Consumption in Sleep Mode (with Cyclic Sense) | Sleep mode, VS = VS_OUT = 12 V, VR1 off, OUTx floating, driven by Timer1/2, bus communication off, No wake-up request pending, $T_j$ = 25°C (Note 3) | | (Note 5) | | μA |
| I_FailSafe | VS + VS_OUT Consumption in Fail-safe Mode | Fail-safe mode, OUTx floating, OUT3/FSO on | | 50 | 100 | μA |

3. Guaranteed by design.
4. Cyclic-sense Standby mode VS + VS_OUT consumption:
   I_standby_cs (typ.) = I_VS_standby + I_VSOUT_sleep + I_VS_standby_cs_add
   I_stdby_cs_add (typ.) = 24.5 μA + (28 μA • Tx_TON / Tx_TPER)
5. Cyclic-sense Sleep mode VS + VS_OUT consumption:
   I_sleep_cs (typ.) = I_VS_sleep + I_VSOUT_sleep + I_VS_sleep_cs_add
   I_sleep_cs_add (typ.) = 25.5 μA + (28 μA • Tx_TON / Tx_TPER)

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
(6 V ≤ $V_S$ ≤ 18 V, 6 V ≤ $V_{S\_out}$ ≤ 18 V, −40°C ≤ $T_j$ ≤ 150°C; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VOLTAGE REGULATOR VR1** | | | | | | |
| V_VR1 | Regulator Output Voltage | 0 mA ≤ I(VR1) ≤ 150 mA, 6 V ≤ VS ≤ 28 V, Cload_LIN ≥ 82 pF | 4.9 | 5 | 5.1 | V |
| | | Under EMC exposure (Note 6, 7) Cload_LIN < 82 pF | 4.85 | 5 | 5.15 | V |
| Iout_VR1 | Regulator Output Current | Maximum VR1 load current | | | 150 | mA |
| Ilim_VR1 | Regulator Current Limitation | Maximum VR1 short current | 240 | | 600 | mA |
| Isink_VR1 | Regulator Sink Current | V(VR1) = 5.2 V | 100 | | | μA |
| Vdrop_VR1 | Dropout Voltage | I(VR1) = 60 mA, VS = 5 V | | 0.25 | 0.4 | V |
| | | I(VR1) = 60 mA, VS = 4.5 V | | 0.3 | 0.5 | |
| | | I(VR1) = 30 mA, VS = 4.5 V | | 0.2 | 0.4 | |
| Loadreg_VR1 | Load Regulation | 1 mA ≤ I(VR1) ≤ 30 mA | −30 | | 30 | mV |
| Linereg_VR1 | Line Regulation | I(VR1) ≤ 5 mA | −30 | | 30 | mV |
| Cload_VR1 | VR1 Load Capacitor | ESR < 200 mΩ, ceramic capacitor recommended | 1 | 2.2 | | μF |
| Icmp_VR1_rise | Current Comp. Rising Threshold | VR1 consumption increasing | 0.8 | 2 | 3.1 | mA |
| Icmp_VR1_fall | Current Comp. Falling Threshold | VR1 consumption decreasing | 0.6 | 1.4 | 2.1 | mA |
| Icmp_VR1_hys | Current Comp. Hysteresis | | | 0.5 | | mA |
| Tfilt_VR1_Icmp | Current Comp. Filter Time | | | 16 | | μs |
| Vfail_VR1 | VR1 Fail Threshold | VR1 forced, VR1 decreasing | 1.85 | 2 | 2.25 | V |
| Tfail_VR1 | VR1 Fail Blanking Time | | | 5 | | μs |
| Tshort_VR1 | VR1 Short Blanking Time | VR1 starting-up | 34 | 40 | 46 | ms |
| Ttsd_VR1 | VR1 Deactivation Time after Thermal Shutdown 2 | | 0.85 | 1 | 1.15 | s |
| Toff_VR1 | VR1 Off Time after 8 Watchdog Failures | | 170 | 200 | 230 | ms |
| **VR1 UNDER-VOLTAGE DETECTOR** | | | | | | |
| VR1_RES1 | VR1 Reset Threshold 1 (Default) | SPI VR1_RES.x = 00, VR1 voltage falling | 4.45 | 4.65 | 4.8 | V |
| VR1_RES2 | VR1 Reset Threshold 2 | SPI VR1_RES.x = 01, VR1 voltage falling | 4.2 | 4.4 | 4.6 | V |
| VR1_RES3 | VR1 Reset Threshold 3 | SPI VR1_RES.x = 10, VR1 voltage falling | 3.8 | 4 | 4.2 | V |
| VR1_RES4 | VR1 Reset Threshold 4 | SPI VR1_RES.x = 11, VR1 voltage falling | 3.6 | 3.8 | 4 | V |
| Tdel_VR1_RES | Reaction Delay between VR1 Undervoltage and NRES Low Pulse | | | | 40 | μs |
| Tfilt_VR1_RES | VR1 Undervoltage Filter Time | | | 16 | | μs |

6. Based on characterization, Guaranteed by design.
7. DPI EMC coupled to LIN pin, Clin not used. Tested according to LIN Conformance Test Specification Package for LIN 2.1, October 10th, 2008.

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
($6\ V \le V_S \le 18\ V$, $6\ V \le V_{S\_out} \le 18\ V$, $-40°C \le T_j \le 150°C$; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **HIGH-SIDE OUTPUTS OUT1−3** | | | | | | |
| Ron_OUT1_norm | On-Resistance to VS_OUT, “Normal-ohmic” Configuration | $T_j$ = 25°C, I(OUT1) = −60 mA | | 5 | | Ω |
| | | $T_j$ = 150°C, I(OUT1) = −60 mA | | | 13 | Ω |
| Ron_OUT1_high | On-Resistance to VS_OUT, “High-ohmic” Configuration | $T_j$ = 25°C, I(OUT1) = −6 mA | | 20 | | Ω |
| | | $T_j$ = 150°C, I(OUT1) = −6 mA | | | 52 | Ω |
| Ron_OUT2−3 | On-Resistance to VS_OUT | $T_j$ = 25°C, I(OUT2−3) = −60 mA | | 5 | | Ω |
| | | $T_j$ = 150°C, I(OUT2−3) = −60 mA | | | 13 | Ω |
| Ilim_OUT1_norm | Output Current Limitation to Ground, “Normal-ohmic” Configuration | V(OUT1) = 0 V | −330 | −235 | −140 | mA |
| Ilim_OUT1_high | Output Current Limitation to Ground, “High-ohmic” Configuration | V(OUT1) = 0 V | −82 | −58 | −35 | mA |
| Ilim_OUT2−3 | Output Current Limitation to Ground | V(OUT2−3) = 0 V | −330 | −235 | −140 | mA |
| Iuld_OUT1_norm | OUT1 Underload Threshold, “Normal-ohmic” Configuration | | −6.5 | −3.5 | −0.8 | mA |
| Iuld_OUT1_high | OUT1 Underload Threshold, “High-ohmic” Configuration | | −1.5 | −0.87 | −0.2 | mA |
| Iuld_OUT1−3 | OUT2−3 Underload Threshold | | −6.5 | −3.5 | −0.8 | mA |
| Ileak_OUT1−3 | Output Leakage Current | VS_OUT = 28 V, V(OUT1−3) = 0 V | −3 | | | μA |
| Slew_OUT1−3 | Slew Rate of OUT1−3 | VS_OUT = 13.2 V, 140 mA resistive load | 0.2 | 0.5 | 0.8 | V/μs |
| Tblank_ULD_OUT1−3 | Underload Detection Blanking Delay | OUT1−3 switched on | 65 | 80 | 95 | μs |
| Tfilt_ULD_OUT1−3 | Underload Detection Filter Time | | 50 | 60 | 75 | μs |
| Tfilt_OLD_OUT1−3 | Overload Shutdown Filter Time | | 50 | 60 | 75 | μs |
| **LOW-SIDE RELAY OUTPUTS LS1/2** | | | | | | |
| Ron_LS1/2 | On-Resistance to Ground | $T_j$ = 25°C, I(LS1/2) = 100 mA | | 1.5 | 3 | Ω |
| | | $T_j$ = 125°C, I(LS1/2) = 100 mA (Note 8) | | | 3.7 | Ω |
| Ilim_LS1/2 | Output Current Limitation | LS1/2 = VS_OUT | 250 | 340 | 500 | mA |
| | | LS1/2 = VS_OUT > 18 V | 200 | 290 | 450 | mA |
| Vclamp_LS1/2 | Output Clamp Voltage | I(LS1/2) = 100 mA | 40 | | 50 | V |
| Ileak_LS1/2 | Output Leakage Current | LS1/2 = VS_OUT = 16 V | | | 3 | μA |
| Slew_LS1/2 | Slew Rate of LS1/2 | VS_OUT = 13.2 V, 100 mA resistive load | 0.2 | 2 | 4 | V/μs |
| Tfilt_OLD_LS1/2 | Overload Shutdown Filter Time | | 50 | 60 | 75 | μs |
| **WAKE-UP INPUT WU** | | | | | | |
| Vth_down_WU | Wake-up Negative Edge Threshold Voltage | WU configurable as Source/Sink via SPI | 0.4 | 0.5 | 0.6 | VS_OUT |
| Vth_up_WU | Wake-up Positive Edge Threshold Voltage | | 0.4 | 0.5 | 0.6 | VS_OUT |
| Vhyst_WU | Wake-up Threshold Hysteresis | | 100 | 300 | 500 | mV |
| Ipullup_WU | Pullup Current | 1.5 V < V(WU) < V(VS_OUT − 3 V) | −30 | −20 | −10 | μA |
| Ipulldown_WU | Pulldown Current | 1.5 V < V(WU) < V(VS_OUT − 3 V) | 10 | 20 | 30 | μA |
| Twu_WU | Minimum Time for Wake-up | | 50 | 64 | 85 | μs |

8. Based on characterization, Guaranteed by design.

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
(6 V ≤ $V_S$ ≤ 18 V, 6 V ≤ $V_{S\_out}$ ≤ 18 V, −40°C ≤ $T_j$ ≤ 150°C; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **MODE TRANSITION TIMING** | | | | | | |
| Tdel_powerup | Transition Time from Power-up to Init | VS reaching VS_PORH to VR1 startup | | | 15 | µs |
| Tdel_norm_stdby | Transition Time from Normal/Flash to Standby Mode via SPI | CSN going high to Standby mode entry (Note 9) | | | 10 | µs |
| Tdel_norm_sleep | Transition Time from Normal/Flash to Sleep Mode via SPI | CSN going high to Sleep mode entry (Note 9) | | | 10 | µs |
| Tdel_stdby_norm | Delay of INTN Pulse in Standby after Wakeup | | | | 10 | µs |
| Tdel_sleep_init | Transition from Sleep to Init Mode via Wakeup | | | | 10 | µs |
| **NRES AND INTN SIGNAL TIMING** | | | | | | |
| T_NRES | NRES Low Pulse Duration, e.g. after a Watchdog Failure or VR1 Undervoltage | | 1.7 | 2 | 2.3 | ms |
| T_INTN | INTN Low Pulse Duration after Wake-up Event | | 106 | 125 | 144 | µs |
| **DRIVER TIMING** | | | | | | |
| Tdel_OUT1−3_on | Activation Delay of OUT1−3 Driver (from CSN rising edge) | VS_OUT = 13.2 V; V(OUT1−3) > 0.5·VS_OUT | 12 | | 40 | µs |
| Tdel_OUT1−3_off | De-activation Delay of OUT1−3 Driver (from CSN rising edge) | VS_OUT = 13.2 V; V(OUT1−3) < 0.5·VS_OUT | 20 | | 55 | µs |
| Tdel_LS1/2_on | Activation Delay of LS1/2 Driver (from CSN rising edge) | VS_OUT = 13.2 V; V(LS1/2) < 0.5·VS_OUT | 17 | 42 | 85 | µs |
| Tdel_LS1/2_off | De-activation Delay of LS1/2 Driver (from CSN rising edge) | VS_OUT = 13.2 V; V(LS1/2) > 0.5·VS_OUT | 17 | 32 | 62 | µs |
| **INTERNAL PWM FOR DRIVERS CONTROL** | | | | | | |
| f_PWM_lo | PWM Controller Frequency, Low Setting | FSEL_OUTx/LSx = 0 | 127 | 150 | 173 | Hz |
| f_PWM_hi | PWM Controller Frequency, High Setting | FSEL_OUTx/LSx = 1 | 170 | 200 | 230 | Hz |
| **TIMER1/2 TIMING** | | | | | | |
| Ttim_acc | Timer1/2 Period/On-time Accuracy (see CONTROL_2 register settings) | T1_TPER.[2:0], T1_TON, T2_TPER.[2:0], T2_TON.[1:0] | −15 | | +15 | % |

9. Delays and slopes of LS1/2 drivers not included.

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
(6 V ≤ $V_S$ ≤ 18 V, 6 V ≤ $V_{S\_out}$ ≤ 18 V, −40°C ≤ $T_j$ ≤ 150°C; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SPI TIMING** | | | | | | |
| tCSN_SCLK | First SPI Clock Edge after CSN Active | (Note 10) | 200 | | | ns |
| tCSN_SDO | SDO Output Stable after CSN Active | C(SDO) = 100 pF (Note 10) | | | 150 | ns |
| tCSN_High | Inter-frame Space (CSN Inactive) | All SPI frames stored into internal registers (Note 10) | 6 | | | µs |
| tSCLK_High | Duration of SPI Clock High Level | (Note 10) | 250 | | | ns |
| tSCLK_Low | Duration of SPI Clock Low Level | (Note 10) | 250 | | | ns |
| tSCLK_per | SPI Clock Period | (Note 10) | 1 | | | µs |
| tSDI_set | Setup Time of SDI Input Towards SPI Clock | (Note 10) | 100 | | | ns |
| tSDI_hold | Hold Time of SDI Input Towards SPI Clock | (Note 10) | 100 | | | ns |
| tSCLK_SDO | SDO Output Stable after SPI Clock Falling Edge | C(SDO) = 100 pF (Note 10) | | | 250 | ns |
| t_SPI_exec | SPI Frame Execution Time | Time from CSN rising edge to execution of the frame | | | 25 | µs |

10. Guaranteed by design; not tested in production.

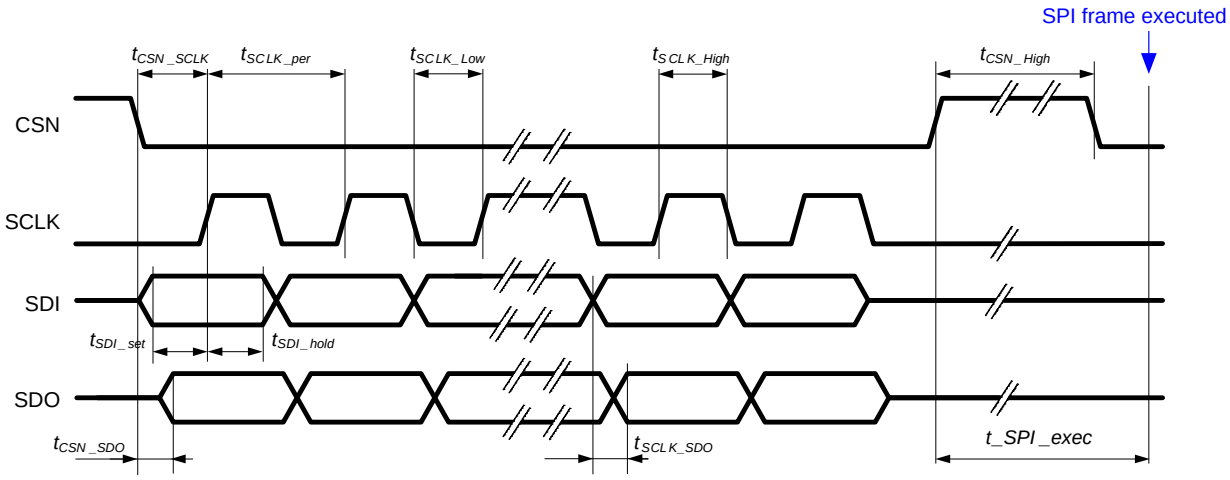



**Figure 3. SPI Timing Parameters**

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
($6\ V \le V_S \le 18\ V$, $6\ V \le V_{S\_out} \le 18\ V$, $-40°C \le T_j \le 150°C$; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **WATCHDOG TIMING** | | | | | | |
| Twd_acc | Watchdog Timing Accuracy | | −15 | | +15 | % |
| T_wd_TO | Timeout Watchdog Period; (watchdog is in the timeout mode after NRES release or in the Stand-by mode) | | 55 | 65 | 75 | ms |
| T_wd_CW | Window Watchdog Closed Window | SPI WD_PER.x = 00 | | 6 | | ms |
| | | SPI WD_PER.x = 01 | | 24 | | |
| | | SPI WD_PER.x = 10 | | 60 | | |
| | | SPI WD_PER.x = 11 | | 120 | | |
| T_wd_OW | Window Watchdog Open Window | SPI WD_PER.x = 00 | | 10 | | ms |
| | | SPI WD_PER.x = 01 | | 40 | | |
| | | SPI WD_PER.x = 10 | | 100 | | |
| | | SPI WD_PER.x = 11 | | 200 | | |
| T_wd_trig | Window Watchdog Trigger Period via SPI (the safe trigger area) | SPI WD_PER.x = 00 | 6.9 | 9.75 | 13.6 | ms |
| | | SPI WD_PER.x = 01 | 27.6 | 39 | 54.1 | |
| | | SPI WD_PER.x = 10 | 69 | 97.5 | 136 | |
| | | SPI WD_PER.x = 11 | 138 | 195 | 272 | |
| T_wd_TO_FLASH | Timeout Watchdog Period in Flash Mode | SPI WD_PER.x = 00 | 13.6 | 16 | 18.4 | ms |
| | | SPI WD_PER.x = 01 | 54.4 | 64 | 73.6 | |
| | | SPI WD_PER.x = 10 | 136 | 160 | 184 | |
| | | SPI WD_PER.x = 11 | 544 | 640 | 736 | |
| T_wd_33_TO | WD_STATUS.1 bit Threshold of Timeout Length (in timeout mode) | Position inside T_wd_TO interval | | 33 | | % |
| T_wd_66_TO | WD_STATUS.0 bit Threshold of Timeout Length (in timeout mode) | Position inside T_wd_TO interval | | 66 | | % |
| T_wd_33_OW | WD_STATUS.1 bit Threshold of Open Window Length (in open window mode) | Position inside T_wd_OW interval | | 33 | | % |
| T_wd_66_OW | WD_STATUS.0 bit Threshold of Open Window Length (in open window mode) | Position inside T_wd_OW interval | | 66 | | % |

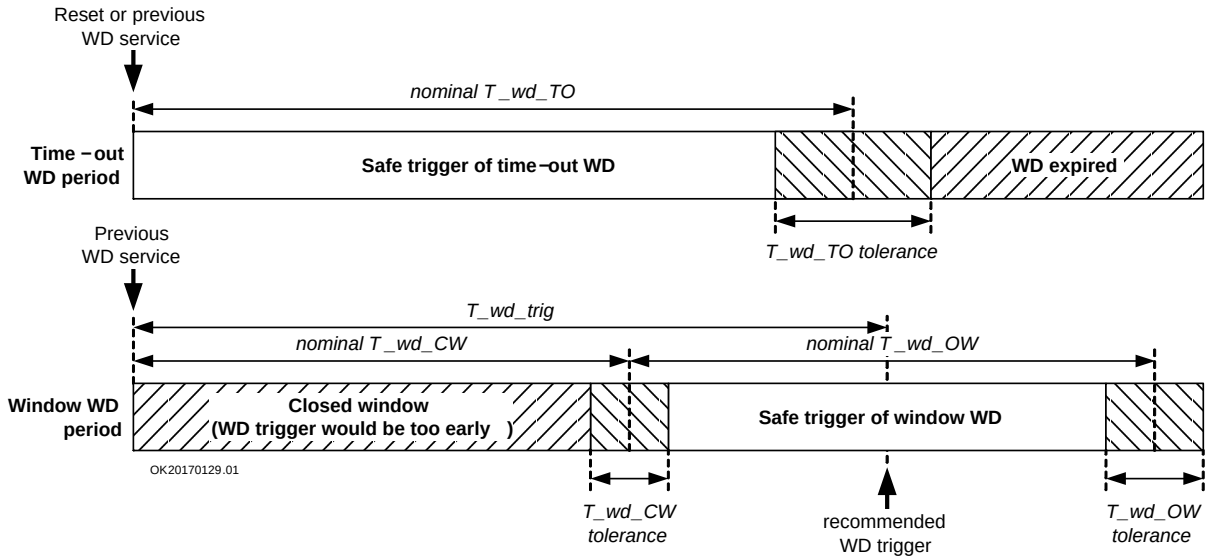



**Figure 4. Watchdog Modes Timing**

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
(6 V ≤ $V_S$ ≤ 18 V, 6 V ≤ $V_{S\_out}$ ≤ 18 V, −40°C ≤ $T_j$ ≤ 150°C; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LIN TRANSMITTER DC CHARACTERISTICS** | | | | | | |
| VLin_dom_LoSup | LIN Dominant Output Voltage | TxDL = low; VS = 7.3 V | | | 1.2 | V |
| VLin_dom_HiSup | LIN Dominant Output Voltage | TxDL = low; VS = 18 V | | | 2 | V |
| VLin_rec | LIN Recessive Output Voltage | TxDL = high;<br>I(LIN) = 0 mA | VS − 1.5 | | VS | V |
| ILIN_lim | Short Circuit Current Limitation | V(LIN) = VS = 18 V | 40 | | 200 | mA |
| Rslave_LIN | Internal Pull-up Resistance | | 20 | 33 | 47 | kΩ |
| **LIN RECEIVER DC CHARACTERISTICS** | | | | | | |
| Vbus_dom_LIN | Bus Voltage for Dominant State | | | | 0.4 | VS |
| Vbus_rec_LIN | Bus Voltage for Recessive State | | 0.6 | | | VS |
| Vrec_dom_LIN | Receiver Threshold | LIN bus recessive → dominant | 0.4 | | 0.5 | VS |
| Vrec_rec_LIN | Receiver Threshold | LIN bus dominant → recessive | 0.5 | | 0.6 | VS |
| Vrec_cnt_LIN | Receiver Center Voltage | (Vrec_dom_LIN + Vrec_rec_LIN) / 2 | 0.475 | | 0.525 | VS |
| Vrec_hys_LIN | Receiver Hysteresis | (Vrec_rec_LIN − Vrec_dom_LIN) | 0.05 | | 0.175 | VS |
| ILIN_off_dom | LIN Output Current,<br>Bus in Dominant State | Normal mode, driver off;<br>VS = 12 V; V(LIN) = 0 V | −1 | | −0.2 | mA |
| ILIN_off_dom_slp | LIN Output Current,<br>Bus in Dominant State | Sleep or Standby mode, driver off;<br>VS = 12 V; V(LIN) = 0 V | −20 | −15 | −2 | μA |
| ILIN_off_rec | LIN Output Current,<br>Bus in Recessive State | Driver off; 8 V < VS < 18 V;<br>8 V < V(LIN) < 18 V; V(LIN) ≥ VS;<br>Guaranteed by design | | | 10 | μA |
| ILIN_no_GND | Communication Not Affected | VS = GND = 12 V;<br>0 < V(LIN) < 18 V | −1 | | 1 | mA |
| ILIN_no_VS | LIN Bus Remains Operational | VS = GND = 0 V;<br>0 < V(LIN) < 18 V | | | 5 | μA |
| **LIN TRANSMITTER DYNAMIC CHARACTERISTICS** | | | | | | |
| D1 | Duty Cycle 1 =<br>tBUS_REC(min) / (2 × TBit) | THREC(max) = 0.744 × VS,<br>THDOM(max) = 0.581 × VS,<br>Tbit = 50 μs,<br>VS = 7 V to 18 V; L1−L3 (Note 11) | 0.396 | | 0.5 | |
| D2 | Duty Cycle 2 =<br>tBUS_REC(max) / (2 × TBit) | THREC(min) = 0.422 × VS,<br>THDOM(mi) = 0.284 × VS,<br>Tbit = 50 μs,<br>VS = 7.6 V to 18 V; L1−L3 (Note 11) | 0.5 | | 0.581 | |
| D3 | Duty Cycle 3 =<br>tBUS_REC(min) / (2 × TBit) | THREC(max) = 0.788 × VS,<br>THDOM(max) = 0.616 × VS,<br>Tbit = 96 μs,<br>VS = 7 V to 18 V; L1−L3 (Note 11) | 0.417 | | 0.5 | |
| D4 | Duty Cycle 4 =<br>tBUS_REC(max) / (2 × TBit) | THREC(min) = 0.389 × VS,<br>THDOM(min) = 0.251 × VS,<br>Tbit = 96 μs<br>VS = 7.6 V to 18 V; L1−L3 (Note 11) | 0.5 | | 0.59 | |

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
(6 V ≤ $V_S$ ≤ 18 V, 6 V ≤ $V_{S\_out}$ ≤ 18 V, −40°C ≤ $T_j$ ≤ 150°C; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LIN TRANSMITTER DYNAMIC CHARACTERISTICS** | | | | | | |
| T_fall_LIN | LIN Falling Edge | VS = 12 V; L1, L2 (Note 11); Normal slope mode | | | 22.5 | µs |
| T_rise_LIN | LIN Rising Edge | VS = 12 V; L1, L2 (Note 11); Normal slope mode | | | 22.5 | µs |
| T_sym_LIN | LIN Slope Symmetry | VS = 12 V; L1, L2 (Note 11); Normal slope mode | −4 | 0 | 4 | µs |
| T_fall_norm_LIN | LIN Falling Edge | VS = 12 V; L3 (Note 11); Normal slope mode | | | 27 | µs |
| T_fall_low_LIN | LIN Falling Edge | VS = 12 V; L3 (Note 11); Low slope mode | | | 62 | µs |
| T_rise_norm_LIN | LIN Rising Edge | VS = 12 V; L3 (Note 11); Normal slope mode | | | 27 | µs |
| T_rise_low_LIN | LIN Rising Edge | VS = 12 V; L3 (Note 11); Low slope mode | | | 62 | µs |
| T_sym_norm_LIN | LIN Slope Symmetry | Normal mode; VS = 12 V; L3 (Note 11) | −5 | 0 | 5 | µs |
| T_TxDL_timeout | TxDL Dominant Time-out Selected by SPI bits TxDL_TO | SPI setting TxDL_TO[1:0]="00" | 27 | 55 | 70 | ms |
| | | SPI setting TxDL_TO[1:0]="01" | 6 | 13 | 20 | |
| | | SPI setting TxDL_TO[1:0]="1X" | | disabled | | |
| C_LIN | Capacitance of the LIN Pin | Guaranteed by design; not tested in production | | 20 | 30 | pF |
| **LIN RECEIVER DYNAMIC CHARACTERISTICS** | | | | | | |
| Trec_prop_down | Propagation Delay of Receiver Falling Edge | C(RxDL) = 20 pF | | | 6 | µs |
| Trec_prop_up | Propagation Delay of Receiver Rising Edge | C(RxDL) = 20 pF | | | 6 | µs |
| Trec_sym | Propagation Delay Symmetry | Trec_prop_down − Trec_prop_up, C(RxDL) = 20 pF | −2 | | 2 | µs |
| T_LIN_wake | Dominant Duration for Wakeup | | 30 | 90 | 150 | µs |

11. The following bus loads are considered: L1 = 1 kΩ/1 nF; L2 = 680 Ω/6.8 nF; L3 = 500 Ω/10 nF.

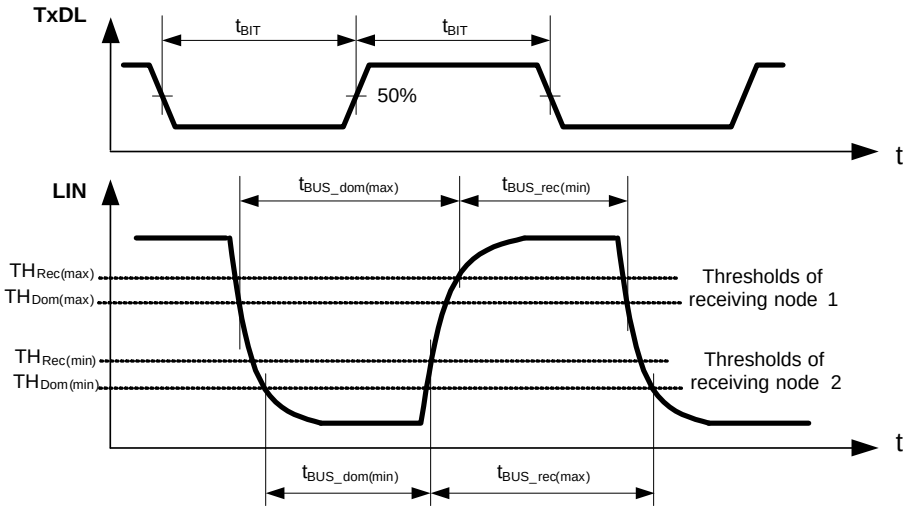



**Figure 5. LIN Dynamic Characteristics − Duty Cycles**

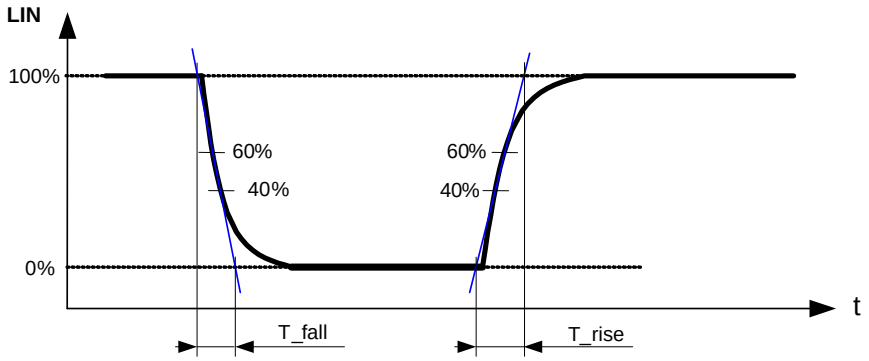



**Figure 6. LIN Dynamic Characteristics − Transmitter Slope**

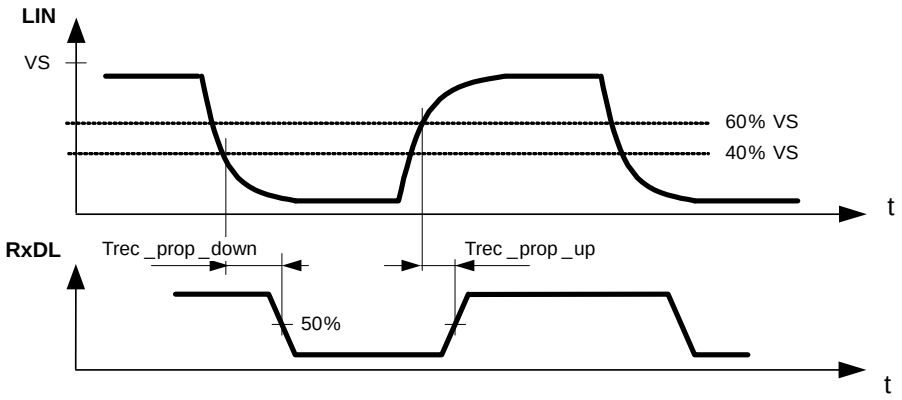



**Figure 7. LIN Dynamic Characteristics − Receiver**

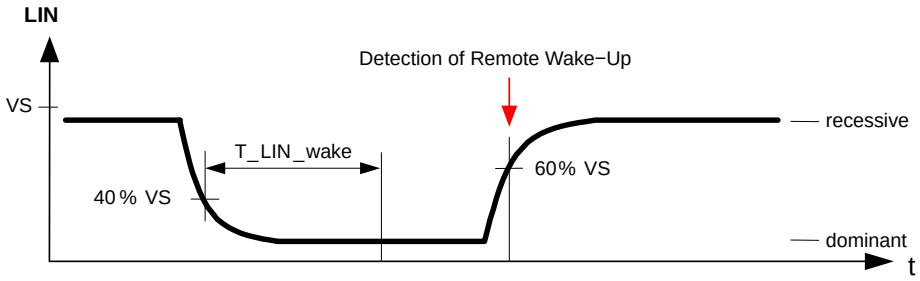



**Figure 8. LIN Wakeup**

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
(6 V ≤ $V_s$ ≤ 18 V, 6 V ≤ $V_{s\_out}$ ≤ 18 V, −40°C ≤ $T_j$ ≤ 150°C; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DIGITAL OUTPUTS RXDL/INTN, SDO** | | | | | | |
| IoutL_pinx | Low-level Output Driving Current | pinx is logical Low, forced V(pinx) = 0.4 V | 2 | 5 | 12 | mA |
| IoutH_pinx | High-level Output Driving Current | pinx is logical High, forced V(pinx) = VR1 − 0.4 V | −12 | −5 | −2 | mA |
| Ileak_HZ_pinx | Leakage in the Tristate, Pin SDO | pinx in the HZ state, forced 0 V < V(pinx) < VR1 | −5 | | 5 | μA |
| **DIGITAL OUTPUT NRES** | | | | | | |
| IoutL_NRES | Low-level Output Driving Current | NRES is active (logical Low), forced V(NRES) = 0.4 V | 2 | 5 | 12 | mA |
| VoutL_NRES | Low-level Output Voltage, Low VR1/VS | VR1 > 2 V, VS < VR1, I(NRES) = 0.1 mA | | | 0.4 | V |
| | | VS > 2 V, I(NRES) = 0.1 mA | | | 0.4 | V |
| Rpullup_NRES | Internal Pull-up Resistor to VR1 | | 55 | 100 | 185 | kΩ |
| **DIGITAL INPUTS SWDM, TXDL, SDI, SCLK, CSN** | | | | | | |
| VinL_pinx | Low-level Input Voltage | | 0 | | 0.8 | V |
| VinH_pinx | High-level Input Voltage | | 2 | | VR1 | V |
| Vin_hys_pinx | Input Voltage Hysteresis | | 100 | | 500 | mV |
| Vin_SWDM | SWDM Pin Threshold Voltage | | 7 | 8.5 | 10 | V |
| Vin_hys_SWDM | SWDM Pin Threshold Hysteresis | | 10 | 200 | 300 | mV |
| Rpullup_pinx | Internal Pull-up Resistor to VR1; Pins TxDL, CSN | | 55 | 100 | 185 | kΩ |
| Rpulldown_pinx | Internal Pull-down Resistor to Ground; Pins SWDM, SDI, SCLK | | 55 | 100 | 185 | kΩ |
| **THERMAL PROTECTION** | | | | | | |
| Tjw | Thermal Warning Level | | 125 | 135 | 145 | °C |
| Tjsd1 | Thermal Shutdown Level 1 | | 135 | 147 | 160 | °C |
| Tjsd2 | Thermal Shutdown Level 2 | | 145 | 159 | 175 | °C |
| Tjsd1−Tjw | Thermal Warning and Thermal Shutdown 1 Level Distance | | 5 | 12 | | °C |
| Tjsd2−Tjsd1 | Thermal Shutdown 1 and Thermal Shutdown 2 Levels Distance | | 5 | 12 | | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## FUNCTIONAL DESCRIPTION

The NCV7429 is a monolithic LIN System-Basis-Chip with enhanced feature set useful in automotive body control systems. Besides the LIN bus interface, the IC features a 5 V voltage regulator, several high-side and low-side switches to control LEDs and relays plus supervision functionality like a window watchdog. This allows a highly integrated solution by replacing external discrete components while maintaining the valuable flexibility. Due to this the board space and ECU weight can be minimized to the lowest level.

### POWER SUPPLY AND REGULATORS

#### VS/VS_OUT – Main Power Supply

VS pin is the main power supply of the device, while VS_OUT supplies OUT1−3 drivers and WU input. In the application, it will be typically connected to the KL30 or KL15 car node. It is necessary to provide an external reverse-polarity protection and filtering capacitor on the VS supply (see Figure 2).

VS/VS_OUT supplies are monitored with respect to the following events:

- VS power-on reset is detected as a crossing of VS_POR level. When VS remains below VS_POR, the device is passive and provides no functionality, the SPI registers are reset to their default values. When VS rises above VS_PORH, the device starts following its state diagram through the power-up state. This event is latched in the SPI bit “COLD_START” so that the application software can detect the VS connection.
- VS_OUT Under-Voltage is detected when VS_OUT falls below VS_*OUT_UV* threshold (typ. 5.5 V). A VS_OUT under-voltage can be encountered, for example, with a discharged car battery or during engine cranking. The high-side and low-side drivers are typically forced off. The exact driver reaction depends on the SPI control settings – see par. “VS_OUT Over- and Under-Voltage”. Under-voltage events are flagged through SPI bit “VS_OUT_UV”.
- VS_OUT Over-Voltage is detected when VS_OUT rises over *VS_OUT_OV* threshold (typ. 21 V). Similarly to the under-voltage, the high-side and low-side drivers are de-activated based on the SPI settings and the event is flagged through SPI bit “VS_OUT_OV”.

#### GND1, GND2 – Ground Connections

The device ground connection is split to two pins – GND1 and GND2. Both pins have to be connected on the application PCB.

#### Regulator VR1

VR1 is a low-drop output regulator providing 5 V voltage derived from the VS main supply. It is able to deliver up to 150 mA and is primarily intended to supply the application microcontroller unit (MCU) and related 5 V loads (e.g. its own MCU-related digital inputs/outputs). An external capacitor needs to be connected on VR1 pin in order to ensure the regulator’s stability and to filter the disturbances caused by the connected loads. Ceramic X7R 2.2 μF capacitor is recommended.

VR1 voltage is supplying all digital low-voltage input/output pins.

The protection and monitoring of the VR1 regulator consist of the following features:

- VR1 Current Limitation – the current protection ensures fast enough charging of the external capacitor at start-up while protecting the regulator in case of shorts to ground
- Junction Temperature Monitor – the junction temperature is monitored and when it rises above the second shutdown level, the VR1 regulator is de-activated and the device is forced to the Fail-safe mode in order to protect the regulators and the full application. For details, see par. “Thermal Protection”.
- VR1 Failure Comparator – during the VR1 start-up and operation, the VR1 voltage is continuously compared with *Vfail_VR1* level (typ. 2 V). During startup, if VR1 does not rise above *Vfail_VR1* level within *Tshort_VR1* (typ. 40 ms), it’s considered shorted to ground and the device is forced to the Fail-safe mode (see Figure 10). During the VR1 operation, any dip below *Vfail_VR1* level longer than *Tfail_VR1* (typ. 5 μs) is considered as a failure – temporary excursions of VR1 under the failure threshold can be caused, for example, by EMC, and can lead to memory data inconsistencies inside the MCU. Both the failure during VR1 startup and the operation are latched in the “VR1_FAIL” SPI bit for subsequent software diagnostics.
- VR1 Reset Comparator – the VR1 regulator output is compared with a reset level *VR1_RES* (programmable to typ. 74%, 79%, 87% and 91% of the nominal VR1 voltage). If the VR1 level drops below this level for longer than *Tfilt_VR1_RES* (typ. 16 μs), a reset towards the MCU is generated through the NRES pin and all outputs (OUT1−3, LS1/2) are switched off and all the control registers are set to their defaults, except “FSO_DIS” bit setting (see Figure 11).
- VR1 Consumption Monitor (Icmp) – to ensure a safe transition into the Standby mode, where VR1 remains active while the watchdog is off, the VR1 current consumption is monitored. The watchdog is really disabled in the Standby mode only when the VR1 consumption falls below *Icmp_VR1_fall* (typ. 1.1 mA). An increase of the VR1 consumption above the *Icmp_VR1_rise* level activates the watchdog again.

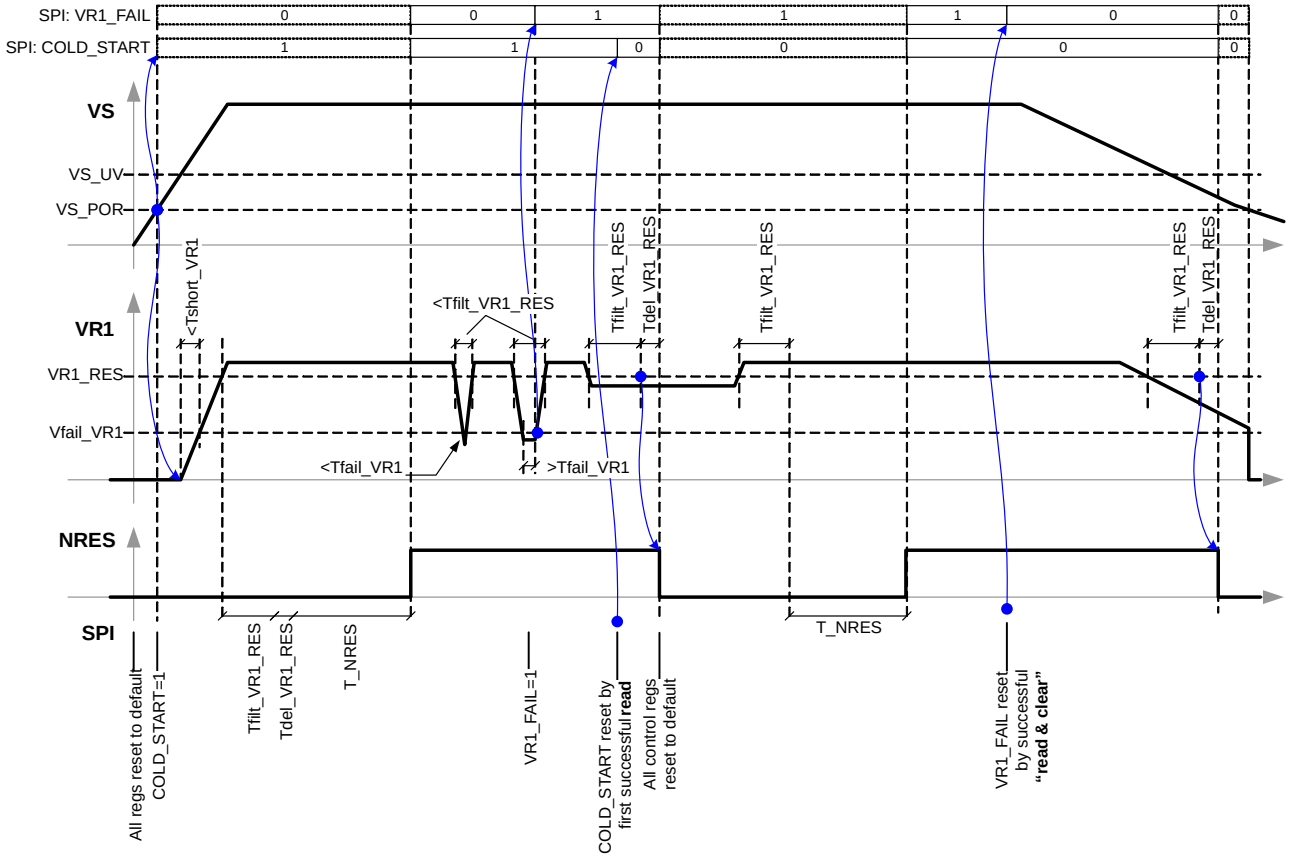



**Figure 9. VR1 Monitoring**

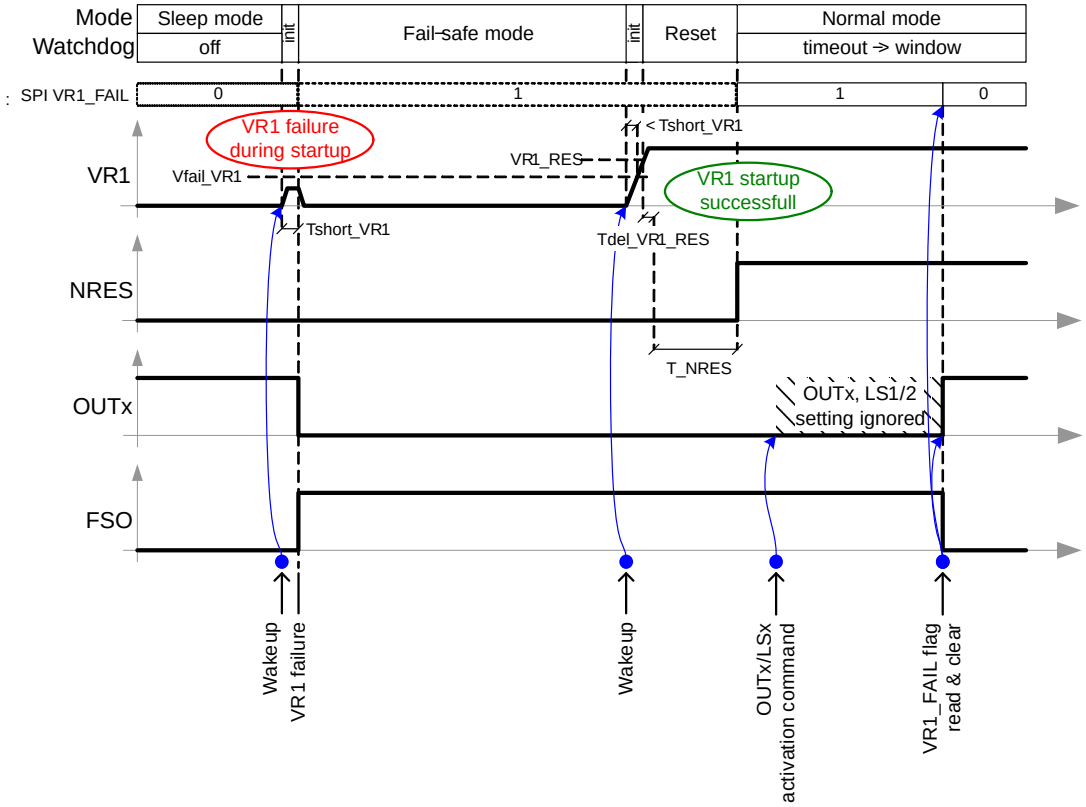



**Figure 10. VR1 Monitoring − VR1 Failure during Startup**

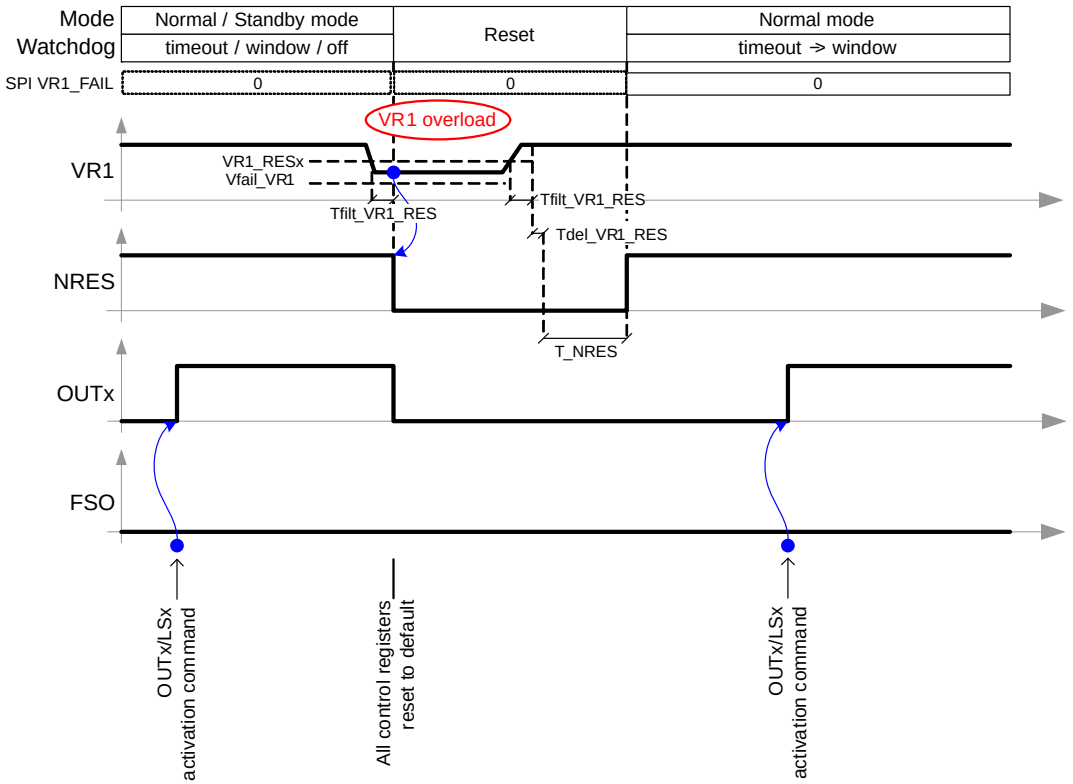



**Figure 11. VR1 Monitoring − VR1 Undervoltage**

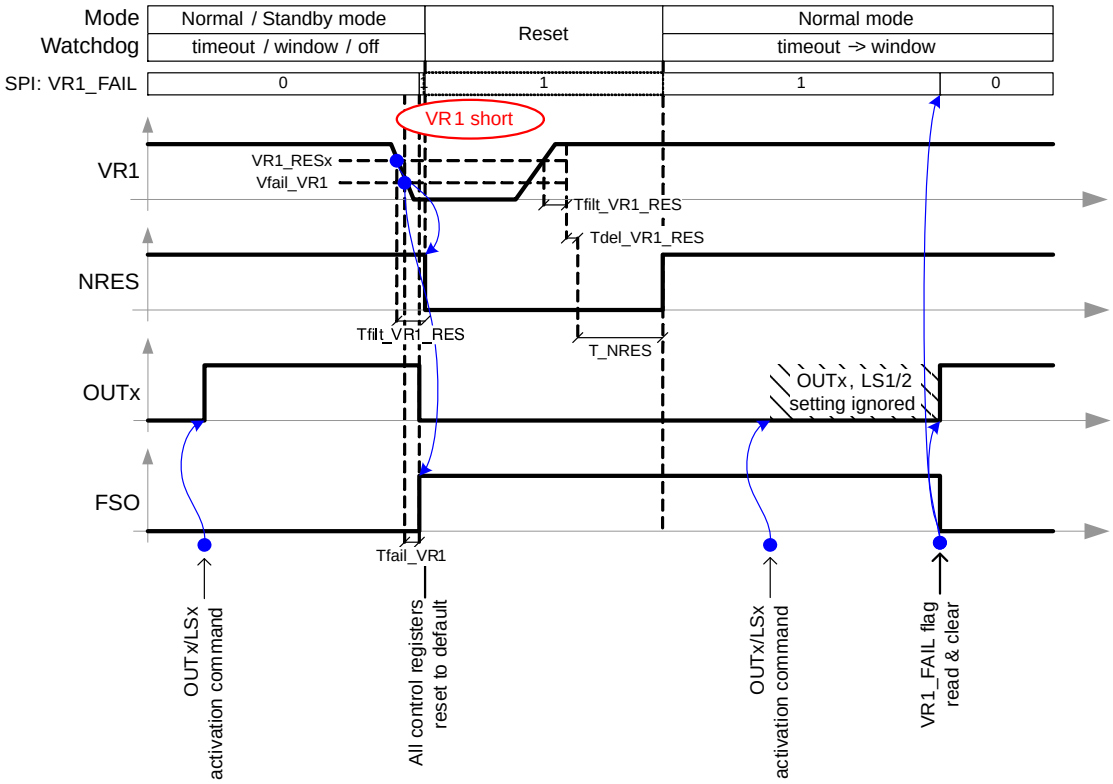



**Figure 12. VR1 Monitoring − VR1 Short in Normal/Standby Mode**

## COMMUNICATION TRANSCEIVER

### LIN Transceiver

The NCV7429 on-chip LIN transceiver is an interface between a physical LIN bus and the LIN protocol controller. It is compatible to LIN2.x and J2602 specifications.

The LIN is supplied solely from the VS pin and its state control is as follows:

- In the Normal mode of the device, LIN transceiver transmits dominant or recessive symbols on the LIN bus based on the logical level on TxDL pin. The signal received from the bus is indicated on RxDL pin. Both logical pins are referred to the VR1 supply. A resistive pull-up path of typ. 30 kΩ is internally connected between LIN and VS.
- In the Standby and Sleep mode of the device, the LIN transceiver is in its wakeup detection state. Logical level on TxDL is ignored and pin RxDL is kept high until it's used as an interrupt request signal. A LIN bus wakeup corresponds to a dominant symbol at least *T_LIN_wake* long (typ. 90 μs) followed by a rising edge (i.e. transition to recessive) – see Figure 8. In this way, false wakeups due to permanent LIN dominant failures are avoided. Only a pull-up current of typ. 15 μA is connected between VS and LIN instead of the 30 kΩ pull-up path. The LIN wakeup detection is by default active in the Standby and Sleep modes and can be disabled via SPI control registers.

The LIN transceiver features SPI-configurable **TxDL dominant time-out timer**. This circuit, if enabled, prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxDL is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxDL. If the duration of the low-level on pin TxDL exceeds the internal timer value *T_TxDL_timeout*, the transmitter is disabled, driving the bus into a recessive state and the event is latched in the SPI status bit "TO_TxDL". The transmission is de-blocked when "TO_TxDL" bit is reset by the corresponding register "read and clear" and TxDL pin returns to high (recessive) state.

The LIN transceiver provides two LIN slope control modes, configured by SPI bit "LIN_SLOPE".

In **normal slope mode** the transceiver can transmit and receive data via LIN bus with speed up to 20 kBaud according LIN2.x specification. This mode is used by default.

In **low slope mode** the slew rate of the signal on the LIN bus is reduced (rising and falling edges of the LIN bus signal are longer). This further reduces the EMC emission. As a consequence the maximum speed on the LIN bus is reduced up to 10 kBaud. This mode is suited for applications where the communication speed is not critical. The low slope mode can be configured by setting SPI bit "LIN_SLOPE".

## HIGH- AND LOW-SIDE DRIVERS

### High-Side Drivers OUT1−3

High-side drivers OUT1−OUT3 are designed to supply mainly LED's or switches (for cyclic monitoring). When switched on, they connect the corresponding pin to the VS_OUT supply. Driver OUT1 can be configured to have two distinct levels of on-resistance; typically 5 Ω in "normal-ohmic" configuration (default) and typically 20 Ω in "high-ohmic" configuration. Drivers OUT2−3 have a typical on-resistance of 5 Ω.

At the VS power-up or wakeup from the Sleep mode, all OUT1−3 drivers are off. Immediately after the device enters the Normal mode, they can be set to one of the following states via the corresponding SPI bits:

- Driver is off in all modes (default)
- Driver is on in all modes, except Fail-safe mode
- Driver is activated periodically in all modes, except Fail-safe mode. The periodicity is driven either by Timer 1 (period from 0.5 sec to 4 sec, on time 10 ms or 20 ms) or Timer 2 (period from 10 ms to 200 ms, on time 100 μs, 200 μs, 1 ms or 5 ms). Periodical activation can be used, for example, for LED flashing or cyclic contact monitoring.
- Driver is controlled by the on-chip PWM controller in all modes, except Fail-safe mode. Each OUTx driver has a dedicated 7-bit PWM duty cycle and the base frequency selectable through individual SPI settings.

The SPI settings for the drivers are applied immediately after the SPI frame is successfully completed (CSN rising edge) as long as FSO is not active. This can be done even immediately after the device initialization before the first watchdog service.

All OUTx outputs are protected by the following features:

- Over-current protection and current limitation: if the driver current exceeds the over-current limit for longer than *Tfilt_OLD_OUTx* (typ. 60 μs), the event is latched into the SPI status bits and the driver is disabled. It will be again enabled only when the corresponding SPI flag is read and cleared. The over-current event in the Standby or Sleep mode causes the interrupt in case SPI bit "WU_OC" is set.
- Under-load detection: during the on-time of the driver, a too low current indicates missing load. The under-load event is latched into the corresponding SPI status bits; however, the driver is not disabled and remains controlled according the SPI bits.
- Thermal protection and VS_OUT under/over-voltage protection: through monitoring of the junction temperature and the VS_OUT supply voltage; all loads are protected as described in par. "Protection". If SPI bit "WU_TSD" resp. "WU_OVUV" is set, the thermal shutdown 1 event resp. VS_OUT over-/under-voltage in the Standby or Sleep mode causes the interrupt.

OUT3 output is also intended for failure indication. By default, OUT3 switch is not controlled by the SPI settings but by the internal FSO signal – see section “Fail-Safe (FSO) Signal”. Only when the FSO signal is disconnected from OUT3 by setting SPI bit “FSO_DIS”, OUT3 acts identically to OUT1 and OUT2.

### Low-Side Drivers LS1/2

NCV7429 offers two low-side drivers LS1 and LS2 primarily intended to drive relays, typically:

- R = 160 Ω ± 10%, L = 240/300 mH
- R = 220 Ω ± 10%, L = 330/420 mH

For the relay demagnetization, LS1/2 drivers feature active flyback clamps towards ground (no diode to VS_OUT) allowing to keep the load off even under load-dump condition on VS_OUT. Alternatively, LS1/2 can drive LED’s.

LS1/2 can be configured in one of the following states:

- Off in all modes (default)
- On in the Normal mode; off in all other modes
- Controlled by individual PWM in the Normal mode; off in all other modes. If a relay is connected to the output, this setting should not be used.

LS1/2 outputs are protected by the following features:

- Over-current protection and current limitation: if the driver current exceeds the over-current limit for longer than *Tfilt_OLD_LS1/2* (typ. 60 μs), the event is latched into the SPI status bits and the driver is disabled. It will be again enabled only when the corresponding SPI flag is read and cleared.
- Thermal protection and VS_OUT under/over-voltage protection: through monitoring of the junction temperature and the VS_OUT supply voltage; all loads are protected as described in par. “Protection”.

## WAKEUP INPUT WU

NCV7429 offers an independent contact-monitoring input WU which can be used either for Normal-mode contact polling or for contact change detection during the Standby and Sleep modes. In any mode, the WU input can be configured into one of the following modes of operation:

- Static sense: the WU input is constantly monitored by an input comparator and a filter of typ. 64 μs. In the Normal mode, the result of the comparison (the input high/low state) can be polled any time through the SPI status bits. In the Standby and Sleep modes, a change of the WU polarity (in any direction) is recognized as a wakeup event. The MCU can then recognize the exact WU wakeup source by reading “WU_WU” SPI status bits.
- Cyclic sense: the WU state detection is performed periodically as fostered by one of the internal timers: Timer 1 (period from 0.5 sec to 4 sec) or Timer 2 (period from 10 ms to 200 ms). WU is left to settle during the on-time and the state detection is started 20 μs before the on-time end through a filter of typ. 16 μs. The result of the periodical state detection is latched into the SPI status register and is not updated until the next period of the selected timer. A wakeup is detected in case sample of the WU state changes in any direction.

Additionally, the WU input can be internally pre-biased through individual control bits by a pull-down (WU_PUD=0) or pull-up (WU_PUD=1) current source. The pre-bias is disabled in Standby or Sleep mode if WU wakeup is disabled (WU_DIS=1).

In case cyclic sense is used, the WU timer settings must be correctly chosen together with the high-side output settings. The driver physically ensuring the periodical contact supply must be set for the same timer as the contact monitor by the MCU software.

## OPERATING MODES

NCV7429 can be configured to different operating modes in function of the application needs and the external conditions. The device resources can be enabled/disabled and the overall power consumption can be adapted to the electronic module state – ranging from full power mode down to a very low quiescent current “sleep” mode. The principal operating modes of NCV7429 are shown in Figure 13.

### Un-Powered and Init Modes

As long as VS remains below the *VS_POR* level (typ. 3.45 V), the device is held in power-up reset. All outputs except NRES are in HiZ state, the linear regulator output is off.

As soon as the VS main supply exceeds the power-on reset level, the device enters an initialization sequence represented by a transient “init” mode. All SPI registers are set to their default values, “COLD_START” SPI bit is set high for subsequent diagnostics and the VR1 regulator is started. After a successful start of the VR1 regulator (i.e. VR1 exceeds the *Vfail_VR1* level in less than *Tshort_VR1* – typ. 40 ms), NRES is still kept low until VR1 reaches its reset level. After another 2 ms (parameter *T_NRES*), NRES is released to high and the device enters Normal mode with timeout watchdog.

In case VR1 does not start within *Tshort_VR1*, it’s again disabled, SPI “VR1_FAIL” bit is set and the device enters Fail-safe mode. The Fail-safe mode can be exited via any valid wakeup event or by VS re-connection. The initialization sequence is shown in Figure 12.

During Init phase, the SWDM input is sampled. In case SWDM is High, the Software Development mode is entered and watchdog is disabled in all modes until the following Init mode. SWDM pin can be sampled upon SPI request as well.

### Normal Mode

In this mode the device provides full functionality, all resources are available. The voltage regulator VR1 is able to source 150 mA. MCU can enable/disable the device features via SPI as well as monitor the status of the device.

VR1 level is monitored through reset and failure comparators – see Figure 12. When the Normal mode is entered, the watchdog is started in a timeout mode; a window watchdog mode is applied after the first correct watchdog service. The watchdog has to be correctly triggered; otherwise a watchdog failure is detected resulting in reset signal to the MCU. Afterwards, the watchdog is re-started in the timeout mode. After eight consecutive watchdog failures, the VR1 regulator is disabled for 200 ms and re-started again. If the watchdog service still fails seven more times, the device is put into Fail-safe mode. The Fail-safe mode can then be exited either via a wakeup or VS re-connection.

Through SPI bits “MODE[1:0]”, the MCU can either keep the device in the Normal mode, or request transition into one of the low-power modes – Standby or Sleep.

### Standby Mode

Standby mode is the first low-power mode. The voltage regulator VR1 remains active while the watchdog is disabled. The Standby mode is mainly intended to keep the application powered (e.g. for RAM content preservation) while the MCU is in a halt-state (software not running).

In order to make a safe transition into the Standby mode, the watchdog will remain enabled even in the Standby mode until the consumption from VR1 decreases below *Icmp_VR1_fall* level (typ. 1.1 mA). When the VR1 consumption increases back above *Icmp_VR1_rise* level (typ. 1.7 mA), the device will perform a wakeup from the Standby mode to ensure supervision of the MCU software. The current supervision of VR1 can be disabled via SPI by setting the bit “ICMP_STBY”.

During the Standby mode, several types of wakeup events can be signaled to the MCU through INTN pin: timer1 or timer2 expiration, wakeup on LIN bus, change on WU pin or SPI activity. SPI activity wakeup is not signaled through INTN pin. The watchdog is started in timeout mode and MCU can request a mode transition afterwards. VR1 also continues to be monitored by the reset circuit, which will generate a low NRES pulse in case the regulator output drops below the reset level.

### Sleep Mode

Sleep mode is the mode with the lowest consumption. VR1 regulator and the watchdog are inactive. The device maintains minimum operation allowing reception of wake-up events generated by WU input, LIN bus line, or driven by timer1 or timer2. In case of a wake-up event, the device switches from the Sleep mode to the Normal mode (through the Init mode, as the VR1 must be started similarly to the VS power-up). SPI bit WD_TRIG is set to 0 after a wakeup.

### Fail-Safe Mode

Fail-safe mode is the mode equals to the Sleep mode, but all peripherals (VR1, OUT1−3, LS1/2) and the watchdog are inactive.

The Fail-safe mode is entered after following failure conditions:

- VR1 did not reach *Vfail_VR1 level* (typ. 2 V) within *Tshort_VR1* during startup (VS connection or wakeup from Sleep mode)
- Fifteen consecutive watchdog failures occur
- The device junction temperature exceeded thermal shutdown level *Tjsd2* (typ. 155°C) for eight times within one minute

Wakeup from Fail-safe mode is indicated by SPI flag “FAIL-SAFE”.

### Flash Mode

Flash mode is identical to the Normal mode with the exception of the watchdog which operates in timeout mode. The purpose of the Flash mode is to enable transfer of bigger bulk of data between the MCU and a programming interface – typically in the field. The Flash mode is entered by setting dedicated SPI bit FLASH_RDY in CONTROL_2 register followed by “MODE[1:0]” = 11b request.

### Software Development Mode

Software Development mode is identical to the Normal mode with the exception of the watchdog which is disabled. The purpose of the Software Development mode is to enable software debugging without watchdog interaction or transfer of bigger bulk of data between the MCU and a programming interface – typically during the module-level production.

The Software Development mode will be entered if the voltage applied on SWDM pin exceeds the corresponding comparison level *Vin_SWDM* in the Init phase or is SWDM sampling is requested by “SWDM_SAMP” SPI bit. Sampled SWDM state is latched in read-only “SWDM” SPI bit. As SWDM pin is high-voltage tolerant, it might be tied to the VS line through a protection resistor.

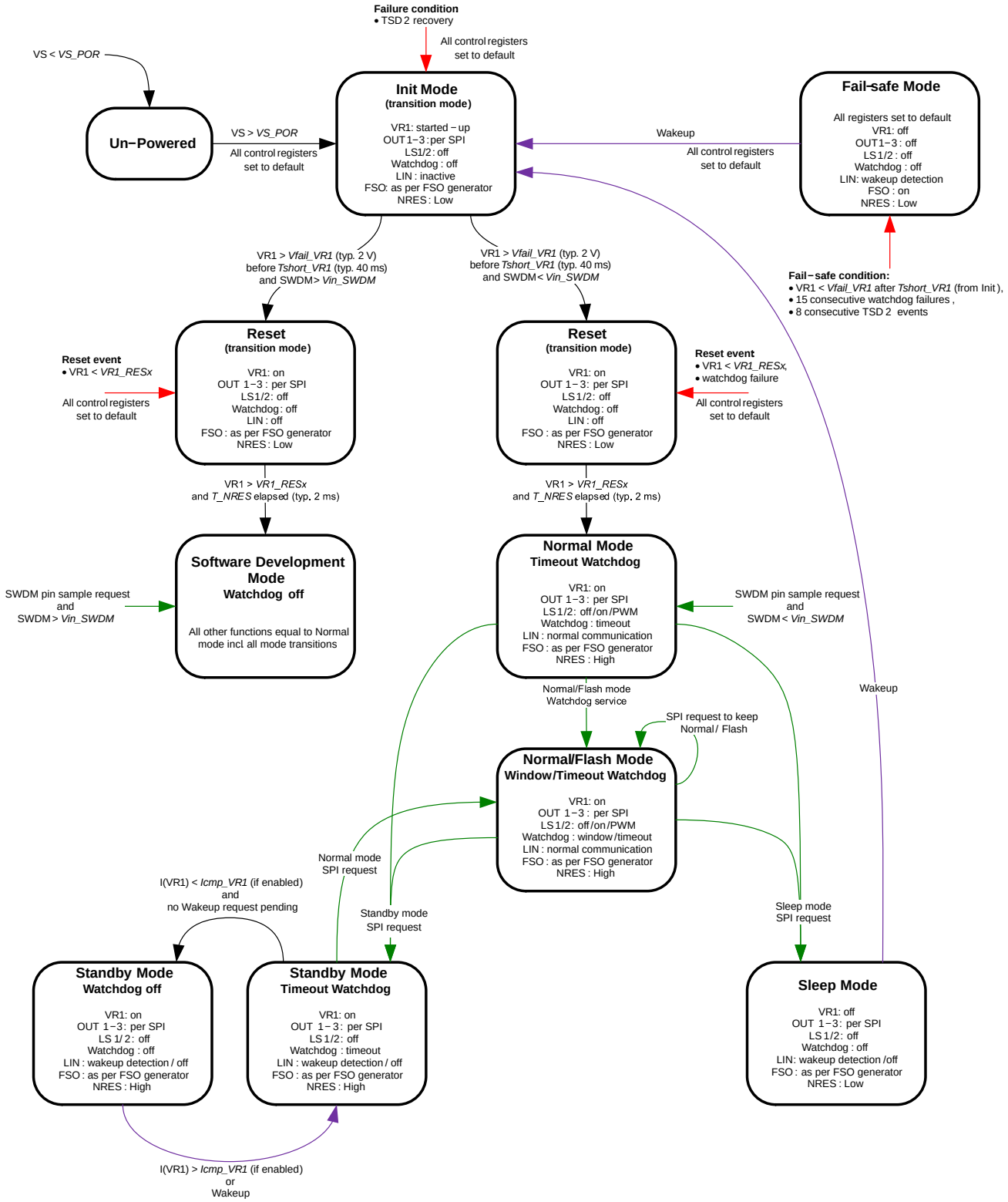



**Figure 13. Principal Operating Modes**

## WAKE-UP EVENTS

In the Standby and Sleep modes, NCV7429 can detect several types of wake-up events summarized in Table 6:

- In the Sleep mode, a wakeup will cause initialization of VR1 regulator and transition to a Reset mode. After the release of the NRES signal, the timeout watchdog will be started and the device enters the Normal mode – i.e. the SPI settings for outputs will be applied immediately. The following events will cause wakeup from the Sleep mode:
  - Bus wakeup through LIN – can be enabled/disabled through SPI.
  - Switch monitoring on WU input – can be configured and enabled/disabled through SPI.
  - Timer wakeup – timer1 and timer2 can be configured to cause a wakeup after a fixed time period – the selected timer is started at the moment the Sleep mode is requested and causes wakeup immediately when the selected time period expires. The timer wakeup can be configured and enabled/disabled by SPI.
  - Thermal shutdown 1 – enabled if “WU_TSD” is set.
  - OUT1−3 overcurrent – enabled if “WU_OC” is set.
  - VS_OUT over-/under-voltage – enabled if “WU_OVUV” is set.
- From the Standby mode, where VR1 remains active, a wakeup event will cause watchdog startup in timeout mode:
  - SPI wakeup (CSN low and rising edge on SCLK). Interrupt request is not generated.
  - VR1 consumption wakeup (VR1 consumption exceeds the *Icmp_VR1_rise* level; can be disabled by SPI control). Interrupt request is generated. If VR1 consumption falls below the *Icmp_VR1_fall* level within the timeout period, the watchdog is disabled again.
  - Bus wakeup through LIN, switch monitoring on WU, timer wakeups, thermal shutdown 1, OUT1−3 overcurrent and VS_OUT over-/under-voltage have the same meaning as in the Sleep mode. Any of them will cause an interrupt request, if enabled.

Every valid wakeup event starts the timeout watchdog, which then must be correctly triggered. If another wakeup event occurs during the initial timeout watchdog, the watchdog is not re-started and another interrupt request (pulse on INTN pin) is generated only if the corresponding wakeup flag is located in different status register. E.g., LIN wakeup will start the watchdog timeout timer while the device remains in the Standby mode. If, for example, a WU pin wakeup is then detected, it will be latched into the SPI registers, but no new interrupt will be generated and the watchdog will keep running. If VS_OUT overvoltage is detected afterwards, new interrupt will be generated. This example is shown in Figure 14 and Figure 15.

In all wakeup cases in the Standby mode, the device remains in the Standby mode with watchdog running until it is changed. SPI settings for drivers are applied after the correct watchdog service.

In case LIN, WU pin and Timer1/2 wakeup sources are disabled while the Standby or Sleep mode is entered through a SPI request, LIN and WU wakeup is automatically enabled (SPI bits “WU_LIN_DIS” and “WU_DIS” are ignored).

SPI wakeup flags have to be cleared before transition to the Standby or Sleep mode is requested, otherwise immediate wakeup occurs.

**Table 6. WAKEUP EVENTS**

| Device Mode | Wakeup Event | SPI Default | SPI Control | SPI Flag | NRES Pulse | INTN Pulse |
|---|---|---|---|---|---|---|
| **Standby** | SPI | N/A | Cannot be Disabled | N/A | No | No |
| | I(VR1) > Icmp | Enabled | ICMP_STBY | N/A | | Yes |
| | Bus Wakeup (LIN) | Enabled | WU_LIN_DIS | STATUS_0.WU_LIN | | |
| | WU Change | Enabled | WU_DIS | STATUS_0.WU_WU | | |
| | Timer1/2 Wakeup | Disabled | WU_TIM_EN[1:0] | STATUS_0.WU_TIM | | |
| | TSD1 | Disabled | WU_TSD | STATUS_1.TSD1 | | |
| | VS_OUT OV/UV | Disabled | WU_OVUV | STATUS_1.VS_OUT_OV, STATUS_1.VS_OUT_UV | | |
| | OUT1−3 Overcurrent | Disabled | WU_OC | STATUS_2.OUTx_OC | | |
| **Sleep** | Bus Wakeup (LIN) | Enabled | WU_LIN_DIS | STATUS_0.WU_LIN | Yes | No |
| | WU Change | Enabled | WU_DIS | STATUS_0.WU_WU | | |
| | Timer1/2 Wakeup | Disabled | WU_TIM_EN[1:0] | STATUS_0.WU_TIM | | |
| | TSD1 | Disabled | WU_TSD | STATUS_1.TSD1 | | |
| | VS_OUT OV/UV | Disabled | WU_OVUV | STATUS_1.VS_OUT_OV, STATUS_1.VS_OUT_UV | | |
| | OUT1−3 Overcurrent | Disabled | WU_OC | STATUS_2.OUTx_OC | | |
| **Fail-safe** | Bus Wakeup (LIN) | Enabled | Cannot be Disabled (settings ignored) | STATUS_0.WU_LIN | Yes | No |
| | WU Change | Enabled | | STATUS_0.WU_WU | | |
| | Timer1/2 Wakeup | Disabled | WU_TIM_EN[1:0] | STATUS_0.WU_TIM | | |

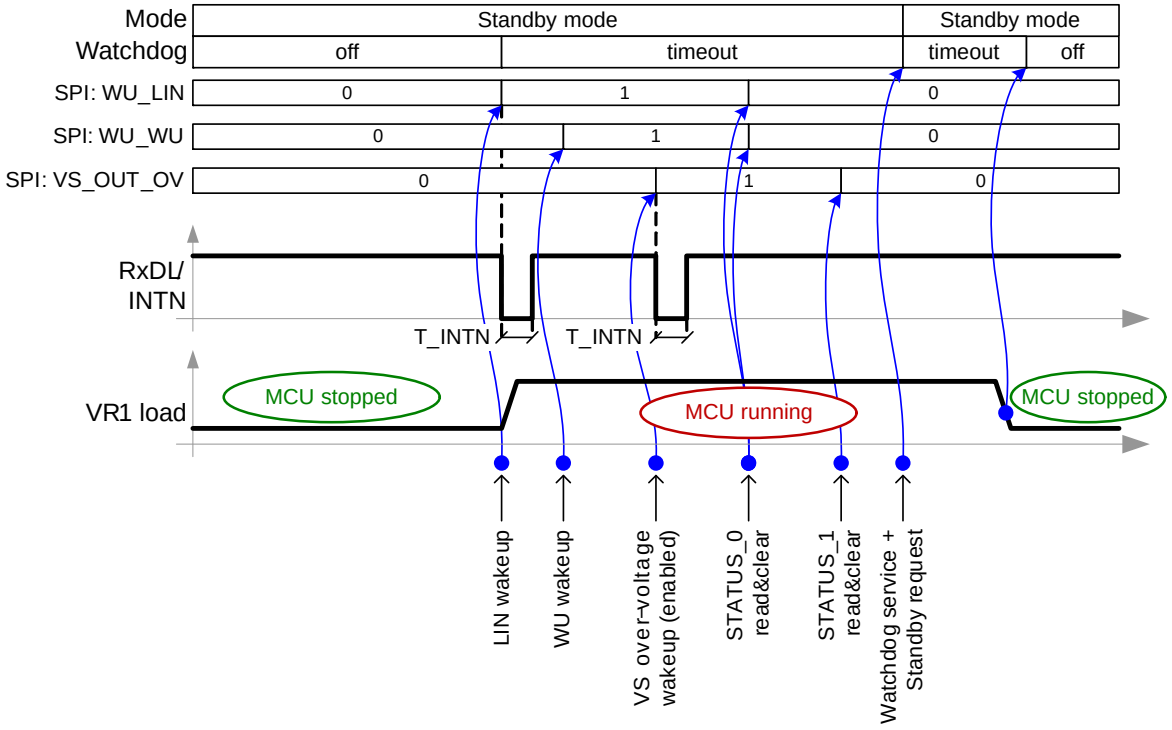



**Figure 14. Interrupt Generation, VR1 Current Comparator Enabled**

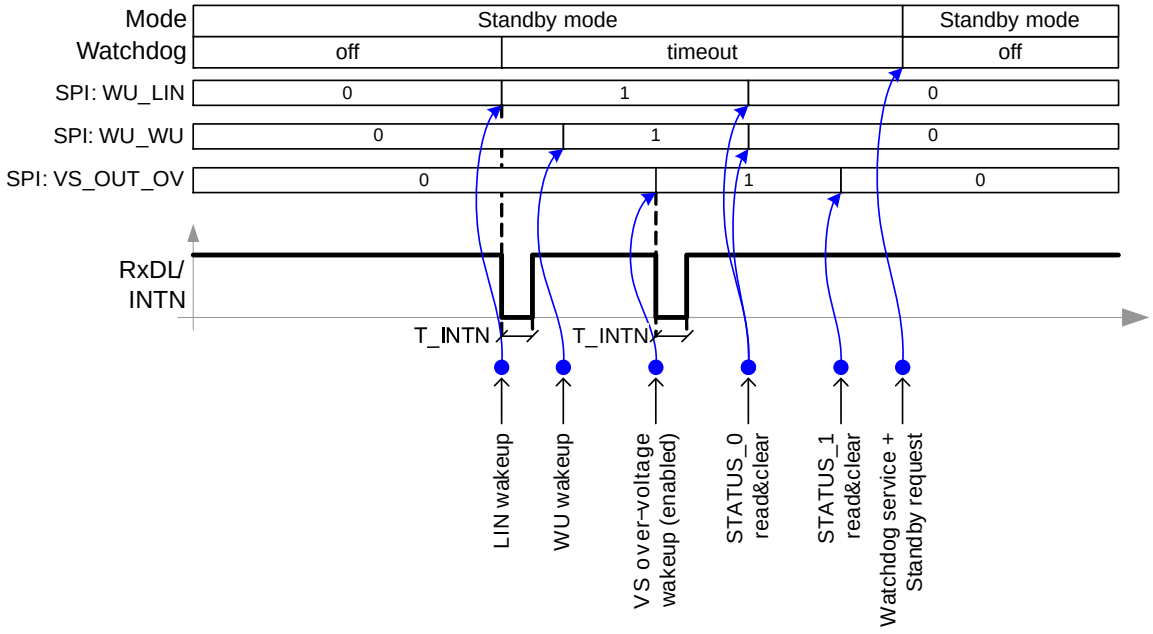



**Figure 15. Interrupt Generation, VR1 Current Comparator Disabled**

## WATCHDOG

The on-chip watchdog requires that the MCU software sends specific SPI messages (watchdog “triggers” or “services”) in a specified time frame. A correct watchdog trigger/service consists of a write access to SPI register CONTROL_0 with “WD_TRIG” bit inverted compared to its previous state. The watchdog timer re-starts immediately after a successful trigger is received.

A read access to the CONTROL_0 register or a write access with “WD_TRIG” bit unchanged does not trigger the watchdog. The moment of the watchdog trigger corresponds to the rising edge of the CSN signal (end of the SPI frame).

The watchdog can work in the following modes (see Figure 4 and Figure 16):

- Off; the watchdog is always off in the Sleep and Software development modes. It is also off in the Standby mode, provided that the VR1 consumption stays below the *Icmp_VR1_rise* limit, or when the Icmp comparator is disabled.
- Timeout: the watchdog works as a timeout timer. The MCU software must serve the watchdog any time before the time-out expiration. Timeout watchdog is started after reset events (power-up, watchdog failure, VR1 under-voltage, thermal shutdown 2), by any wakeup event from both Standby and Sleep mode and in Flash mode. After NRES event, the timeout is typ. 65 ms, while in the Flash mode the timeout may be selected via SPI. The timeout watchdog is started regardless if the wakeup is or is not accompanied by a reset. Watchdog counter position is reflected in SPI status bits “WD_STATUS[1:0]”.
- Window: the watchdog time is split to two distinct parts – a closed window, where the watchdog may not be triggered, is followed by an open window where the MCU must send a valid watchdog trigger. Window watchdog is used during the Normal operating mode of the device after the initial timeout watchdog is correctly triggered. Position of the watchdog counter inside the open window is reflected in SPI status bits “WD_STATUS[1:0]”.
- Failure: If the watchdog is not triggered correctly (trigger not sent during timeout or open window; or sent during the closed window), reset is generated on pin NRES and the “WD_TRIG” bit is reset to ”0”. After the NRES release, the watchdog always starts in the timeout mode. Watchdog failures are counted and their number can be read from the SPI status registers (bits “WD_CNT[3:0]”). After eight watchdog failures in sequence, the VR1 regulator is switched off for 200 ms. In case of seven more watchdog failures, VR1 is completely turned off and the device goes into Fail-safe mode until a wake-up occurs (e.g. via the LIN bus). Second successful watchdog trigger (first in window mode) resets the failure counter. Watchdog failure handling is shown in Figure 17 and Figure 18.

The watchdog time for window mode is selectable from four different values by SPI bits “WD_PER[1:0]”. The watchdog time setting is applied only if it’s contained in an SPI frame representing a correct watchdog trigger message. The setting is ignored otherwise.

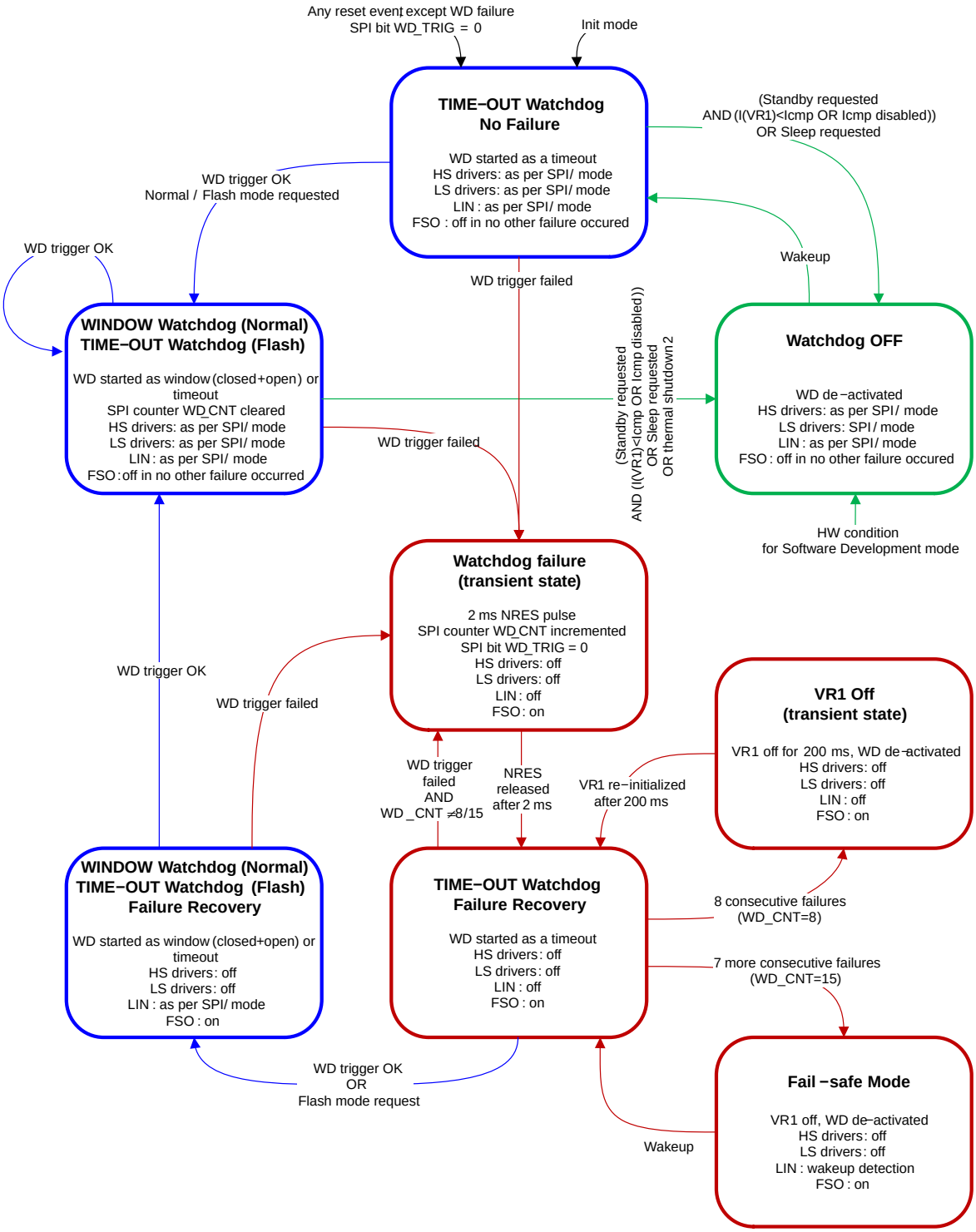



**Figure 16. Watchdog Operation**

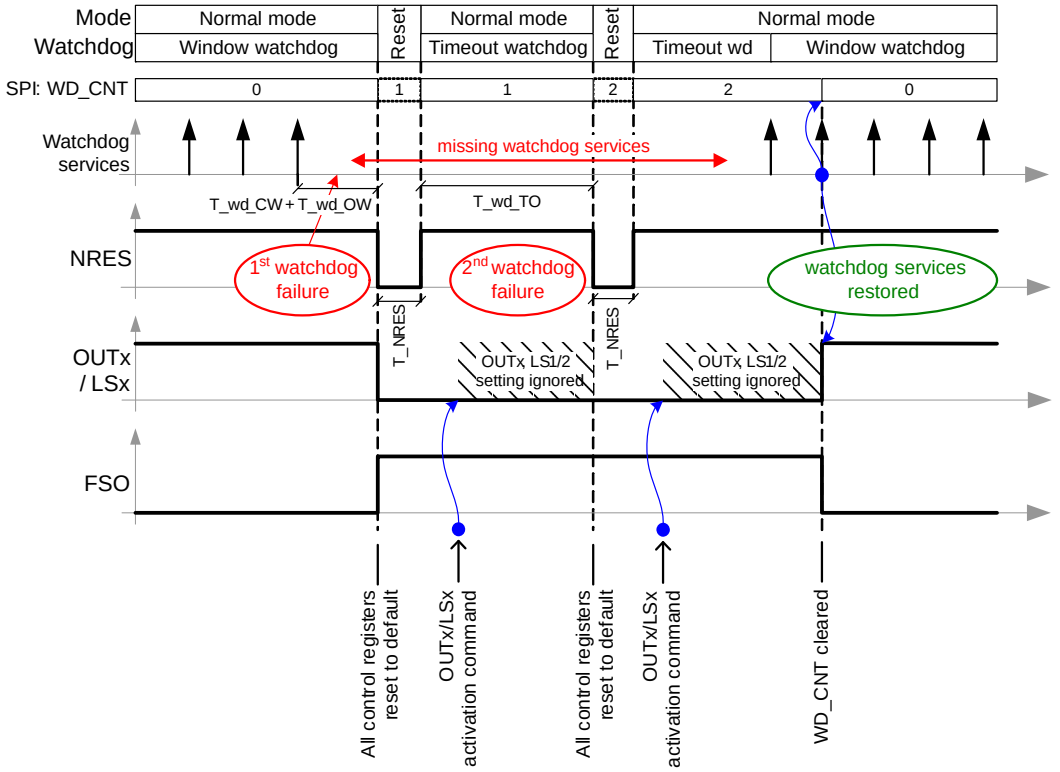



**Figure 17. Watchdog Failure − Isolated Events**

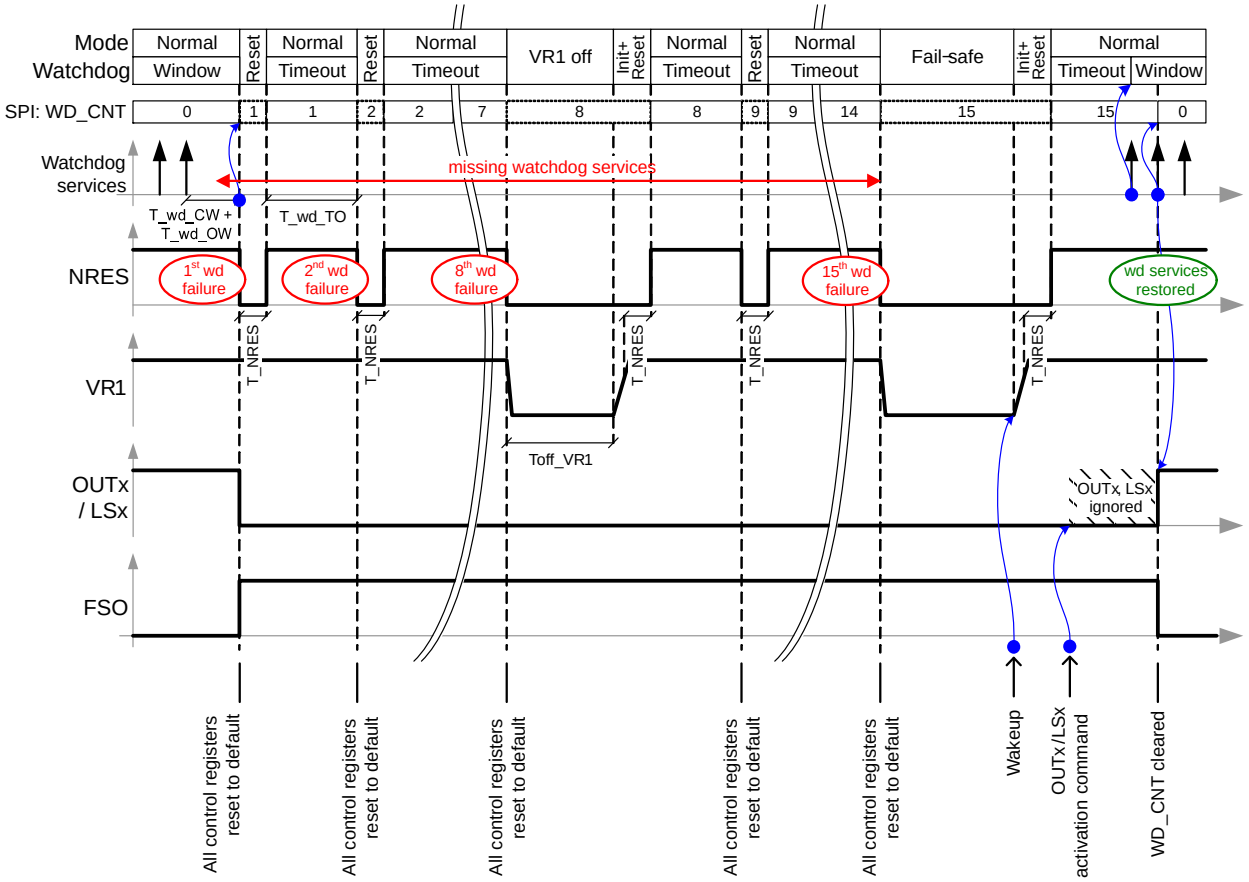



**Figure 18. Watchdog Failure − Multiple Events**

## PROTECTION

### Thermal Protection

The device junction temperature is monitored in order to avoid permanent degradation or damage. Three distinct junction temperature levels are provided – thermal warning level Tjw (typ. 135°C), thermal shutdown level 1 Tjsd1 (typ. 145°C) and thermal shutdown level 2 Tjsd2 (typ. 155°C). The thermal protection circuit is always active in the Normal and Standby mode. It is also active in the Sleep mode if any of the high-side outputs is active.

When the junction temperature exceeds the warning level, the event is only latched into the SPI for subsequent diagnostics without any direct effect on the device configuration. When the first thermal shutdown level is exceeded, the most power-consuming functions are disabled (high- and low- side drivers) while VR1 keeps running so that the MCU can still take appropriate actions. Junction temperature above the second shutdown level leads to complete device de-activation, VR1 included and SPI counter TSD_CNT[2:0] is incremented. VR1 is re-started after a waiting time of 1 second in case the junction temperature drops below the second shutdown level. If the thermal shutdown then re-occurs seven more times, the device is forced into the Fail-safe mode. TSD_CNT[2:0] is decremented by one after each one minute without thermal shutdown 2 event.

"TSD1" SPI flag has to be cleared to re-activate the high- and low- side drivers. In the Standby and Sleep mode, the interrupt request is generated to inform the microcontroller about the thermal shutdown 1 event.

The details of the thermal protection handling are shown in Figure 19, Figure 20 and Figure 21.

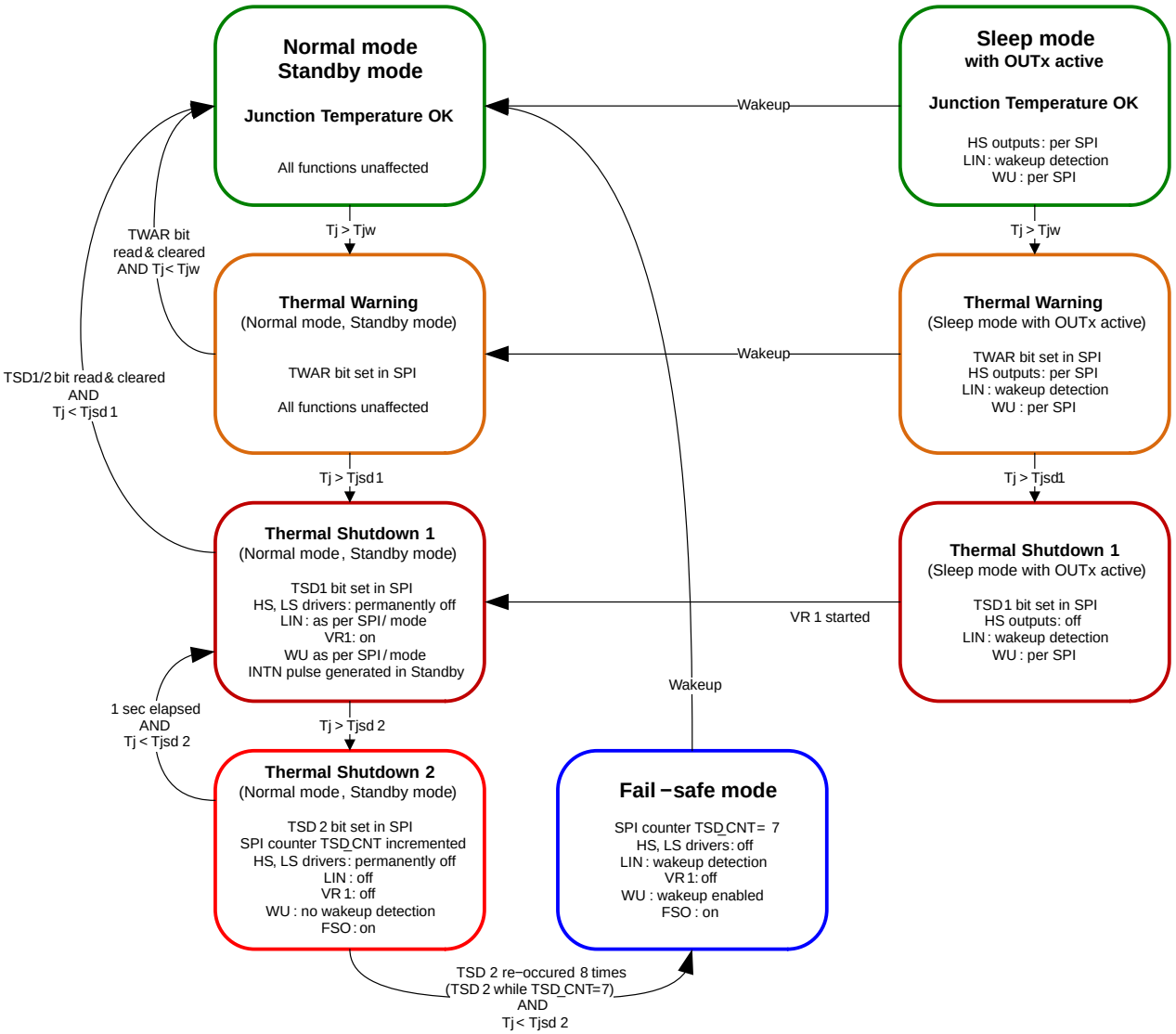



**Figure 19. Thermal Protection**

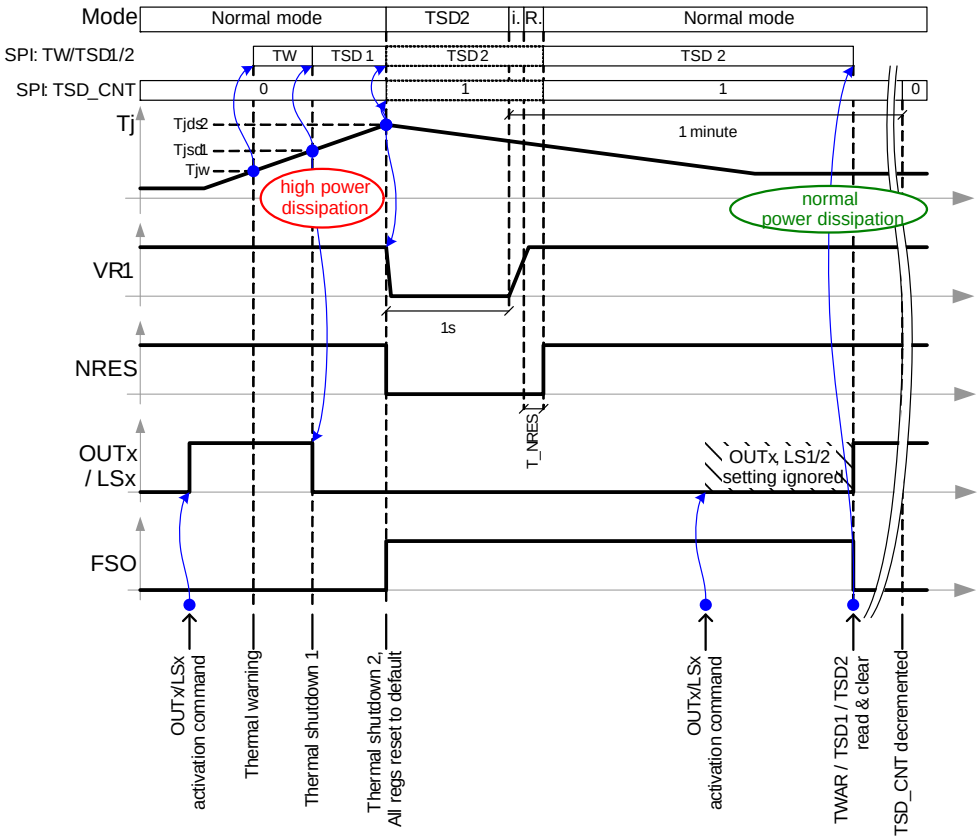



**Figure 20. Thermal Monitoring − Single Event**

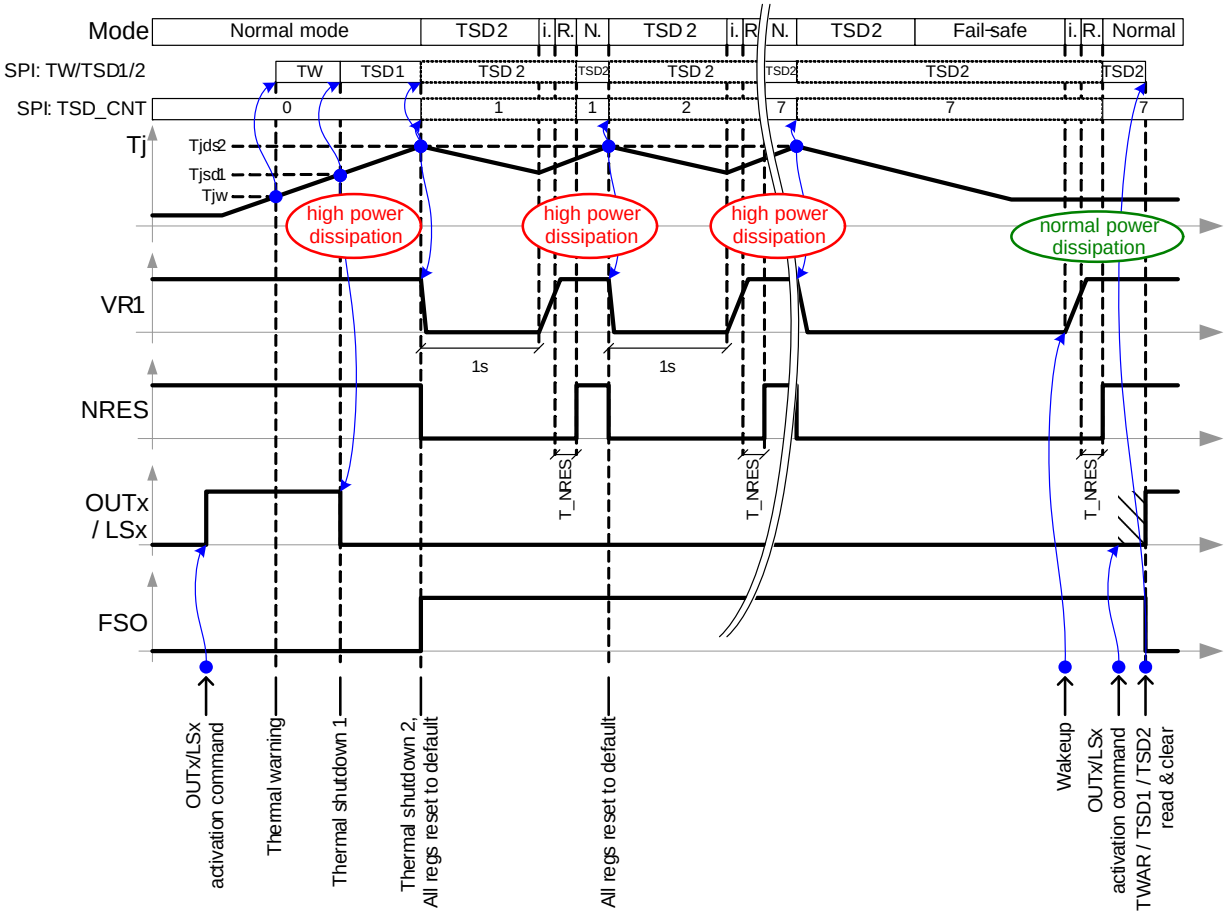



**Figure 21. Thermal Monitoring − Multiple Events**

### VS_OUT Over- and Under-Voltage

In order to protect the loads connected to the high- and low- side drivers, the VS_OUT (car battery) supply is compared against two levels – under-voltage level *VS_OUT_UV* (typ. 5.5 V) and *VS_OUT_OV* (typ. 21 V). The VS_OUT monitoring circuitry is active in Normal mode as well as in the Standby and Sleep modes.

Whenever VS_OUT falls below the *VS_OUT_UV* level or raises above *VS_OUT_OV* level, all high-side drivers are disabled. The under/over-voltage event is latched in the corresponding SPI status bit and if SPI bit “WU_OVUV” is set, the wakeup request is generated in Standby or Sleep mode.

If the SPI control bit “LS_OVUV” is low, the same action is taken for the low-side drivers. After the VS_OUT under/over-voltage condition disappears, it remains flagged in the SPI status. If the SPI control bit “VS_LOCK_DIS” is low, the drivers will remain deactivated until the corresponding flag is not read and cleared. If “VS_LOCK_DIS” is high, the drivers will return to their state defined by SPI registers settings. The details of the VS_OUT monitoring are shown in Figure 22.

SPI control bit “VS_LOCK_DIS” is ignored by OUT3 driver in case it is controlled by FSO signal. OUT3 will return to the previous state immediately after VS_OUT under/over-voltage disappears.

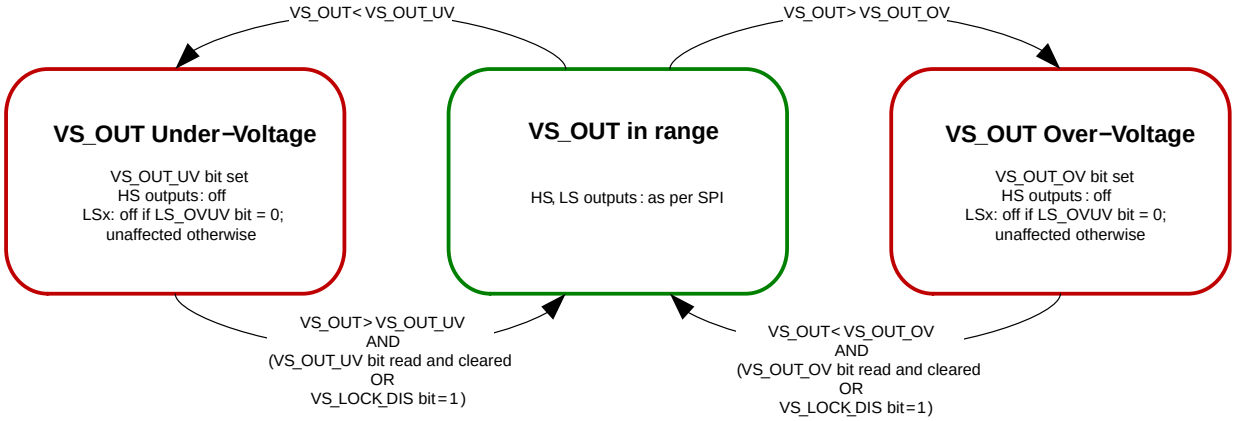



**Figure 22. Under- and Over-voltage on VS_OUT Supply**

## RESET SIGNAL NRES

NRES is an open-drain output with an internal pull-up resistor connected to VR1. It signals reset to the MCU as a consequence of several specific events:

- VR1 under-voltage (including VS power-up)
- Watchdog failure
- Thermal shutdown 2
- Sleep mode
- Wakeup from Sleep mode (the wakeup is accompanied by reset – see Table 6; SPI control registers are not cleared)
- Fail-safe mode

The low-level pulse on NRES pins always extends *T_NRES* (typ. 2 ms) beyond the reset event – e.g. a watchdog failure causes a 2 ms NRES low pulse; a VR1 under-voltage causes NRES pulse extending 2 ms beyond the under-voltage disappearance.

After NRES pulse caused by failure (not after wakeup from Sleep mode), all outputs (OUT1−3, LS1/2) are inactive and CONTROL SPI registers are cleared, except “FSO_DIS” bit. After a wakeup from the Sleep mode, registers content is preserved.

Both LIN transmission and reception is blocked during NRES pulse. A recessive-to-dominant edge on TxDL pin after NRES pulse is required to start transmission to the LIN bus.

## INTERRUPT SIGNAL

An interrupt request is used in the Standby mode to indicate some of the wakeup events to the MCU – see section “Wake-up Events”. Interrupt is signaled through RxDL pin by pulling it Low for typically 125 µs. Beside the 125 µs Low pulse, RxDL/INTN remains High throughout the Standby mode.

During Normal mode, RxDL/INTN assumes its normal function (LIN received data).

## FAIL-SAFE (FSO) SIGNAL

A fail-safe signal is internally generated reflecting some critical system failures and events. By default, the signal is connected to the OUT3 output and over-rules the OUT3 SPI settings – active FSO signal switches OUT3 on, inactive FSO signal switches OUT3 off. In case the SPI bit “FSO_DIS” is set, OUT3 acts as a general-purpose high-side driver identically to OUT1 and OUT2. FSO remains then only an internal signal not visible to the application. SPI bit “FSO_DIS” is not cleared during any reset event.

FSO internal signal is active after the following events:

- During the Init phase:
  - VR1 short: FSO is active when VR1 is below its failure level (*Vfail_VR1*) for more than *Tshort_VR1* (typ. 40 ms) during VR1 regulator startup.

- In the Normal and Standby modes:
  - VR1 under-voltage: FSO is active when VR1 is below its failure level (*Vfail_VR1*). It is deactivated only when VR1_FAIL status bit is cleared.
  - Watchdog: FSO is immediately activated in case of failed watchdog trigger. It is deactivated only when the watchdog is correctly triggered again for two times.
  - Thermal shutdown: FSO is active when the junction temperature is above the second shutdown threshold (*Tjsd2*). It is deactivated only when TSD2 status bit is cleared.
- In the Fail-safe mode: FSO is always active. FSO is deactivated only when corresponding SPI flag is cleared.

## SPI CONTROL

Serial Peripheral Interface (SPI) is the main communication channel between the application MCU and NCV7429. The structure of a SPI frame is shown in Figure 23. MCU starts the frame by sending an 8-bit header consisting of two bits of register access mode type followed by a six-bit address. During the header transmission, NCV7429 sends out eight bits of status information regardless the address. After the header, sixteen bits of data are exchanged. A correct SPI frame has either no bits (no SCLK edges during CSN low; serves to read out the global status information) or exactly twenty-four bits. If another amount of clock edges occurs during CSN low, the frame is considered incorrect and the input data are always ignored.

Depending on the access type, the transmitted/received data are treated differently:

- During a write access, SDO signals current content of the register while new data for the same register are received on SDI. The register is refreshed with the new data after a successful completion of the frame (rising edge on CSN). Only the bits eligible for write access are refreshed, the input data are ignored for the others (e.g. a write access to status registers).
- For read access, the data on SDI are ignored; SDO signals data content of the register addressed by the header. After the frame completion, the register content remains unchanged regardless the type of the individual bits.
- For read & clear access, a normal register read is performed. When the frame is completed (CSN rising edge), the register bits eligible for read & clear access are reset to 0.
- Device ROM access switches the address space to sixteen-bit constant data memorized in the NCV7429 (indicating the device version, SPI frame format and other information). Input data are ignored.

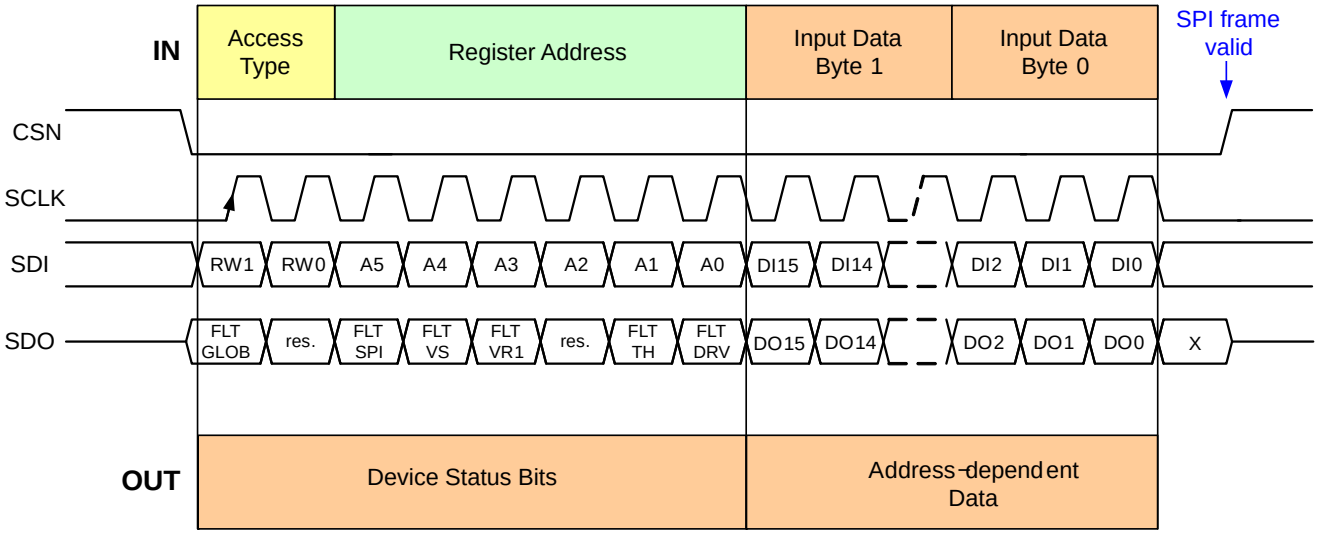



**Figure 23. SPI Frame Structure**

## SPI FRAME FORMAT

| | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | ... | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **NCV7429 IN** | RW1 | RW0 | A5 | A4 | A3 | A2 | A1 | A0 | DI15 | ... | DI0 |
| **NCV7429 OUT** | FLT_GLOB | Reserved | FLT_SPI | FLT_VS | FLT_VR1 | Reserved | FLT_TH | FLT_DRV | DO15 | ... | DO0 |

**Inframe:**

| | RW1 | RW0 | Description |
|---|---|---|---|
| **SPI Access Type** | 0 | 0 | Write to SPI Register |
| | 0 | 1 | Read Only from SPI Register |
| | 1 | 0 | Read & Clear SPI Register |
| | 1 | 1 | Access Device ROM |

| | A5 | A4 | A3 | A2 | A1 | A0 | Register | SPI Access |
|---|---|---|---|---|---|---|---|---|
| **SPI Registers** | 0 | 0 | 0 | 0 | 0 | 0 | CONTROL_0 | Write, Read |
| | 0 | 0 | 0 | 0 | 0 | 1 | CONTROL_1 | Write, Read |
| | 0 | 0 | 0 | 0 | 1 | 0 | CONTROL_2 | Write, Read |
| | 0 | 0 | 0 | 0 | 1 | 1 | CONTROL_3 | Write, Read |
| | 0 | 0 | 0 | 1 | 0 | 0 | CONTROL_4 | Write, Read |
| | 0 | 0 | 0 | 1 | 0 | 1 | Reserved | |
| | 0 | 0 | 0 | 1 | 1 | 0 | PWM_OUT1/2 | Write, Read |
| | 0 | 0 | 0 | 1 | 1 | 1 | PWM_OUT3 | Write, Read |
| | 0 | 0 | 1 | 0 | 0 | 0 | PWM_LS | Write, Read |
| | 0 | 0 | 1 | 0 | 0 | 1 | STATUS_0 | Read, Read & Clear |
| | 0 | 0 | 1 | 0 | 1 | 0 | STATUS_1 | Read, Read & Clear |
| | 0 | 0 | 1 | 0 | 1 | 1 | STATUS_2 | Read, Read & Clear |
| | 0 | 0 | 1 | 1 | X | X | Reserved | |
| | 0 | 1 | X | X | X | X | Reserved | |
| | 1 | X | X | X | X | X | Reserved | |

| | A5 | A4 | A3 | A2 | A1 | A0 | Data Content | Comment |
|---|---|---|---|---|---|---|---|---|
| **Device ROM** | 0 | 0 | 0 | 0 | 0 | 0 | $4300 | ID_HEADER |
| | 0 | 0 | 0 | 0 | 0 | 1 | $0203 | PRODUCT VERSION |
| | 0 | 0 | 0 | 0 | 1 | 0 | $7400 | PRODUCT CODE 1 |
| | 0 | 0 | 0 | 0 | 1 | 1 | $2900 | PRODUCT CODE 2 |
| | 0 | 0 | 0 | 1 | 0 | 0 | Reserved | |
| | ... | ... | ... | ... | ... | ... | Reserved | |
| | 1 | 1 | 1 | 1 | 0 | 1 | Reserved | |
| | 1 | 1 | 1 | 1 | 1 | 0 | $0200 | SPI_FRAME_ID |
| | 1 | 1 | 1 | 1 | 1 | 1 | Reserved | |

**Outframe:**

| | SDO Bit | Bit Name | Bit Content |
|---|---|---|---|
| **General Device Status Info** | D23 | FLT_GLOB | Logical combination (OR) of all following flags |
| | D22 | Reserved | 0 |
| | D21 | FLT_SPI | Previous SPI frame faulty − wrong number of clocks or addressing a nonexistent address |
| | D20 | FLT_VS | VS_OV OR VS_UV |
| | D19 | FLT_VR1 | Equal to VR1_FAIL bit |
| | D18 | Reserved | 0 |
| | D17 | FLT_TH | TSD2 OR TSD1 OR TWAR |
| | D16 | FLT_DRV | OR combination of all overcurrent and underload bits of OUTx and LSx |

## SPI REGISTER DETAILS

### CONTROL_0 REGISTER

Address: 00h
Access: Write, Read

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Access Type | RW | RW | RW | RW | RW | RW | − | − | RW | RW | − | − | RW | RW | RW | RW |
| Bit Name | MODE.1 | MODE.0 | WD TRIG | WD PER.1 | WD PER.0 | ICMP STBY | Res. | Res. | VR1 RES.1 | VR1 RES.0 | Res. | Res. | LIN SLOPE | TXDL TO.1 | TXDL TO.0 | FSO DIS |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x |

| | MODE.1 | MODE.0 | Operating Mode Request |
|---|---|---|---|
| Mode Control | 0 | 0 | Normal mode (window watchdog) |
| | 0 | 1 | Go to Sleep mode |
| | 1 | 0 | Go to Standby mode |
| | 1 | 1 | Flash mode (time-out watchdog); preceding SPI command has to set FLASH_RDY bit in CONTROL_2, otherwise mode is not changed |

| | WD_TRIG | Watchdog Trigger Bit |
|---|---|---|
| Watchdog Trigger Bit | 0 | Watchdog trigger set to 0; default state after wakeup from Sleep |
| | 1 | Watchdog trigger set to 1 |

| | WD_PER.1 | WD_PER.0 | Configuration of the Watchdog Trigger Time |
|---|---|---|---|
| Watchdog Trigger Time | 0 | 0 | Trigger time = 9.75 ms (Normal mode) / Timeout = 16 ms (Flash mode) |
| | 0 | 1 | Trigger time = 39 ms (Normal mode) / Timeout = 64 ms (Flash mode) |
| | 1 | 0 | Trigger time = 97.5 ms (Normal mode) / Timeout = 160 ms (Flash mode) |
| | 1 | 1 | Trigger time = 195 ms (Normal mode) / Timeout = 640 ms (Flash mode) |

| | ICMP_STBY | Disables the VR1 Current Comparator |
|---|---|---|
| Standby VR1 Comparator | 0 | Comparator is Enabled in Standby mode |
| | 1 | Comparator is Disabled |

| | VR1_RES.1 | VR1_RES.0 | Adjustment of the VR1 Reset Level |
|---|---|---|---|
| VR1 Reset Level | 0 | 0 | Set the reset threshold to typ. 4.5 V (91%) |
| | 0 | 1 | Set the reset threshold to typ. 4.3 V (87%) |
| | 1 | 0 | Set the reset threshold to typ. 3.9 V (79%) |
| | 1 | 1 | Set the reset threshold to typ. 3.7 V (74%) |

| | LIN_SLOPE | Change of the LIN Slope |
|---|---|---|
| LIN Slope Control | 0 | High slew rate (as per LIN specification) |
| | 1 | Low slew rate |

| | TxDL_TO.1 | TxDL_TO.0 | Dominant TxD Time-out Configuration of the LIN Interface |
|---|---|---|---|
| TxDL Time-out Timer | 0 | 0 | Set the timer to typ. 55 ms |
| | 0 | 1 | Set the timer to typ. 13 ms |
| | 1 | 0 | Time-out timer disabled |
| | 1 | 1 | Time-out timer disabled |

| | FSO_DIS | OUT3/FSO Function |
|---|---|---|
| FSO Function Disable | 0 | OUT3 pin is driven by internal FSO signal |
| | 1 | OUT3 pins is a general-purpose high-side driver, setting not cleared during Reset |

### CONTROL_1 REGISTER

Address: 01h
Access: Write, Read

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Access Type** | – | RW | RW | RW | – | – | RW | – | – | RW | – | – | – | – | RW | RW |
| **Bit Name** | Res. | WU LIN DIS | WU TIM EN.1 | WU TIM EN.0 | Res. | Res. | WU DIS | Res. | Res. | WU PUD | Res. | Res. | Res. | Res. | WU T.1 | WU T.0 |
| **Reset Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | WU_LIN_DIS | Disables LIN Wakeup in Standby or Sleep Mode |
|---|---|---|
| **LIN Wakeup Disable** | 0 | LIN Wakeup Enabled |
| | 1 | LIN Wakeup Disabled |

| | WU_DIS | Disables WU Input Wakeup in Standby or Sleep Mode |
|---|---|---|
| **WU Input Wakeup Disable** | 0 | WU Input Wakeup Enabled |
| | 1 | WU Input Wakeup Disabled |

| | WU_PUD | WU Input Sink/Source Current Configuration |
|---|---|---|
| **WU Input Sink/Source** | 0 | WU configured as current sink in all modes, if WU wakeup is enabled |
| | 1 | WU configured as current source in all modes, if WU wakeup is enabled |

| | WU_TIM_EN.[1:0] | | Enables Cyclic (Timer Controlled) Wakeup from Standby or Sleep Mode |
|---|---|---|---|
| **Timer Wakeup Control** | 0 | 0 | Timers 1/2 are not used as wakeup sources |
| | 0 | 1 | Wakeup generated based on Timer 1 |
| | 1 | 0 | Wakeup generated based on Timer 2 |
| | 1 | 1 | Wakeup generated based on Timer 1 |

| | WU_T.[1:0] | | Defines the Filter Configuration for Wake Input WU |
|---|---|---|---|
| **WU Input Filter Time** | 0 | 0 | Static sense with 64 μs filter time (static sense) |
| | 0 | 1 | Timer 2 cyclic sense with sampling start 20 μs before off-state and 16 μs filter time |
| | 1 | 0 | Timer 2 cyclic sense with sampling start 20 μs before off-state and 16 μs filter time |
| | 1 | 1 | Timer 1 cyclic sense with sampling start 20 μs before off-state and 16 μs filter time |

### CONTROL_2 REGISTER

Address: 02h
Access: Write, Read

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Access Type** | RW | RW | – | – | – | – | – | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| **Bit Name** | FLASH RDY | SWDM SAMP | Res. | Res. | Res. | Res. | Res. | T2 TPER.2 | T2 TPER.1 | T2 TPER.0 | T2 TON.1 | T2 TON.0 | T1 TPER.2 | T1 TPER.1 | T1 TPER.0 | T1 TON |
| **Reset Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | FLASH_RDY | Unlocks Flash Mode Entry |
|---|---|---|
| **Flash Ready** | 0 | Flash mode request in CONTROL_0 register ignored |
| | 1 | Flash mode may be entered by setting MODE.[1:0] to 11b in following SPI write request. This bit is automatically cleared by any following SPI write command. |

| | SWDM_SAMP | SWDM Pin Sample Request |
|---|---|---|
| **SWDM Pin Sample** | 0 | SWDM latched value preserved |
| | 1 | SWDM pin sample is requested. New SWDM value will be latched. This bit is automatically cleared when the sampling is finished. |

| | T2_TPER.[2:0] | | | Defines the Period of the Cyclic Sense Timer2 |
|---|---|---|---|---|
| **Timer2 Period** | 0 | 0 | 0 | Period: 200 ms |
| | 0 | 0 | 1 | Period: 50 ms |
| | 0 | 1 | 0 | Period: 20 ms |
| | 0 | 1 | 1 | Period: 10 ms |
| | 1 | 0 | 0 | Period: 100 ms |
| | 1 | 0 | 1 | Period: 150 ms |
| | 1 | 1 | 0 | Reserved − if used, will be equal to the default value of 200 ms |
| | 1 | 1 | 1 | Reserved − if used, will be equal to the default value of 200 ms |

| | T2_TON.[1:0] | | Defines the On Time for the Cyclic Sense Timer2 |
|---|---|---|---|
| **Timer2 On-time** | 0 | 0 | ON time 100 μs |
| | 0 | 1 | ON time 200 μs |
| | 1 | 0 | ON time 1 ms |
| | 1 | 1 | ON time 5 ms |

| | T1_TPER.[2:0] | | | Defines the Period of the Cyclic Sense Timer1 |
|---|---|---|---|---|
| **Timer1 Period** | 0 | 0 | 0 | Period: 0.5 s |
| | 0 | 0 | 1 | Period: 1.0 s |
| | 0 | 1 | 0 | Period: 1.5 s |
| | 0 | 1 | 1 | Period: 2.0 s |
| | 1 | 0 | 0 | Period: 2.5 s |
| | 1 | 0 | 1 | Period: 3.0 s |
| | 1 | 1 | 0 | Period: 3.5 s |
| | 1 | 1 | 1 | Period: 4.0 s |

| | T1_TON | Defines the On Time for the Cyclic Sense Timer1 |
|---|---|---|
| **Timer1 On-time** | 0 | ON time 10 ms |
| | 1 | ON time 20 ms |

### CONTROL_3 REGISTER

Address: 03h
Access: Write, Read

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Access Type** | RW | RW | RW | – | – | – | – | – | RW | RW | RW | RW | RW | RW | – | – |
| **Bit Name** | WU TSD | WU OC | WU OVUV | Res. | Res. | Res. | Res. | Res. | VS LOCK DIS | LS OVUV | LS2 ON.1 | LS2 ON.0 | LS1 ON.1 | LS1 ON.0 | Res. | Res. |
| **Reset Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | WU_TSD | Enables Thermal Shutdown 1 Wakeup |
|---|---|---|
| **Thermal Shutdown 1 Wakeup** | 0 | TSD1 wakeup disabled |
| | 1 | TSD1 wakeup enabled in Standby/Sleep mode |

| | WU_OC | Enables OUT1−3 Overcurrent Wakeup |
|---|---|---|
| **OUT1−3 Overcurrent Wakeup** | 0 | OUT1−3 overcurrent wakeup disabled |
| | 1 | OUT1−3 overcurrent wakeup enabled in Standby/Sleep mode |

| | WU_OVUV | Enables VS_OUT Over-/Under-voltage Wakeup |
|---|---|---|
| **VS_OUT OV/UV Wakeup** | 0 | VS_OUT OV/UV wakeup disabled |
| | 1 | VS_OUT OV/UV wakeup enabled in Standby/Sleep mode |

| | VS_LOCK_DIS | Disables the Automatic VS_OUT Lockout |
|---|---|---|
| **VS_OUT UV/OV Lockout** | 0 | Outputs will be reactivated only when the VS_OUT UV/OV flag is cleared |
| | 1 | Outputs will be reactivated when VS_OUT UV/OV condition disappears |

| | LS_OVUV | Enables LSx in Case of VS_OUT OV/UV |
|---|---|---|
| **LS1/2 Active in VS_OUT UV/OV** | 0 | Disabled − LSx will be disabled in case of VS_OUT UV/OV |
| | 1 | Enabled − LSx will remain in their previous state in case of VS_OUT UV/OV |

| | LSx_ON.1 | LSx_ON.0 | Defines the Configuration of the Low-side LS1/2 |
|---|---|---|---|
| **LS1/2 Driver Control** | 0 | 0 | Driver is off in all modes |
| | 0 | 1 | Driver is on in Normal/Flash mode (off in other modes) |
| | 1 | 0 | Driver is controlled by its PWM setting in Normal/Flash mode (off in other modes) |
| | 1 | 1 | Reserved − if used, LSx will be off in all modes (equal to default) |

### CONTROL_4 REGISTER

Address: 04h
Access: Write, Read

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Access Type** | RW | – | – | – | RW | RW | RW | RW | RW | RW | RW | RW | RW | – | – | – |
| **Bit Name** | OUT1 HIGHR | Res. | Res. | Res. | OUT3 ON.2 | OUT3 ON.1 | OUT3 ON.0 | OUT2 ON.2 | OUT2 ON.1 | OUT2 ON.0 | OUT1 ON.2 | OUT1 ON.1 | OUT1 ON.0 | Res. | Res. | Res. |
| **Reset Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | OUT1_HIGHR | Enables Weaker Switch on OUT1 Output |
|---|---|---|
| **OUT1 Switch Strength** | 0 | “Normal-ohmic” configuration; typ. 5 Ω Ron; parameters equal to OUT2−3 |
| | 1 | “High-ohmic” configuration; typ. 20 Ω Ron; lower underload threshold and current limitation |

| | OUTx_ON.[2:0] | | | Defines the Configuration of the High-side OUT1..3 |
|---|---|---|---|---|
| **OUT1−3 Driver Control** | 0 | 0 | 0 | Driver is off in all modes |
| | 0 | 0 | 1 | Driver is on in Normal/ Flash, Standby and Sleep mode |
| | 0 | 1 | 0 | Driver is cyclic on with the timing of Timer1 in Normal/Flash, Standby and Sleep mode |
| | 0 | 1 | 1 | Driver is cyclic on with the timing of Timer2 in Normal/Flash, Standby and Sleep mode |
| | 1 | 0 | 0 | Driver is controlled by the corresponding PWM unit in Normal/Flash, Standby and Sleep mode |
| | 1 | 0 | 1 | Reserved − if used, the driver is off in all modes (equal to default) |
| | 1 | 1 | 0 | Reserved − if used, the driver is off in all modes (equal to default) |
| | 1 | 1 | 1 | Reserved − if used, the driver is off in all modes (equal to default) |

### PWM_OUT1/2 REGISTER

Address: 06h
Access: Write, Read

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Access Type** | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| **Bit Name** | FSEL OUT1 | PW OUT1.6 | PW OUT1.5 | PW OUT1.4 | PW OUT1.3 | PW OUT1.2 | PW OUT1.1 | PW OUT1.0 | FSEL OUT2 | PW OUT2.6 | PW OUT2.5 | PW OUT2.4 | PW OUT2.3 | PW OUT2.2 | PW OUT2.1 | PW OUT2.0 |
| **Reset Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### PWM_OUT3 REGISTER

Address: 07h
Access: Write, Read

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Access type** | RW | RW | RW | RW | RW | RW | RW | RW | – | – | – | – | – | – | – | – |
| **Bit Name** | FSEL OUT3 | PW OUT3.6 | PW OUT3.5 | PW OUT3.4 | PW OUT3.3 | PW OUT3.2 | PW OUT3.1 | PW OUT3.0 | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. |
| **Reset Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### PWM_LS REGISTER

Address: 08h
Access: Write, Read

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Access Type** | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| **Bit Name** | FSEL LS1 | PW LS1.6 | PW LS1.5 | PW LS1.4 | PW LS1.3 | PW LS1.2 | PW LS1.1 | PW LS1.0 | FSEL LS2 | PW LS2.6 | PW LS2.5 | PW LS2.4 | PW LS2.3 | PW LS2.2 | PW LS2.1 | PW LS2.0 |
| **Reset Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| PWM Frequency | FSEL_OUTx<br>FSEL_LSx | PWM Frequency Selector |
|---|---|---|
| | 0 | Base frequency of PWM on the corresponding output f(PWM) = 150 Hz |
| | 1 | Base frequency of PWM on the corresponding output f(PWM) = 200 Hz |

| Output Duty Cycle | PW_OUTx[6:0]<br>PW_LSx[6:0] | Duty Cycle Selector |
|---|---|---|
| | $0 … $7F | Corresponding output is active with duty cycle PW_xxx[6:0] / 127 |

### STATUS_0 REGISTER

Address: 09h
Access: Read, Read & Clear

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Access Type | R | R | R | R/RC | R/RC | R | – | – | R/RC | R | R | R | R | R | R | R |
| Bit Name | OP MOD.1 | OP MOD.0 | COLD START | WU TIM | WU LIN | SWDM | Res. | Res. | WU WU | WD CNT.3 | WD CNT.2 | WD CNT.1 | WD CNT.0 | TSD CNT.2 | TSD CNT.1 | TSD CNT.0 |

| | OPMOD.1 | OPMOD.0 | Operating Mode |
|---|---|---|---|
| **Operating Mode** | 0 | 0 | Sleep or Fail-safe – latched; updated after first successful access to the register |
| | 0 | 1 | Standby |
| | 1 | 0 | Normal |
| | 1 | 1 | Flash |

| | COLD_START | Power on Reset Status |
|---|---|---|
| **Cold Start** | 0 | Cold start (= VS connection) not occurred |
| | 1 | Cold start (= VS connection) occurred;<br>cleared after first successful access of the register |

| | WU_TIM | WU_LIN | Remote Wake-up Source |
|---|---|---|---|
| **Wake-up Source Recognition** | 0 | 0 | No timer nor LIN wake-up occurred |
| | X | 1 | LIN wake-up occurred |
| | 1 | X | Timer wake-up occurred |

| | SWDM | Software Development Mode Status (SWDM Pin) |
|---|---|---|
| **SWDM Status** | 0 | SWDM low during sampling – Normal watchdog operation |
| | 1 | SWDM high during sampling – Software Development mode entered |

| | WU_WU | Local Wake-up Source (WU Pin) |
|---|---|---|
| **Wake-up Source Recognition** | 0 | No WU pin wake-up occurred |
| | 1 | WU pin wake-up occurred |

| | WD_CNT.[3:0] | Number of Watchdog Failures |
|---|---|---|
| **Watchdog Failure Counter** | 0 | No watchdog failure encountered |
| | $1 … $E | Non-zero number of watchdog failures encountered;<br>cleared by second successful watchdog service |
| | $F | Fail-safe mode entered due to 15 watchdog failures;<br>cleared by successful watchdog service |

| | TSD_CNT.[2:0] | Number of VR1 Restarts after Thermal Shutdown 2 |
|---|---|---|
| **TSD2 VR1 Restart Counter** | 0 | No VR1 restarts encountered |
| | $1 … $6 | Non-zero VR1 restarts encountered; decremented after 1 minute |
| | $7 | Seven consecutive thermal shutdown 2 events, another TSD2 leads to Fail-safe mode entry; decremented after 1 minute after wakeup if no another TSD2 occurs |

### STATUS_1 REGISTER

Address: 0Ah
Access: Read, Read & Clear

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Access Type** | R/RC | – | – | R | – | – | R/RC | – | – | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | – |
| **Bit Name** | FAIL SAFE | Res. | Res. | WU | Res. | Res. | VR1 FAIL | Res. | Res. | VS OUT OV | VS OUT UV | TSD2 | TSD1 | TWAR | TO TxDL | Res. |

| | FAIL_SAFE | Wakeup from Fail-safe Mode |
|---|---|---|
| **Fail-safe Mode** | 0 | Fail-safe was not entered |
| | 1 | Wakeup from Fail-safe mode |

| | WU | Status of WU Input in Normal Mode |
|---|---|---|
| **Status of WU Input** | 0 | WU is Low |
| | 1 | WU is High |

| | VR1_FAIL | Voltage Regulator VR1 Failure |
|---|---|---|
| **VR1 Failure** | 0 | No VR1 failure occurred |
| | 1 | VR1 fails for at least 5 μs (VR1 < 2 V for > 5 μs) OR<br>(VR1 < 2 V at 40 ms after turn-on) |

| | VS_OUT_OV | Overvoltage on VS_OUT Pin |
|---|---|---|
| **VS_OUT Overvoltage** | 0 | VS_OUT has not been above the overvoltage limit |
| | 1 | VS_OUT exceeded the overvoltage limit (latched) |

| | VS_OUT_UV | Undervoltage on VS_OUT Pin |
|---|---|---|
| **VS_OUT Undervoltage** | 0 | VS_OUT has not been below the undervoltage limit |
| | 1 | VS_OUT fell below the undervoltage limit (latched) |

| | TSD2 | TSD1 | TWAR | Thermal Warning/Shutdown |
|---|---|---|---|---|
| **Thermal Protection** | 0 | 0 | 0 | No thermal limit exceeded |
| | 0 | 0 | 1 | Thermal warning encountered |
| | 0 | 1 | 1 | Thermal shutdown 1 encountered |
| | 1 | 1 | 1 | Thermal shutdown 2 encountered |
| | Other Combinations | | | Reserved |

| | TO_TxDL | TxDL Dominant |
|---|---|---|
| **Permanent Dominant Protection** | 0 | No LIN transmitter timeout encountered |
| | 1 | LIN transmitter timeout encountered |

### STATUS_2 REGISTER

Address: 0Bh
Access: Read, Read & Clear

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Access Type** | − | − | R | R | R/RC | R/RC | − | − | R/RC | R/RC | R/RC | − | − | R/RC | R/RC | R/RC |
| **Bit Name** | Res. | Res. | WD STAT.1 | WD STAT.0 | LS2 OC | LS1 OC | Res. | Res. | OUT3 OC | OUT2 OC | OUT1 OC | Res. | Res. | OUT3 UL | OUT2 UL | OUT1 UL |

| | WD_STAT.[1:0] | | Watchdog Counter Status |
|---|---|---|---|
| **Watchdog Counter Status** | 0 | 0 | Watchdog counter below 33% of acceptable interval (Note 1) |
| | 0 | 1 | Watchdog counter above 33% and below 66% of acceptable interval (Note 1) |
| | 1 | 0 | Reserved − not used |
| | 1 | 1 | Watchdog counter above 66% of acceptable interval (Note 1) |

1. Acceptable interval means timeout or open window interval

| | LSx_OC OUTx_OC | Overcurrent Status of the Corresponding Output |
|---|---|---|
| **Driver Overcurrent** | 0 | No overcurrent encountered |
| | 1 | Overcurrent encountered |

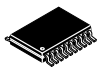
| | OUTx_UL | Underload Status of the Corresponding Output |
|---|---|---|
| **Driver Underload** | 0 | No underload encountered |
| | 1 | Underload encountered |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

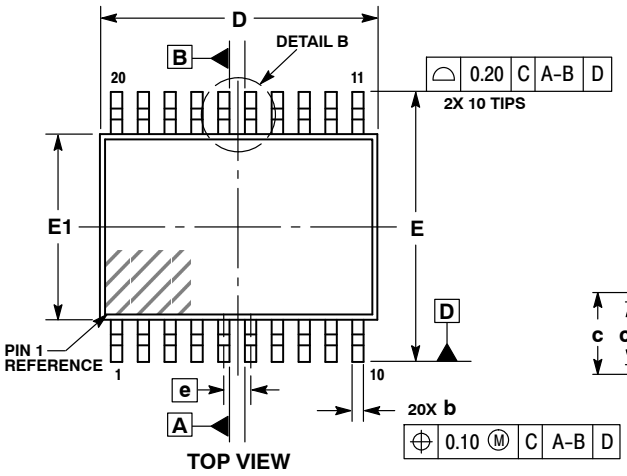
ON Semiconductor®

**TSSOP−20 EP**
CASE 948AB−01
ISSUE O

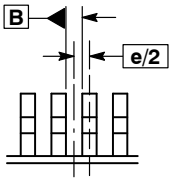
DATE 17 JUN 2008



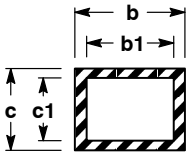
SCALE 1:1




TOP VIEW

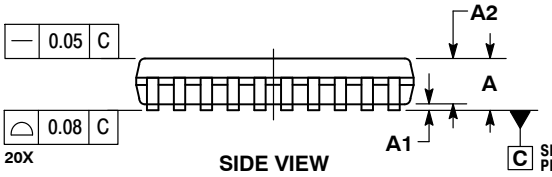



DETAIL B

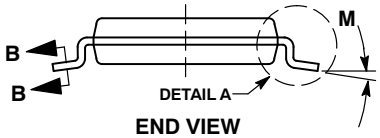



SECTION B−B

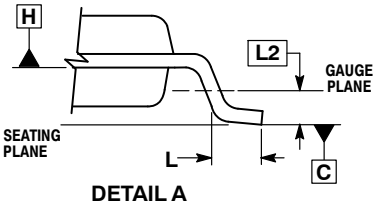
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07 IN EXCESS OF THE LEAD WIDTH AT MMC. DAMBAR CANNOT BE LOACTED ON THE LOWER RADIUS OR THE FOOT OF THE LEAD.
4. DIMENSIONS b, b1, c, c1 TO BE MEASURED BETWEEN 0.10 AND 0.25 FROM LEAD TIP.
5. DATUMS A AND B ARE ARE DETERMINED AT DATUM H. DATUM H IS LOACTED AT THE MOLD PARTING LINE AND COINCIDENT WITH LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
6. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.




SIDE VIEW

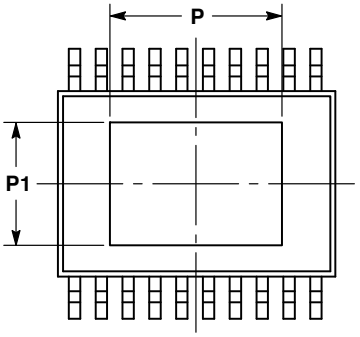



END VIEW



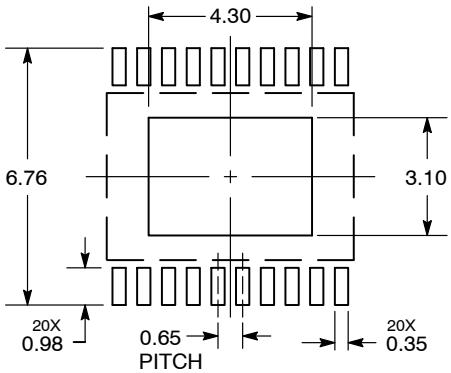

DETAIL A

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | --- | 1.10 |
| A1 | 0.05 | 0.15 |
| A2 | 0.85 | 0.95 |
| b | 0.19 | 0.30 |
| b1 | 0.19 | 0.25 |
| c | 0.09 | 0.20 |
| c1 | 0.09 | 0.16 |
| D | 6.40 | 6.60 |
| E | 6.40 BSC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BSC | |
| L | 0.50 | 0.70 |
| L2 | 0.25 BSC | |
| M | 0° | 8° |
| P | --- | 4.20 |
| P1 | --- | 3.00 |



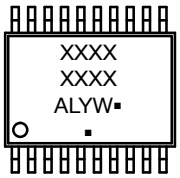

BOTTOM VIEW

**SOLDERING FOOTPRINT**




DIMENSIONS: MILLIMETERS

**GENERIC MARKING DIAGRAM***




XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

| | | |
|---|---|---|
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