THIS SPEC IS OBSOLETE

Spec No: 002-06635

Spec Title: MB89470 Series, F2MC-8L 8-bit Proprietary Microcontroller

Replaced by: NONE

The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

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FUJITSU MICROELECTRONICS
DATA SHEET

DS07-12552-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89470 Series

MB89475/P475/PV470

■ DESCRIPTION

The MB89470 series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontroller contains a variety of peripheral functions such as 21-bit time-base timer, watch prescaler, PWC timer, PWM timer, 8/16-bit timer/counter, external interrupt 1 (edge) , external interrupt 2 (level) , 10-bit A/D converter, UART/SIO, buzzer, watchdog timer reset.

The MB89470 series is designed suitable for home appliance as well as in a wide range of applications for consumer product.

* : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- Package used
  QFP package, LQFP package and SH-DIP package for MB89P475, MB89475
  MQFP package for MB89PV470

(Continued)

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

2008.9

(Continued)

- High-speed operating capability at low voltage
- Minimum execution time : 0.32 µs/12.5 MHz
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test and branch instructions
  - Bit manipulation instructions, etc.
- Six timers
  PWC timer (also usable as an interval timer)
  PWM timer
  8/16-bit timer/counter × 2
  21-bit timebase timer
  Watch prescaler
- Buzzer
  7 frequency types are selectable by software
- External interrupts
  Edge detection (Selectable edge) : 4 channels
  Low-level interrupt (Wake-up function) : 5 channels
- A/D converter (8 channels)
  10-bit successive approximation type
- UART/SIO
  Synchronous/asynchronous data transfer capable
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Subclock mode (for dual clock product)
  Watch mode (for dual clock product)
- Watchdog timer reset
- I/O ports : Max 39 channels

■ PRODUCT LINEUP

Part number / Parameter	MB89475	MB89P475	MB89PV470
Classification	Mass production products (mask ROM product)	OTP	Piggy-back
ROM size	16 K × 8-bit (internal ROM)	16 K × 8-bit (internal PROM, can be written to by ROM programmer)	32 K × 8-bit (external ROM)
RAM size	512 × 8 bits		1 K × 8 bits
CPU functions	Number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum execution time : 0.32 µs/12.5 MHz Minimum interrupt processing time : 2.88 µs/12.5 MHz		
Ports	Output-only ports (N-channel open drain) : 7 pins Input-only ports : 3 pins (1 pin in product with dual clock) I/O ports (CMOS) : 29 pins Total : 39 pins		
21-bit Time-base timer	Interrupt period (0.82 ms, 3.3 ms, 26.2 ms, 419.4 ms) at 10 MHz Interrupt period (0.66 ms, 2.6 ms, 21.0 ms, 335.5 ms) at 12.5 MHz		
Watchdog timer	Reset period (209.7 ms to 419.4 ms) at 10 MHz Reset period (167.8 ms to 335.5 ms) at 12.5 MHz		
Watch prescaler	17 bits Interrupt cycle : 31.25 ms, 0.25 ms, 0.5 s, 1.00 s, 2.00 s, 4.00 s/32.768 kHz for subclock		
Pulse width count timer	2 channels 8-bit one-shot timer operation (supports underflow output, operating clock period : 1, 4, 32 t_{inst}*, external) 8-bit reload timer operation (supports square wave output, operating clock period : 1, 4, 32 t_{inst}*, external) 8-bit pulse width measurement operation (supports continuous measurement, H width, L width, rising edge to rising edge, falling edge to falling edge measurement and both edge measurement)		
PWM timer	8-bit reload timer operation (supports square wave output, operating clock period : 1, 4, 32 t_{inst}*, external) 8-bit resolution PWM operation		
8/16-bit timer/ counter 1, 2	Can be operated either as a 2-channel 8-bit timer/counter (Timer 1 and Timer 2, each with its own independent operating clock cycle) , or as one 16-bit timer/counter In Timer 1 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capable		
8/16-bit timer/ counter 3, 4	Can be operated either as a 2-channel 8-bit timer/counter (Timer 3 and Timer 4, each with its own independent operating clock cycle) , or as one 16-bit timer/counter In Timer 3 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capable		
External interrupt	4 independent channels (selectable edge, interrupt vector, request flag) 5 channels (low level interrupt)		

(Continued)

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Parameter \ Part number	MB89475	MB89P475	MB89PV470
A/D converter	10-bit resolution × 8 channels A/D conversion function (conversion time : 60 t_{inst}*) Supports repeated activation by internal clock.		
UART/SIO	Synchronous/asynchronous data transfer capable (Max baud rate : 78.125 Kbps at 10 MHz) (7 and 8 bits with parity bit ; 8 and 9 bits without parity bit)		
Buzzer output	7 frequency types ($F_{CH}/2^{12}$, $F_{CH}/2^{11}$, $F_{CH}/2^{10}$, $F_{CH}/2^{9}$, $F_{CL}/2^{5}$, $F_{CL}/2^{4}$, $F_{CL}/2^{3}$) are selectable by software.		
Standby mode	Sleep mode, stop mode, subclock mode (dual clock product) and watch mode (dual clock product)		
Process	CMOS		
Operating Voltage	2.2 V to 5.5 V	3.5 V to 5.5 V	2.7 V to 5.5 V

* : t_{inst} is one instruction cycle (execution time) , which can be selected as 1/4, 1/8, 1/16, or 1/64 of main clock.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package \ Part number	MB89475	MB89P475	MB89PV470
DIP-48P-M01	O	O	X
FPT-48P-M26	O	O	X
FPT-48P-M13	O	O	X
MQP-48C-P01	X	X	O

O : Available
X : Not available

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following point :

- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

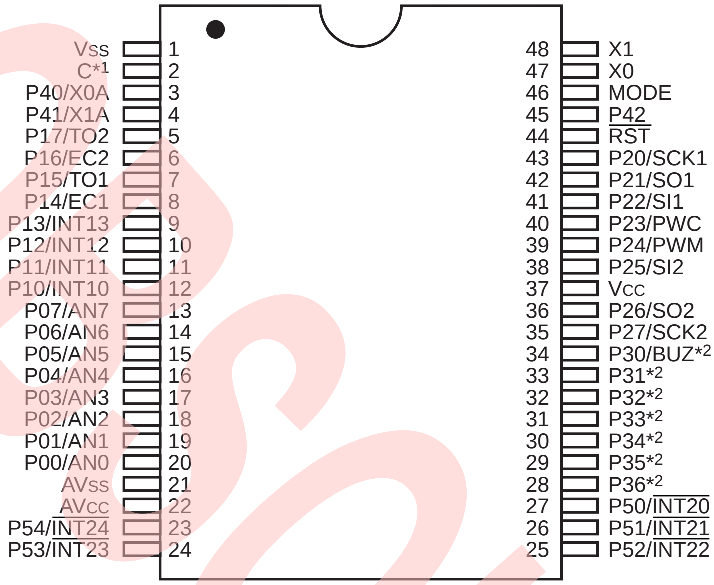
- For the MB89PV470, add the current consumed by the EPROM mounted in the piggy-back socket.
- When operating at low speed, the current consumed by the one-time PROM product is greater than that for the mask ROM product. However, the current consumption are roughly the same in sleep or stop mode.
- For more information, see "■ ELECTRICAL CHARACTERISTICS".

3. Oscillation stabilization time after power-on reset

- For MB89PV470, there is no power-on stabilization time after power-on reset.
- For MB89P475, there is power-on stabilization time after power-on reset.
- For MB89475, the power-on stabilization time can be select.
- For more information, refer to "■ MASK OPTIONS".

■ PIN ASSIGNMENTS

(TOP VIEW)



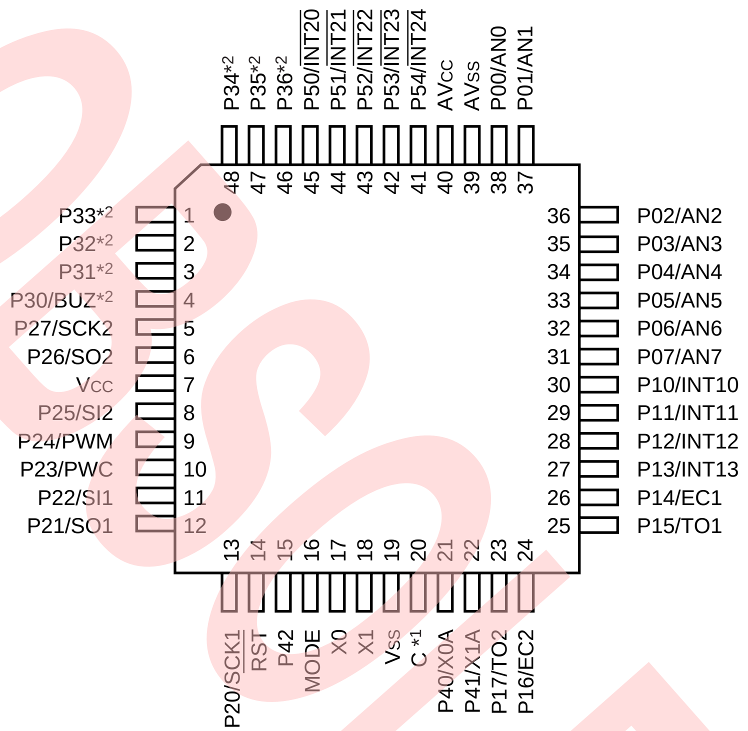
(DIP-48P-M01)

*1 : For pin no. 2, connect this pin to an external 0.1 µF capacitor to ground (for MB89P475 only) .
For MB89PV470 and MB89475, this pin should be left unconnected.

*2 : High current drive type

(Continued)

(TOP VIEW)



(FPT-48P-M26)
(FPT-48P-M13)

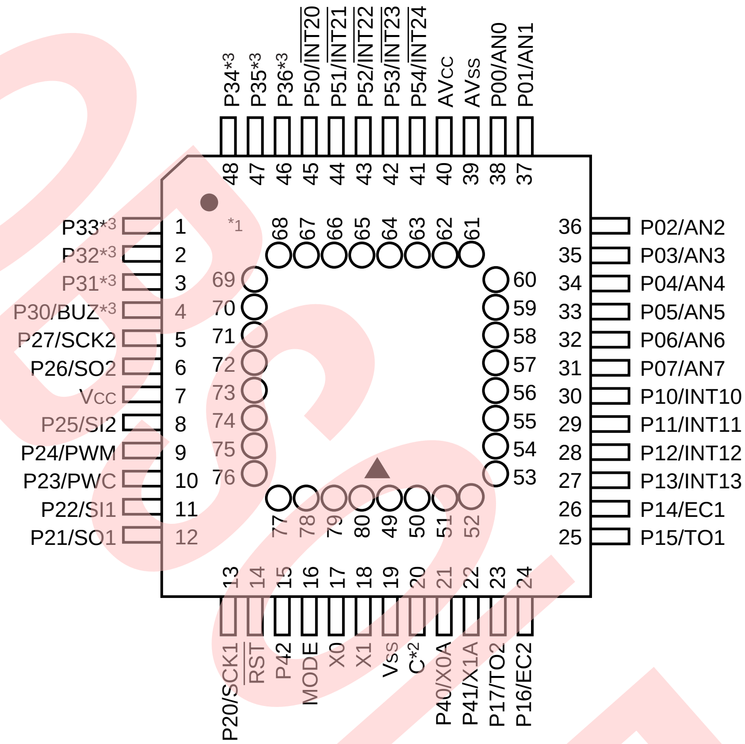
*1 : For pin no. 20, connect this pin to an external 0.1 µF capacitor to ground (for MB89P475 only) .
For MB89PV470 and MB89475, this pin should be left unconnected.

*2 : High current drive type

(Continued)

(Continued)

(TOP VIEW)



(MQP-48C-P01)

*1 : Package upper-side pin assignment (MB89PV470 only)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
49	V_{pp}	57	N.C.	65	O4	73	$\overline{OE}$
50	A12	58	A2	66	O5	74	N.C.
51	A7	59	A1	67	O6	75	A11
52	A6	60	A0	68	O7	76	A9
53	A5	61	O1	69	O8	77	A8
54	A4	62	O2	70	$\overline{CE}$	78	A13
55	A3	63	O3	71	A10	79	A14
56	N.C.	64	V_{ss}	72	N.C.	80	Vcc

N.C. : As connected internally, do not use.

*2 : Pin no. 20 should be left unconnected.

*3 : High current drive type

■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit	Function
LQFP/QFP/ MQFP*2	SDIP*1			
17	47	X0	A	Connection pins for a crystal or other oscillator. An external clock can be connected to X0. In this case, leave X1 open.
18	48	X1		
16	46	MODE	B	Input pins for setting the memory access mode. Connect directly to V_{SS}.
14	44	$\overline{\text{RST}}$	C	Reset I/O pin. The pin is a N-ch open-drain type with pull-up resistor and a hysteresis input. The pin outputs an “L” level when an internal reset request is present. Inputting an “L” level initializes internal circuits.
38 to 31	20 to 13	P00/AN0 to P07/AN7	D	General-purpose I/O port. The pins are shared with the analog inputs for the A/D converter.
30 to 27	12 to 9	P10/INT10 to P13/INT13	E	General-purpose I/O port. A hysteresis input for INT10 to INT13. The pin is shared with an external interrupt 1 input.
26	8	P14/EC1	E	General-purpose I/O port. A hysteresis input for EC1. The pin is shared with the 8/16 bit timer 1 input.
25	7	P15/TO1	F	General-purpose I/O port. The pin is shared with the output of 8/16-bit timer 1.
24	6	P16/EC2	E	General-purpose I/O port. A hysteresis input for EC2. The pin is shared with the 8/16 bit timer 2 input.
23	5	P17/TO2	F	General-purpose I/O port. The pin is shared with the output of 8/16-bit timer 2.
13	43	P20/SCK1	E	General-purpose I/O port. A hysteresis input for SCK1. The pin is shared with the clock I/O of UART/SIO 1.
12	42	P21/SO1	F	General-purpose I/O port. The pin is shared with the serial data output of UART/SIO 1.
11	41	P22/SI1	E	General-purpose I/O port. A hysteresis input for SI1. The pin is shared with the serial data input of UART/SIO 1.
10	40	P23/PWC	E	General-purpose I/O port. A hysteresis input for PWC. This pin is shared with PWC input.
9	39	P24/PWM	F	General-purpose input port. This pin is shared with PWM output.
8	38	P25/SI2	E	General-purpose I/O port. A hysteresis input for SI2. The pin is shared with the serial data input of UART/SIO 2.

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Pin no.		Pin name	I/O circuit	Function
LQFP/QFP/ MQFP*2	**SDIP*1**			
6	36	P26/SO2	F	General-purpose I/O port. The pin is shared with the serial data output of UART/SIO 2.
5	35	P27/SCK2	E	General-purpose I/O port. A hysteresis input for SCK2. The pin is shared with the clock I/O of UART/SIO 2.
4	34	P30/BUZ	G	N-channel open-drain output. The pin is shared with buzzer output.
3 to 1, 48 to 46	33 to 28	P31 to P36	G	N-channel open-drain output.
21	3	P40/X0A	H	General-purpose input port. (single clock system)
			A	Connection pins for a crystal or other oscillator. (dual clock system) An external clock can be connected to X0A. In this case, leave X1A open.
22	4	P41/X1A	H	General-purpose input port. (single clock system)
			A	Connection pins for a crystal or other oscillator. (dual clock system) An external clock can be connected to X0A. In this case, leave X1A open.
15	45	P42	H	General-purpose input port.
45 to 41	27 to 23	P50/$\overline{INT20}$ to P54/$\overline{INT24}$	E	General-purpose I/O port. A hysteresis input for $\overline{INT20}$ to $\overline{INT24}$. The pin is shared with an external interrupt 2 input.
20	2	C	—	Capacitor connection pin *3
7	37	V_{CC}	—	Power supply pin (+5 V) .
19	1	V_{SS}	—	Power supply pin (GND) .
40	22	AV_{CC}	—	A/D converter power supply pin.
39	21	AV_{SS}	—	A/D converter power supply pin. Use at the same voltage level as V_{SS}.

*1 : DIP-48P-M01

*2 : FPT-48P-M26/FPT-48P-M13/MQP-48C-P01

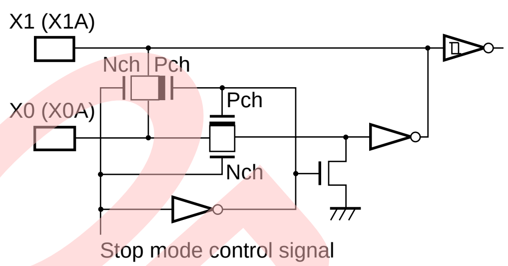
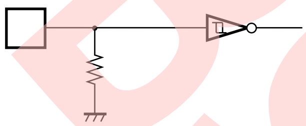
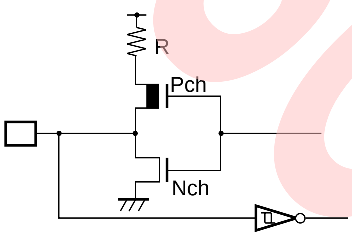
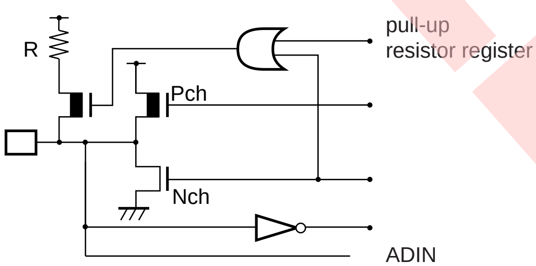
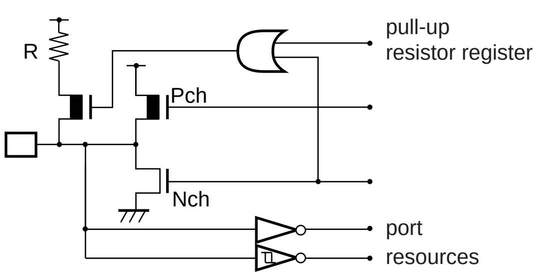
*3 : When MB89475 or MB89PV470 is used, this pin will become a N.C. pin without internal connection.
When MB89P475 is used, connect this pin to an external 0.1 µF capacitor to ground.

- **External EPROM Socket** (**MB89PV470 only**)

Pin no. MQFP*	Pin name	I/O	Function
49	V_{pp}	O	"H" level output pin
50 51 52 53 54 55 58 59 60	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins.
61 62 63	O1 O2 O3	I	Data input pins.
64	V_{SS}	O	Power supply pin (GND) .
65 66 67 68 69	O4 O5 O6 O7 O8	I	Data input pins.
70	$\overline{CE}$	O	Chip enable pin for the ROM. Outputs "H" in standby mode.
71	A10	O	Address output pin.
73	$\overline{OE}$	O	Output enable pin for the ROM. Always outputs "L".
75 76 77 78 79	A11 A9 A8 A13 A14	O	Address output pins.
80	V_{CC}	O	Power supply pin for the EPROM.
56 57 72 74	N.C.	—	Internally connected pins. Always leave open.

* : MQP-48C-P01

■ I/O CIRCUIT TYPE

<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>A</td><td>
</td><td>• Main and sub-clock circuits
• Oscillation feedback resistance is approx. 500 kΩ for main clock circuit and 5 MΩ for sub-clock circuit.</td></tr>
<tr><td>B</td><td></td><td>• Hysteresis input
• The pull-down resistor is approx. 50 kΩ.
(No pull-down resistor in MB89P475)</td></tr>
<tr><td>C</td><td>
</td><td>• The pull-up resistance (P-channel) is approx. 50 kΩ.
• Hysteresis input</td></tr>
<tr><td>D</td><td>
</td><td>• CMOS output
• CMOS input
• Selectable pull-up resistor Approx. 50 kΩ</td></tr>
<tr><td>E</td><td>
</td><td>• CMOS output
• CMOS input
• Selectable pull-up resistor Approx. 50 kΩ</td></tr>
</table>

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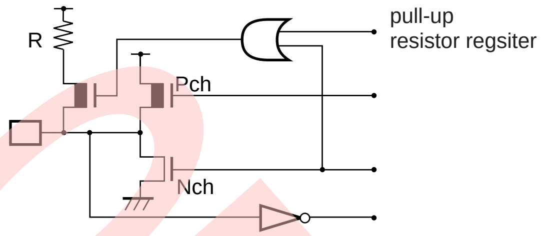
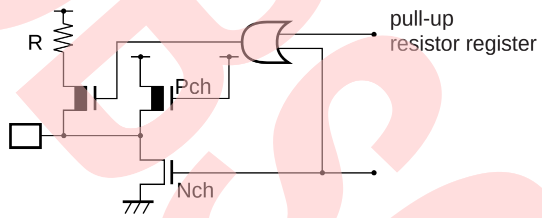
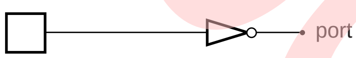
<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>F</td><td></td><td>• CMOS output
• CMOS input
• Selectable pull-up resistor
Approx. 50 kΩ</td></tr>
<tr><td>G</td><td></td><td>• N-channel open-drain output
• Selectable pull-up resistor
Approx. 50 kΩ</td></tr>
<tr><td>H</td><td></td><td>• CMOS input</td></tr>
</table>

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ ELECTRICAL CHARACTERISTICS” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC}) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$ even if the A/D converter is not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

7. Note to noise in the External Reset Pin ($\overline{RST}$)

If the reset pulse applied to the external reset pin ($\overline{RST}$) does not meet the specifications, it may cause malfunctions. Use causion so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{RST}$).

■ PROGRAMMING OTPROM IN MB89P475 WITH SERIAL PROGRAMMER

1. Programming the OTPROM with serial programmer

- All OTP products can be programmed with serial programmer.

2. Programming the OTPROM

- To program the OTPROM using FUJITSU MCU programmer MB91919-001.

Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65) -2810770
FAX (65) -2810220

3. Programming Adapter for OTPROM

- To program the OTPROM using FUJITSU MCU programmer MB91919-001, use the programming adapter listed below.

Package	Compatible socket adapter
DIP-48P-M01	MB91919-805+MB91919-800
FPT-48P-M26	MB91919-806+MB91919-800
FPT-48P-M13	MB91919-807+MB91919-800

Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65) -2810770
FAX (65) -2810220

4. OTPROM Content Protection

For product with OTPROM content protection feature (MB89P475-102, MB89P475-202) , OTPROM content can be read using serial programmer if the OTPROM content protection mechanism is not activated.

One predefined area of the OTPROM ($FFFC_H$) is assigned to be used for preventing the read access of OTPROM content. If the protection code “00_H” is written in this address ($FFFC_H$) , the OTPROM content cannot be read by any serial programmer.

Note : The program written into the OTPROM cannot be verified once the OTPROM protection code is written (“00_H” in $FFFC_H$) . It is advised to write the OTPROM protection code at last.

5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

■ PROGRAMMING OTPROM IN MB89P475 WITH PROGRAMMER

1. Programming OTPROM with parallel programmer

- Only products without protection feature (i.e. MB89P475-101 and MB89P475-201) can be programmed with parallel programmer. Product with protection feature (i.e. MB89P475-102 and MB89P475-202) cannot be programmed with parallel programmer.

2. ROM Writer Adapters and Recommended ROM Writers

- The following shows ROM writer adapters and recommended ROM writers.

Fujitsu Microelectronics Asia Pte Ltd. (Serial programmer)

Package	Applicable adapter model	Recommended writer
DIP-48P-M01	MB91919-601	MB91919-001
FPT-48P-M26	MB91919-602	
FPT-48P-M13	MB91919-603	

Inquiries : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65) -2810770

Writing data to the OTPROM

(1) Set the OTPROM writer for the CU50-OTP (device code : cdB6DC) .

(2) Load the program data to the OTPROM writer.

(3) Write data using the OTPROM writer.

3. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

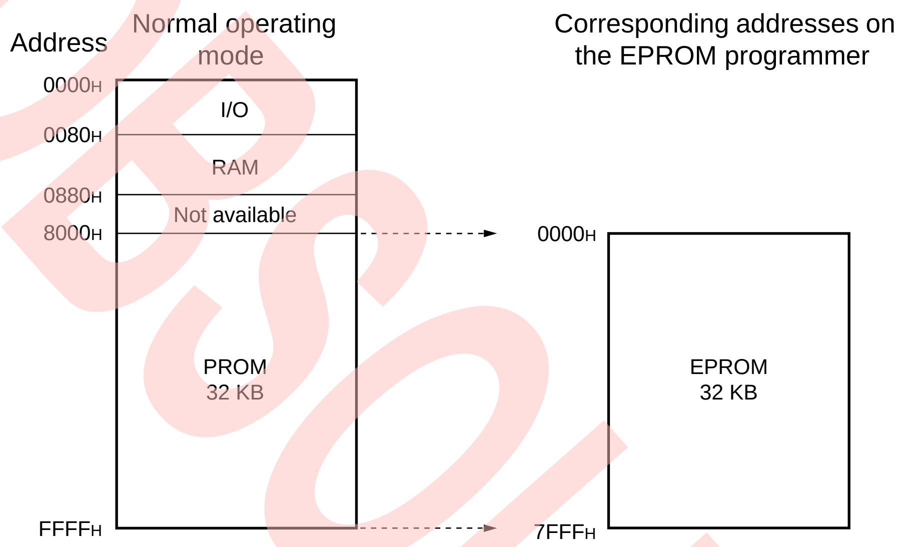
■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

2. Memory Space

Memory space in each mode is diagrammed below.



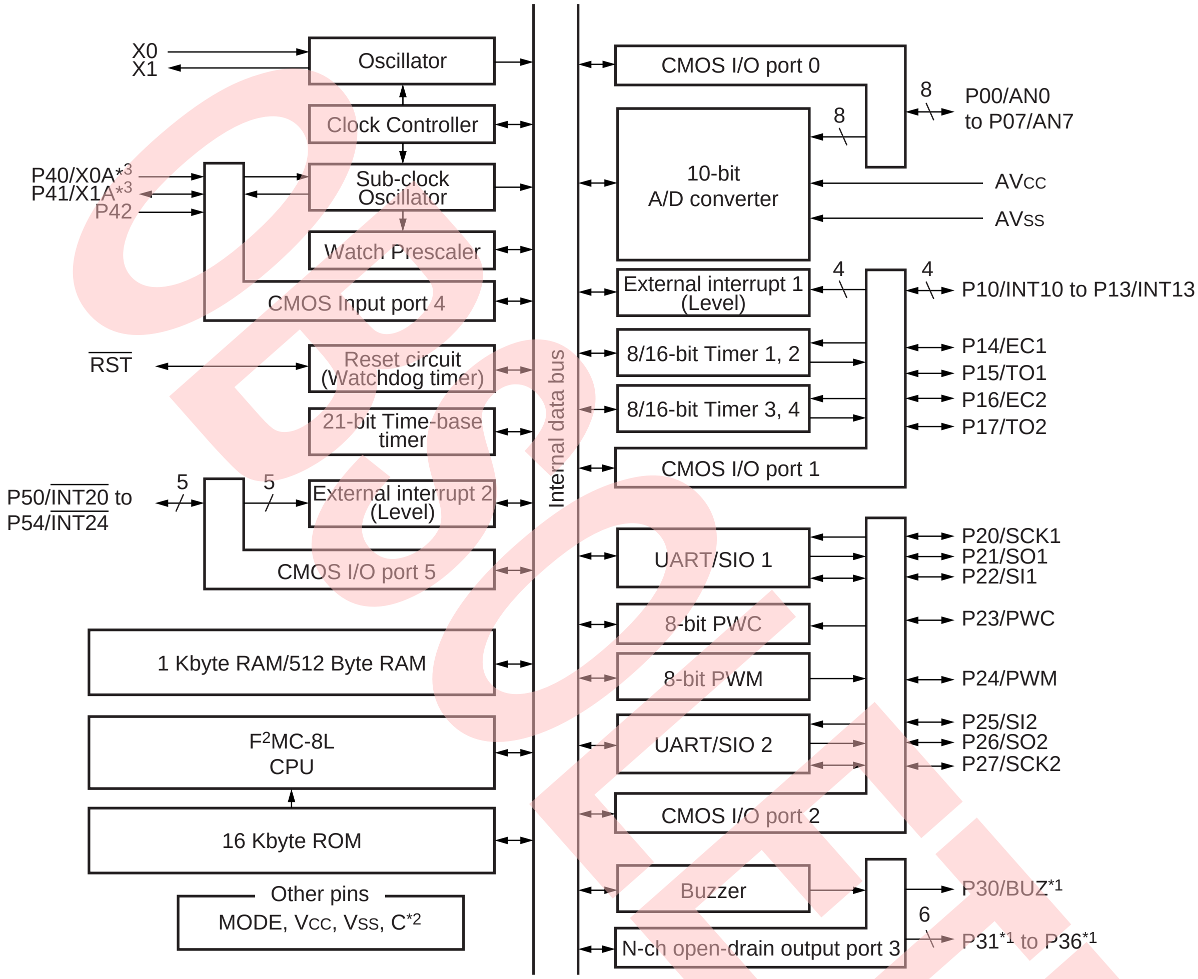
3. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM



*1 : High Current Pins

*2 : Unconnected pin for MB89PV470 and MB89475

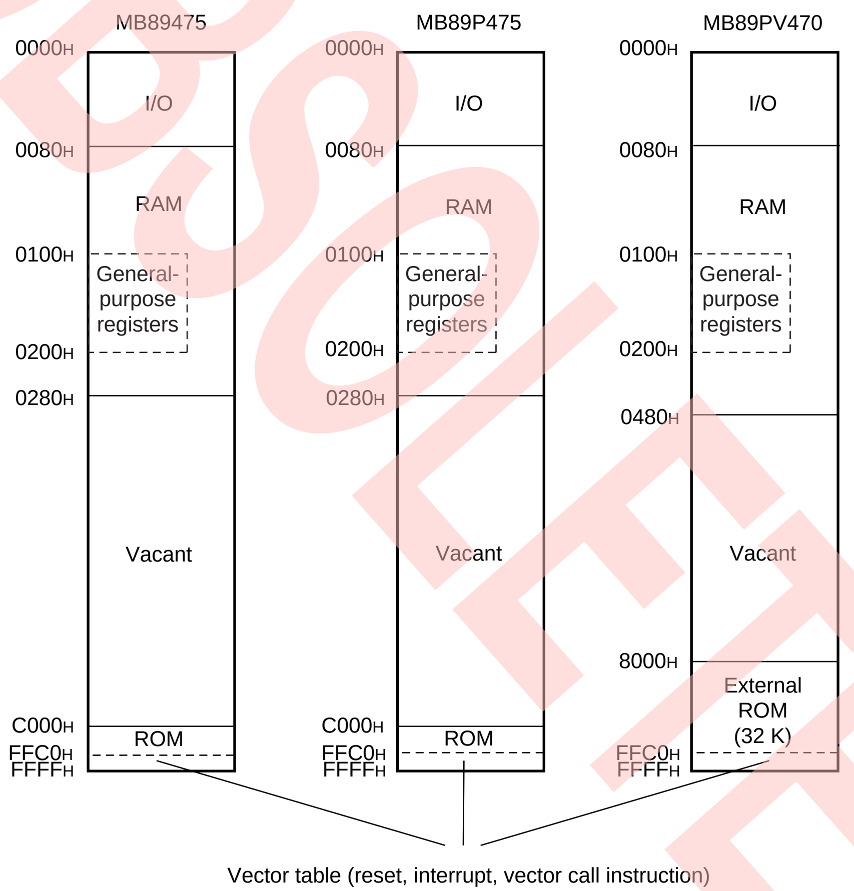
*3 : P40, P41 pins for single-clock system and X01A, X1A pins for dual-clock system

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89470 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89470 series is structured as illustrated below.

Memory Map



2. Registers

The F[2]MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following registers are provided :

Program counter (PC)	:	A 16-bit register for indicating instruction storage positions
Accumulator (A)	:	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T)	:	A 16-bit register which performs arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX)	:	A 16-bit register for index modification
Extra pointer (EP)	:	A 16-bit pointer for indicating a memory address
Stack pointer (SP)	:	A 16-bit register for indicating a stack area
Program status (PS)	:	A 16-bit register for storing a register pointer, a condition code

16 bits		Initial value
PC	: Program counter	FFFDH
A	: Accumulator	Undefined
T	: Temporary accumulator	Undefined
IX	: Index register	Undefined
EP	: Extra pointer	Undefined
SP	: Stack pointer	Undefined
PS	: Program status	I-flag = 0, IL1, 0 = 11 Other bits are undefined.

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR) . (See the diagram below.)

Structure of the Program Status Register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS	RP					Vacancy	Vacancy	Vacancy	H	I	IL1, 0		N	Z	V	C
	RP								CCR							

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area

									RP				Lower OP codes		
	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"	R4	R3	R2	R1	R0	b2	b1	b0
Generated addresses	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag : Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag : Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		↕
1	0	2	
1	1	3	Low = no interrupt

N-flag : Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag : Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag : Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

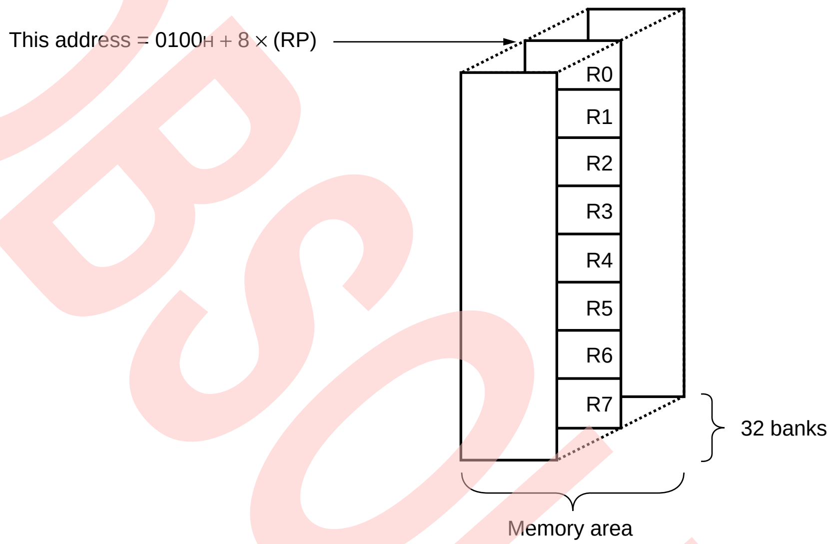
C-flag : Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared other-wise. Set to the shift-out vallue in the case of a shift instruction.

The following general-purpose registers are provided :

General-purpose registers : An 8-bit resister for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB89470 series. The bank currently in use is indicated by the register bank pointer (RP) .

Register Bank Configuration



■ I/O MAP

Address	Register name	Register Description	Read/Write	Initial value
00H	PDR0	Port 0 data register	R/W	XXXXXXXXB
01H	DDR0	Port 0 data direction register	W*	00000000B
02H	PDR1	Port 1 data register	R/W	XXXXXXXXB
03H	DDR1	Port 1 data direction register	W*	00000000B
04H	PDR2	Port 2 data register	R/W	00000000B
05H	(Reserved)			
06H	DDR2	Port 2 data direction register	R/W	00000000B
07H	SYCC	System clock control register	R/W	-XXMM-00B
08H	STBC	Standby control register	R/W	0001XXXXB
09H	WDTC	Watchdog timer control register	W*	0---XXXXB
0AH	TBTC	Timebase timer control register	R/W	00---000B
0BH	WPCR	Watch prescaler control register	R/W	00--0000B
0CH	PDR3	Port 3 data register	R/W	-1111111B
0DH	PDR4	Port 4 data register	R	-----XXXB
0EH	RSFR	Reset flag register	R	XXXX----B
0FH	BUZR	Buzzer register	R/W	-----000B
10H	PDR5	Port 5 data register	R/W	---XXXXXB
11H	DDR5	Port 5 data direction register	R/W	---00000B
12H, 13H	(Reserved)			
14H	T4CR	Timer 4 control register	R/W	000000X0B
15H	T3CR	Timer 3 control register	R/W	000000X0B
16H	T4DR	Timer 4 data register	R/W	XXXXXXXXB
17H	T3DR	Timer 3 data register	R/W	XXXXXXXXB
18H	T2CR	Timer 2 control register	R/W	000000X0B
19H	T1CR	Timer 1 control register	R/W	000000X0B
1AH	T2DR	Timer 2 data register	R/W	XXXXXXXXB
1BH	T1DR	Timer 1 data register	R/W	XXXXXXXXB
1CH to 1FH	(Reserved)			
20H	ADC1	A/D control register 1	R/W	-00000X0B
21H	ADC2	A/D control register 2	R/W	-0000001B
22H	ADDH	A/D data register (Upper byte)	R	------XXB
23H	ADDL	A/D data register (Lower byte)	R	XXXXXXXXB
24H	ADER	A/D input enable register	R/W	11111111B
25H	(Reserved)			
26H	SMC11	UART/SIO serial mode control register 11	R/W	00000000B

(Continued)

(Continued)

Address	Register name	Register Description	Read/Write	Initial value
27H	SMC12	UART/SIO serial mode control register 12	R/W	00000000B
28H	SSD1	UART/SIO serial status and data register 1	R	00001---B
29H	SIDR1/SODR1	UART/SIO serial data register 1	R/W *	XXXXXXXXB
2AH	SRC1	UART/SIO serial rate control register 1	R/W	XXXXXXXXB
2BH	SMC21	UART serial mode control register 21	R/W	00000000B
2CH	SMC22	UART serial mode control register 22	R/W	00000000B
2DH	SSD2	UART serial status and data register 2	R	00001---B
2EH	SIDR2/SODR2	UART serial data register 2	R/W *	XXXXXXXXB
2FH	SRC2	UART serial rate control register 2	R/W	XXXXXXXXB
30H	EIC1	External interrupt 1 control register 1	R/W	00000000B
31H	EIC2	External interrupt 1 control register 2	R/W	00000000B
32H	EIE2	External interrupt 2 enable register	R/W	---00000B
33H	EIF2	External interrupt 2 flag register	R/W	-------0B
34H	PCR1	PWC control register 1	R/W	0-0--000B
35H	PCR2	PWC control register 2	R/W	00000000B
36H	PLBR	PWC reload buffer register	R/W	XXXXXXXXB
37H	(Reserved)			
38H	CNTR	PWM timer control register	R/W	0-00000000B
39H	COMR	PWM timer compare register	W*	XXXXXXXXB
3AH to 6FH	(Reserved)			
70H	PURC0	Port 0 pull up resistor control register	R/W	11111111B
71H	PURC1	Port 1 pull up resistor control register	R/W	11111111B
72H	PURC2	Port 2 pull up resistor control register	R/W	11111111B
73H	PURC3	Port 3 pull up resistor control register	R/W	-1111111B
74H	(Reserved)			
75H	PURC5	Port 5 pull up resistor control register	R/W	---1111B
76H to 7AH	(Reserved)			
7BH	ILR1	Interrupt level setting register 1	W*	11111111B
7CH	ILR2	Interrupt level setting register 2	W*	11111111B
7DH	ILR3	Interrupt level setting register 3	W*	11111111B
7EH	ILR4	Interrupt level setting register 4	W*	11111111B
7FH	(Reserved)			

* : Bit manipulation instruction cannot be used.

- **Read/write access symbols**

  R/W : Readable and writable
  R : Read-only
  W : Write-only

- **Initial value symbols**

  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.
  \- : Unused bit.
  M : The initial value of this bit is determined by mask option.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	AV_{CC} must not exceed V_{CC}
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
"L" level maximum output current	I_{OL}	—	15	mA	
"L" level average output current	I_{OLAV1}	—	4	mA	Average value (operating current × operating rate) P00 to P07, P10 to P17, P20 to P27, P50 to P54, $\overline{RST}$
	I_{OLAV2}	—	12	mA	Average value (operating current × operating rate) P30 to P36
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	40	mA	Average value (operating current × operating rate)
"H" level maximum output current	I_{OH}	—	–15	mA	
"H" level average output current	I_{OHAV}	—	–2	mA	Average value (operating current × operating rate)
"H" level total maximum output current	ΣI_{OH}	—	–50	mA	
"H" level total average output current	ΣI_{OHAV}	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

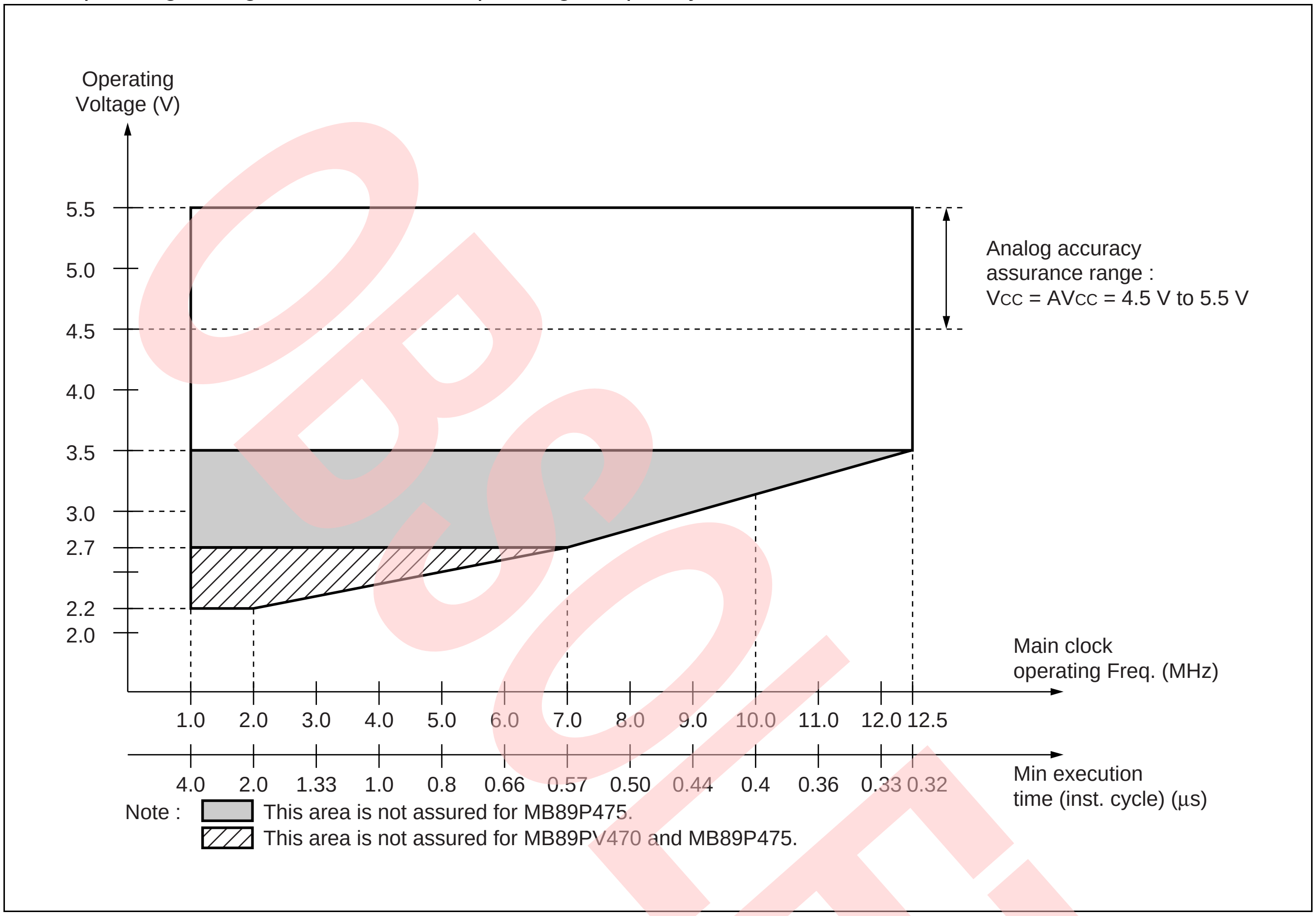
2. Recommended Operating Conditions

($AV_{SS} = V_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC} AV_{CC}	2.2*	5.5	V	Operation assurance range	MB89475
		3.5*	5.5	V	Operation assurance range	MB89P475
		2.7*	5.5	V	Operation assurance range	MB89PV470
		1.5	5.5	V	Retains the RAM state in stop mode	
Operating temperature	T_A	–40	+85	°C		

* : These values depend on the operating conditions and the analog assurance range. See “Operating Voltage vs. Main Clock Operating Frequency” and “5. A/D Converter Electrical Characteristics.”

• Operating Voltage vs. Main Clock Operating Frequency



“Operating Voltage vs. Main Clock Operating Frequency” indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_{CH}.
Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

($AV_{CC} = V_{CC} = 5.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27, P40 to P42, P50 to P54	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{\text{RST}}$, MODE, EC1, EC2, SCK1, SI1, SCK2, SI2, PWC, $\overline{\text{INT10}}$ to $\overline{\text{INT13}}$, $\overline{\text{INT20}}$ to $\overline{\text{INT24}}$	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27, P40 to P42, P50 to P54	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{\text{RST}}$, MODE, EC1, EC2, SCK1, SI1, SCK2, SI2, PWC, $\overline{\text{INT10}}$ to $\overline{\text{INT13}}$, $\overline{\text{INT20}}$ to $\overline{\text{INT24}}$	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P30 to P36	—	V_{SS} − 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P50 to P54	$I_{OH} = -2.0$ mA	4.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P27, P50 to P54, $\overline{\text{RST}}$	$I_{OL} = 4.0$ mA	—	—	0.4	V	
	V_{OL2}	P30 to P36	$I_{OL} = 12.0$ mA	—	—	0.4	V	
Input leakage current	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P50 to P54	0.45 V < V_I < V_{CC}	−5	—	+5	µA	Without pull-up resistor
Open drain output leakage current	I_{LOD}	P30 to P36	0.45 V < V_I < V_{CC}	−5	—	+5	µA	

(Continued)

(Continued)

($AV_{CC} = V_{CC} = 5.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-down resistance	R_{DOWN}	MODE	$V_I = V_{CC}$	25	50	100	kΩ	Except MB89P475
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P30 to P36, P50 to P54, $\overline{RST}$	$V_I = 0.0$ V	25	50	100	kΩ	When pull-up resistor is selected (except $\overline{RST}$)
Power supply current	I_{CC1}	V_{CC}	$F_{CH} = 12.5$ MHz $t_{inst} = 0.32$ µs Main clock run mode	—	7	13	mA	
	I_{CC2}		$F_{CH} = 12.5$ MHz $t_{inst} = 5.12$ µs Main clock run mode	—	1	3	mA	
	I_{CCS1}		$F_{CH} = 12.5$ MHz $t_{inst} = 0.32$ µs Main clock sleep mode	—	2.5	5	mA	
	I_{CCS2}		$F_{CH} = 12.5$ MHz $t_{inst} = 5.12$ µs Main clock sleep mode	—	0.7	2	mA	
	I_{CCL}		F_{CL} = 32.768 kHz Subclock mode	—	37	85	µA	MB89PV470 MB89475
				—	350	785	µA	MB89P475
	I_{CCLS}		F_{CL} = 32.768 kHz Subclock sleep mode	—	11	30	µA	
	I_{CCT}		F_{CL} = 32.768 kHz Watch mode Main clock stop mode	—	1.4	15	µA	MB89PV470 MB89475
				—	5.6	21	µA	MB89P475
	I_{CCH}		Ta = +25 °C Subclock stop mode		1	10	µA	
	I_A	AV_{CC}	$F_{CH} = 12.5$ MHz	—	2.8	6	mA	A/D converting
	I_{AH}		Ta = +25 °C	—	1	5	µA	A/D stop
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}, AV_{CC}, AV_{SS}	f = 1 MHz	—	5	15	pF	

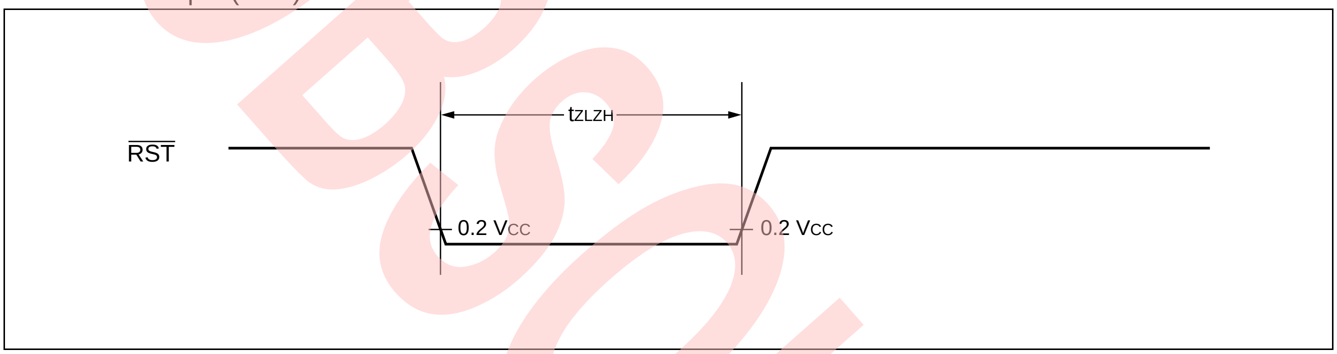
4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

Notes : • t_{HCYL} is the oscillation cycle ($1/F_C$) to input to the X0 pin.
• If the reset pulse applied to the external reset pin ($\overline{RST}$) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{RST}$).

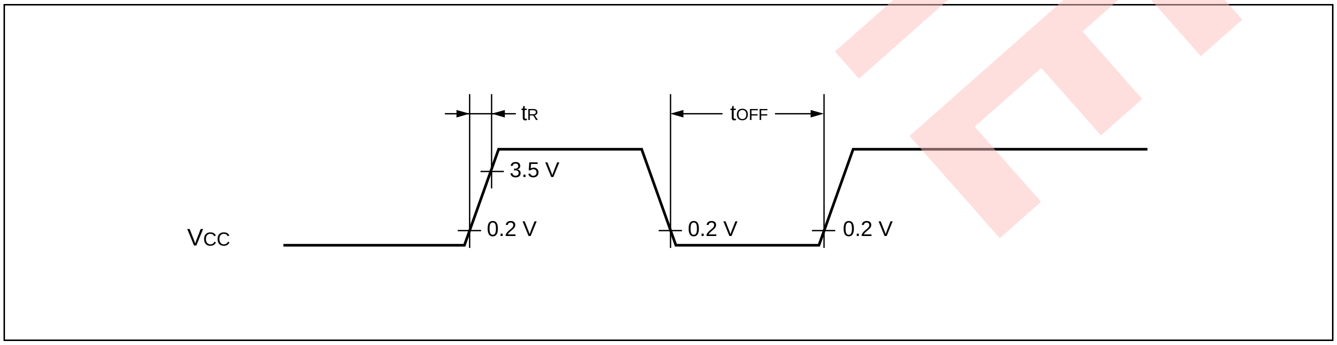


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note : Make sure that power supply rises within the selected oscillation stabilization time.
Rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

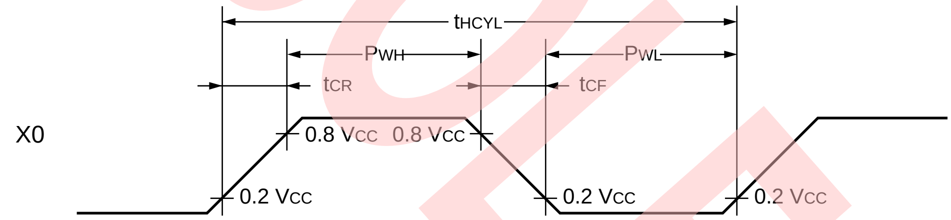


(3) Clock Timing

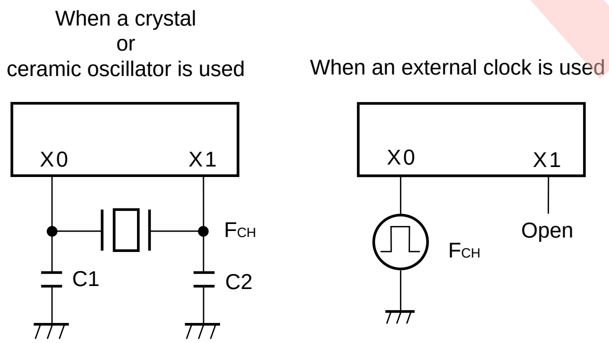
($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to $+85$ °C)

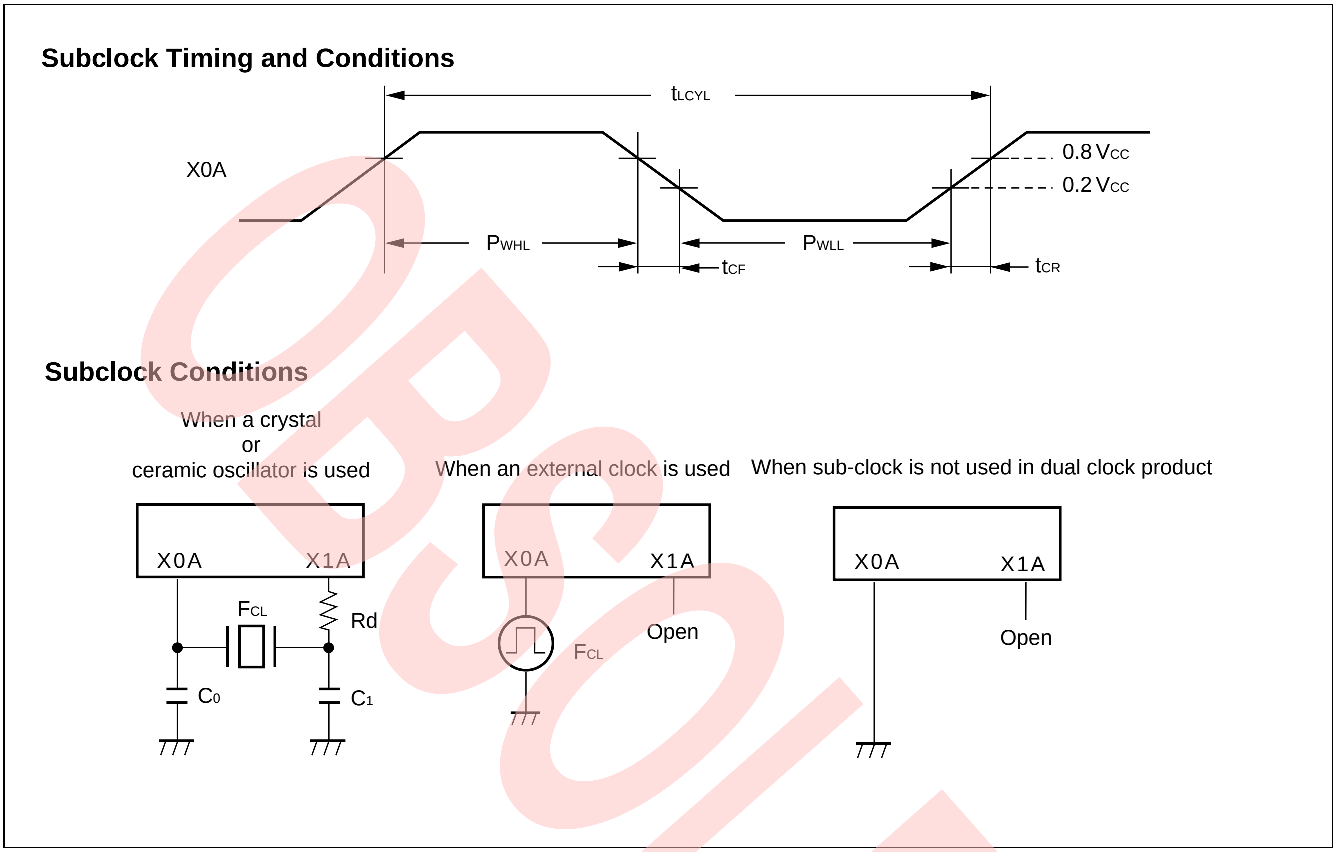
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	1	—	12.5	MHz	
	F_{CL}	X0A, X1A	—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1	80	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0	20	—	—	ns	External clock
	P_{WHL} P_{WLL}	X0A	—	15.2	—	µs	
Input clock rising/falling time	t_{CR} t_{CF}	X0, X0A	—	—	10	ns	

X0 and X1 Timing and Conditions



Main Clock Conditions





(4) Instruction Cycle

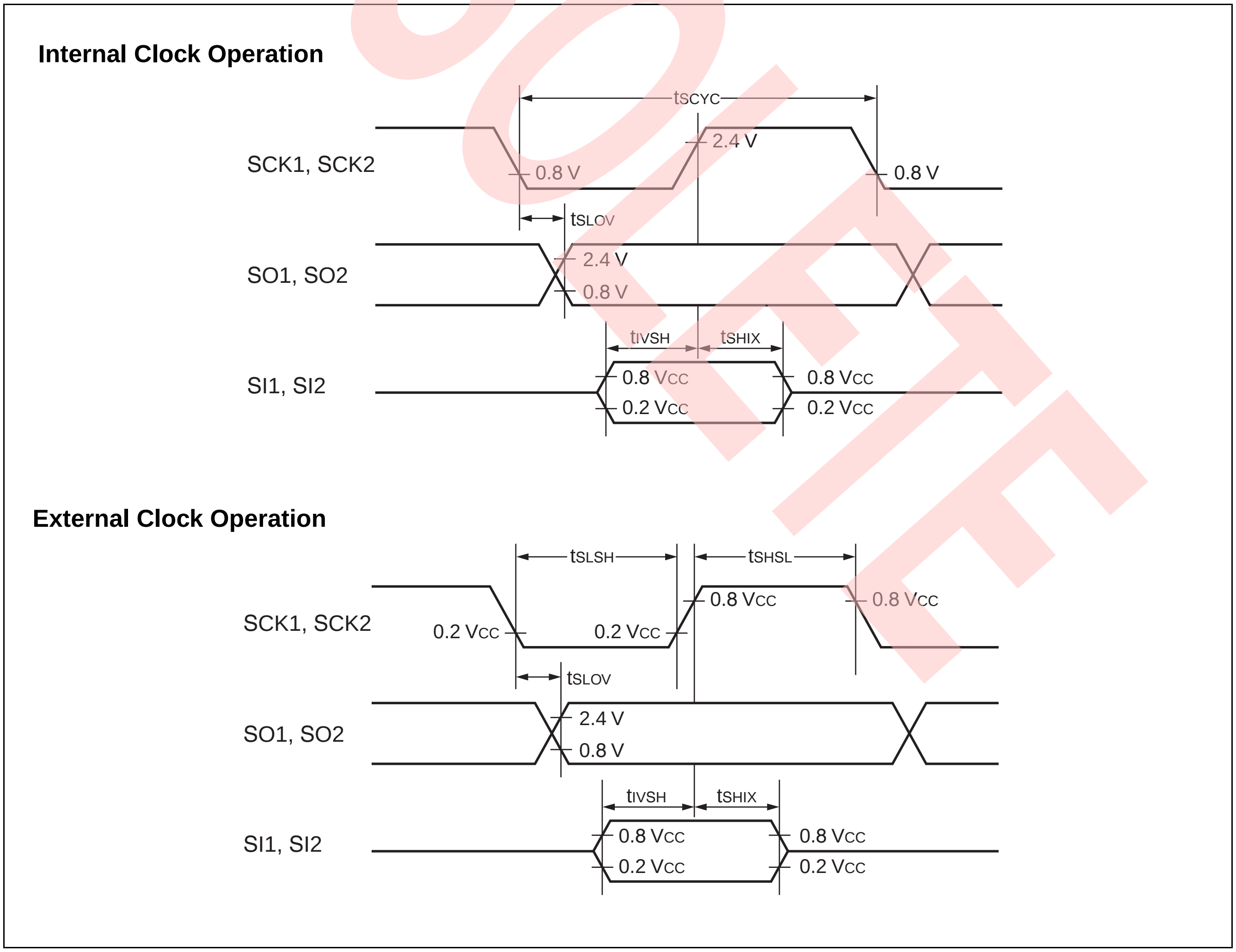
Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})$ $t_{inst} = 0.32$ µs when operating at $F_{CH} = 12.5$ MHz
		$2/F_{CL}$	µs	$t_{inst} = 61.036$ µs when operating at $F_{CL} = 32.768$ kHz

(5) Serial I/O Timing

(V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK1, SCK2	Internal shift clock mode	2 t_{inst}*	—	µs
SCK ↓ → SO time	t_{SLOV}	SCK1, SO1, SCK2, SO2		−200	+200	ns
Valid SI → SCK ↑	t_{IVSH}	SI1, SCK1, SI2, SCK2		1/2 t_{inst}*	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}	SCK1, SI1, SCK2, SI2		1/2 t_{inst}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK1, SCK2	External shift clock mode	1 t_{inst}*	—	µs
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs
SCK ↓ → SO time	t_{SLOV}	SCK1, SO1, SCK2, SO2		0	200	ns
Valid SI → SCK ↑	t_{IVSH}	SI1, SCK1, SI2, SCK2		1/2 t_{inst}*	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}	SCK1, SI1, SCK2, SI2		1/2 t_{inst}*	—	ns

* : For information on t_{inst}, see “ (4) Instruction Cycle.”

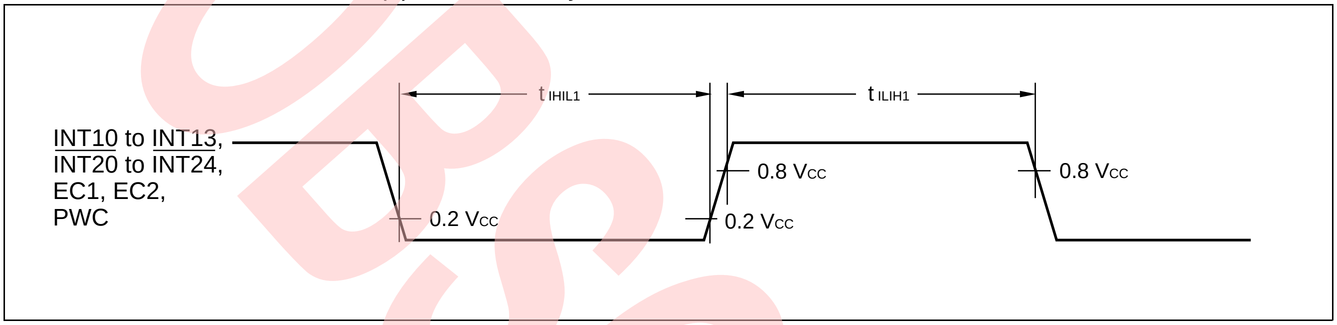


(6) Peripheral Input Timing

($AV_{CC} = V_{CC} = 5.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to +85 °C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Peripheral input “H” pulse width 1	t_{ILIH1}	$\overline{\text{INT10}}$ to $\overline{\text{INT13}}$, $\overline{\text{INT20}}$ to $\overline{\text{INT24}}$, EC1, EC2, PWC	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “ (4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

(1) A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC} = 4.5$ V to 5.5 V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to +85 °C)

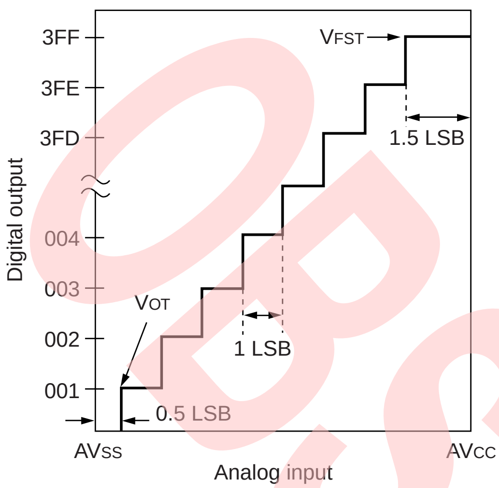
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	10	—	bit	
Total error			—	—	±4.0	LSB	
Linearity error			—	—	±2.5	LSB	
Differential linearity error			—	—	±1.9	LSB	
Zero transition voltage	V_{OT}		AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}		AV_{CC} – 4.5 LSB	AV_{CC} – 2.5 LSB	AV_{CC} – 0.5 LSB	V	
A/D mode conversion time	—		—	—	60 t_{inst}*	µs	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}		AV_{SS}	—	AV_{CC}	V	

* : For information on t_{inst}, see “ (4) Instruction Cycle” in “4. AC Characteristics”.

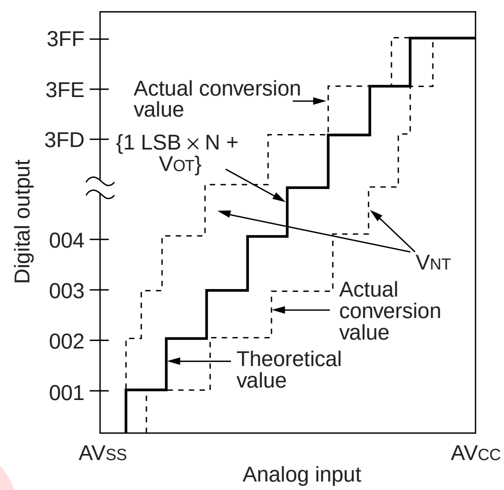
(2) A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics.
- Differential linearity error (unit : LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
- Total error (unit : LSB)
  The difference between theoretical and actual conversion values.

Theoretical I/O characteristics



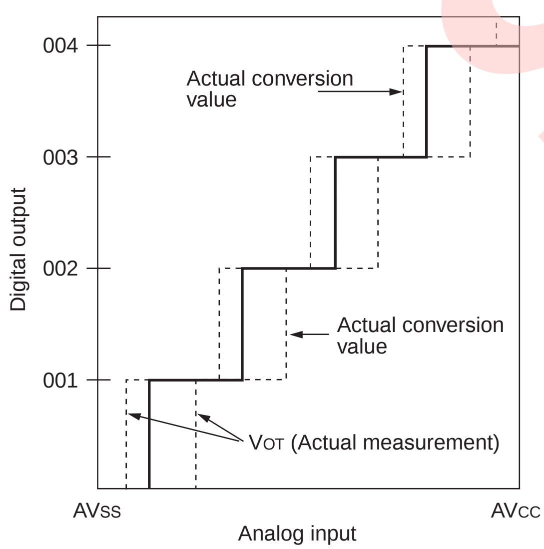
Total error



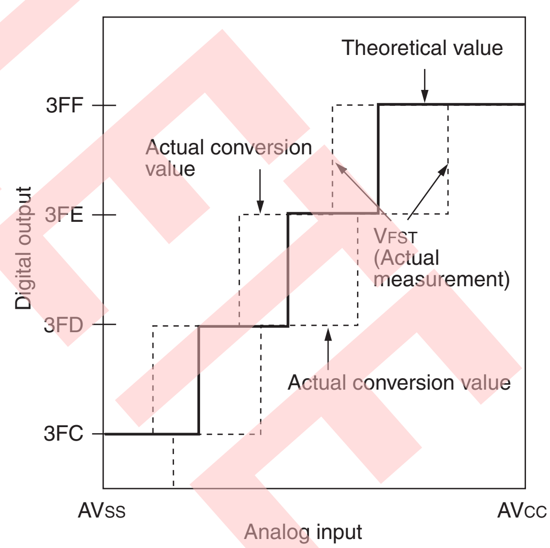
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ (\text{V})$$

$$\text{Total error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

Zero transition error



Full-scale transition error



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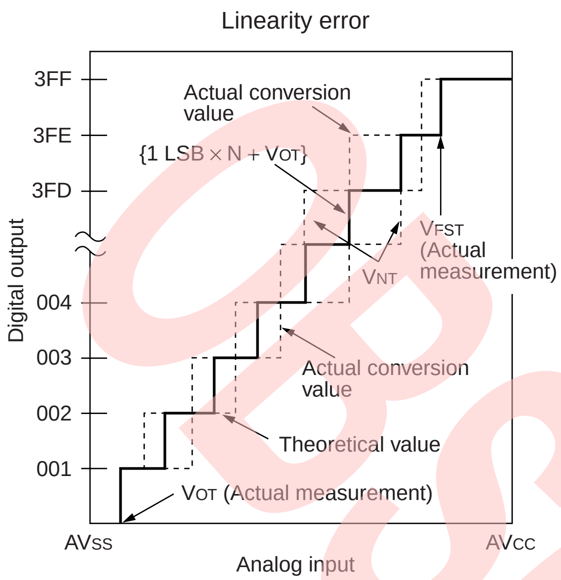

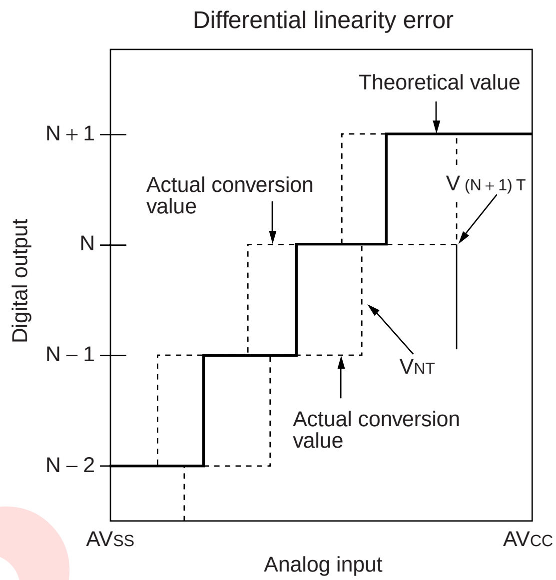

$$\text{Linearity error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

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(3) Notes on Using A/D Converter

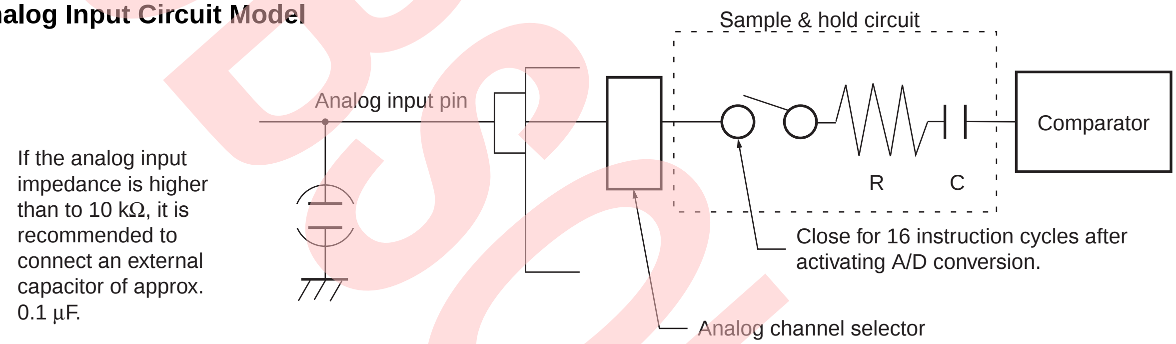
- Input impedance of the analog input pins

  The A/D converter used for the MB89470 series contains a sample & hold circuit as illustrated below to fetch analog input voltage into the sample & hold capacitor for 16 instruction cycles after activation A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low.

  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 µF for the analog input pin.

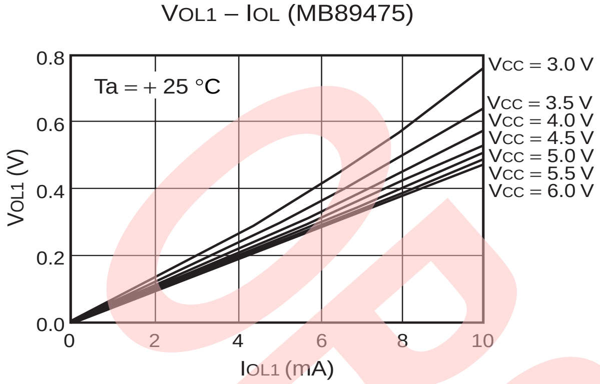
Analog Input Circuit Model

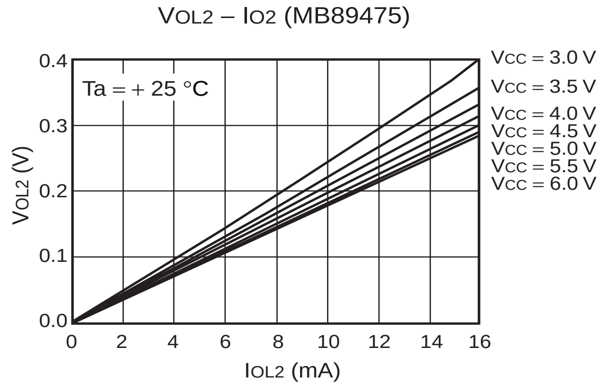


Sample & hold circuit	MB89475 MB89PV470	MB89P475
R : analog input equivalent resistance	2.2 kΩ	2.6 kΩ
C : analog input equivalent capacitance	45 pF	28 pF

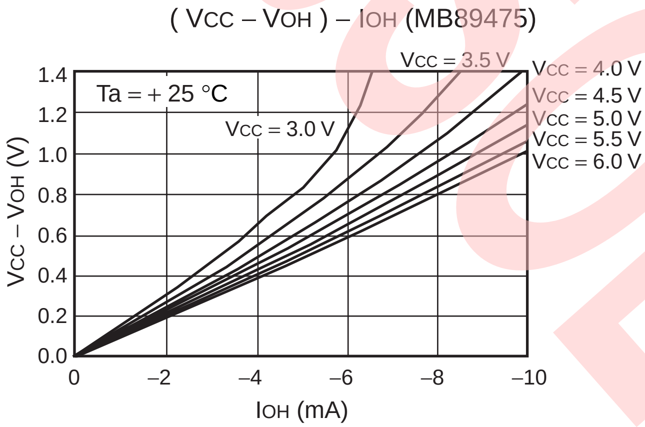
■ EXAMPLE CHARACTERISTICS

• "L" level output voltage

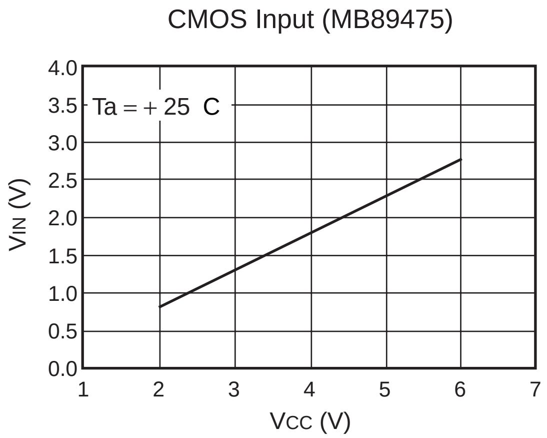


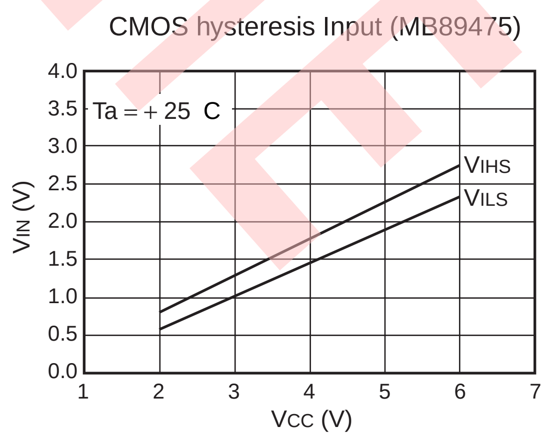


• "H" level output voltage



• "H" level input voltage/"L" level input voltage

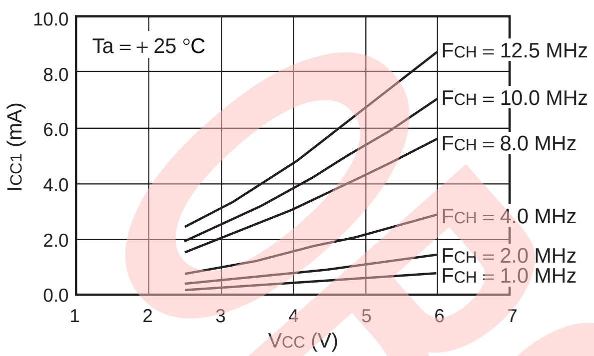




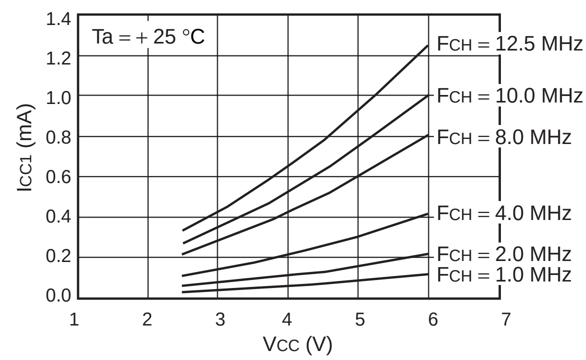
V_{IHS} : Threshold when input voltage in hysteresis characteristics is set to "H" level.
V_{ILS} : Threshold when input voltage in hysteresis characteristics is set to "L" level.

• Power supply current (External clock)

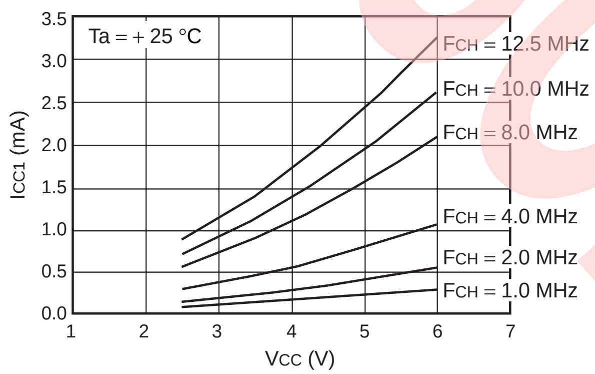
ICC1 – VCC (MB89475)



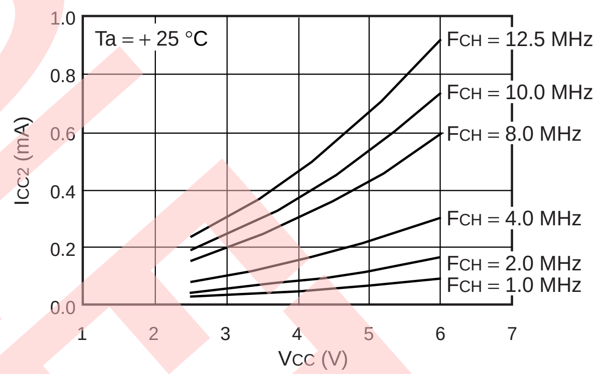
ICC2 – VCC (MB89475)



ICCS1 – VCC (MB89475)



ICCS2 – VCC (MB89475)



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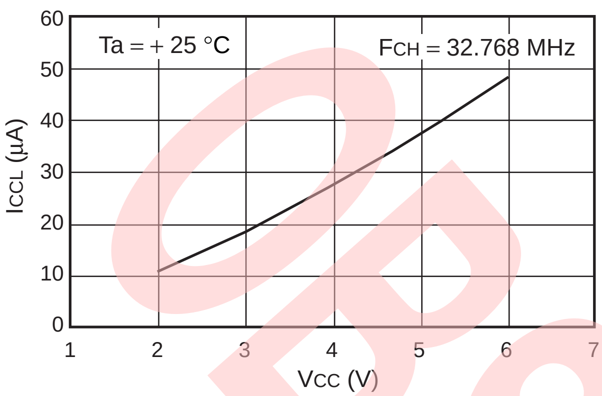
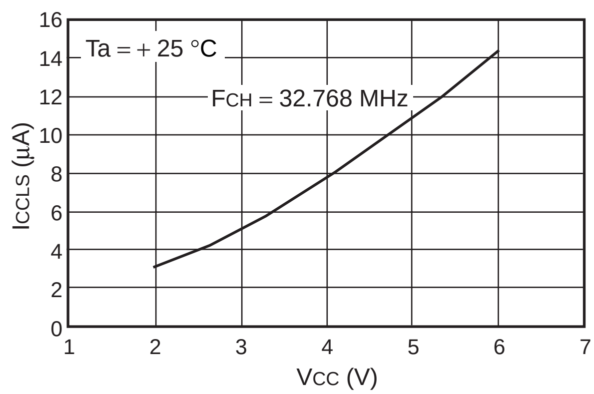
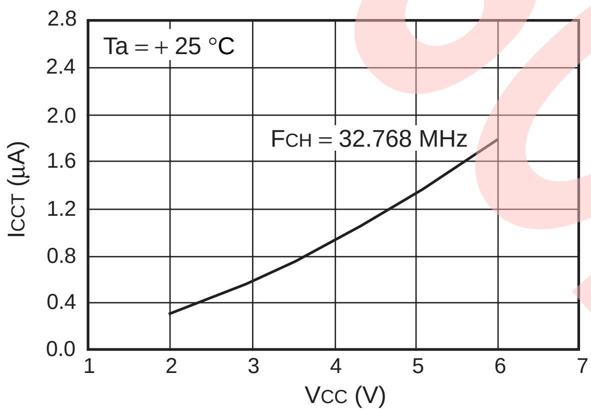
ICCL – VCC (MB89475)



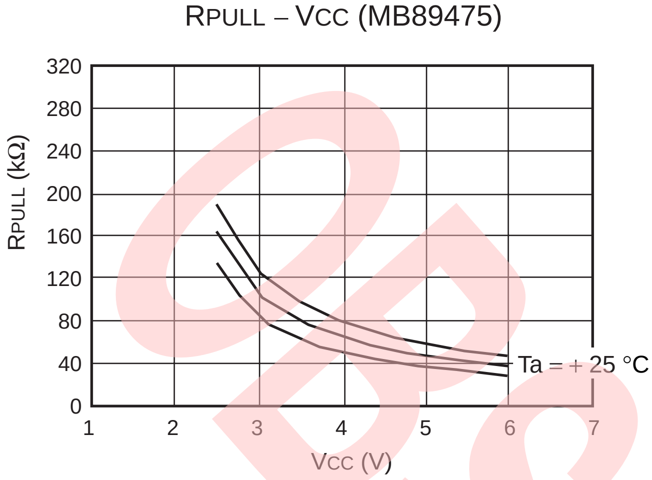
ICCLS – VCC (MB89475)



ICCT – VCC (MB89475)



• Pull-up resistance



■ MASK OPTIONS

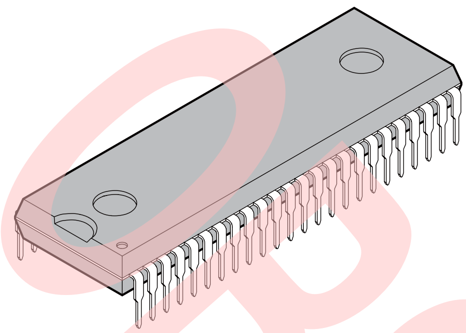
No.	Part number	MB89475	MB89P475	MB89PV470
	Specifying procedure	Specify when ordering mask	Setting not possible	Setting not possible
1	Selection of clock mode • Single clock mode • Dual clock mode	Selectable	101/102 : Single clock 201/202 : Dual clock	101 : Single clock 201 : Dual clock
2	Selection of oscillation stabilization time (OSC) • The initial value of the oscillation stabilization time for the main clock can be set by selecting the values of the WTM1 and WTM0 bits on the right.	Selectable OSC 1 : $2^{14}/F_{CH}$ 2 : $2^{17}/F_{CH}$ 3 : $2^{18}/F_{CH}$	Fixed to oscillation stabilization time of $2^{18}/F_{CH}$	Fixed to oscillation stabilization time of $2^{18}/F_{CH}$
3	Selection of power-on stabilization time • Nil • $2^{17}/F_{CH}$	Selectable	Fixed to power-on stabilization time of $2^{17}/F_{CH}$	Fixed to nil

■ ORDERING INFORMATION

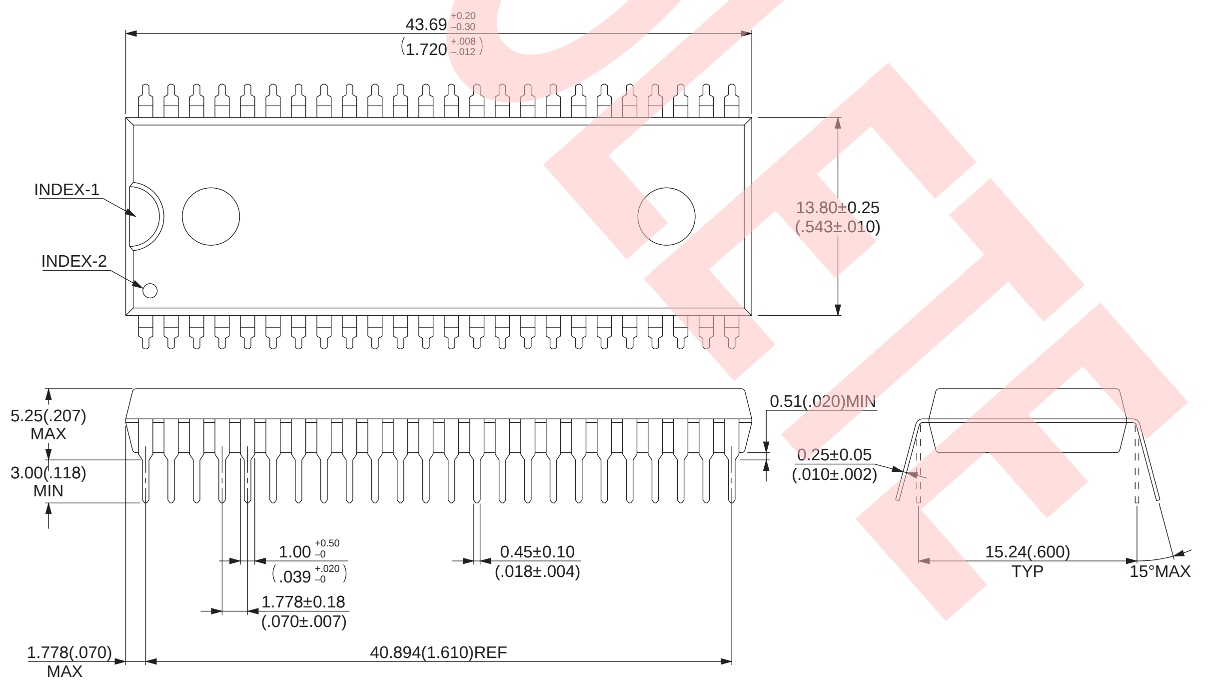
Part number	Package	Remarks
MB89475PFM MB89P475-101PFM MB89P475-102PFM MB89P475-201PFM MB89P475-202PFM	48-pin Plastic QFP (FPT-48P-M13)	101 : Single clock, without content protection 102 : Single clock, with content protection 201 : Dual clock, without content protection 202 : Dual clock, with content protection
MB89475PMC MB89P475-101PMC MB89P475-102PMC MB89P475-201PMC MB89P475-202PMC	48-pin Plastic LQFP (FPT-48P-M26)	
MB89475P-SH MB89P475-101P-SH MB89P475-102P-SH MB89P475-201P-SH MB89P475-202P-SH	48-pin Plastic SH-DIP (DIP-48P-M01)	
MB89PV470-101CF MB89PV470-201CF	48-pin Ceramic MQFP (MQP-48C-P01)	

■ PACKAGE DIMENSIONS

48-pin plastic SH-DIP	Lead pitch	1.778mm(70mil)
	Row spacing	15.24mm(600mil)
	Sealing method	Plastic mold
(DIP-48P-M01)		



48-pin plastic SH-DIP
(DIP-48P-M01)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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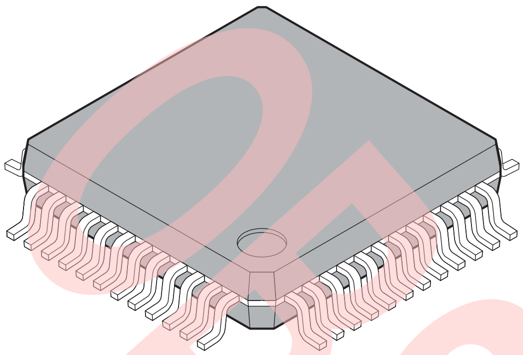
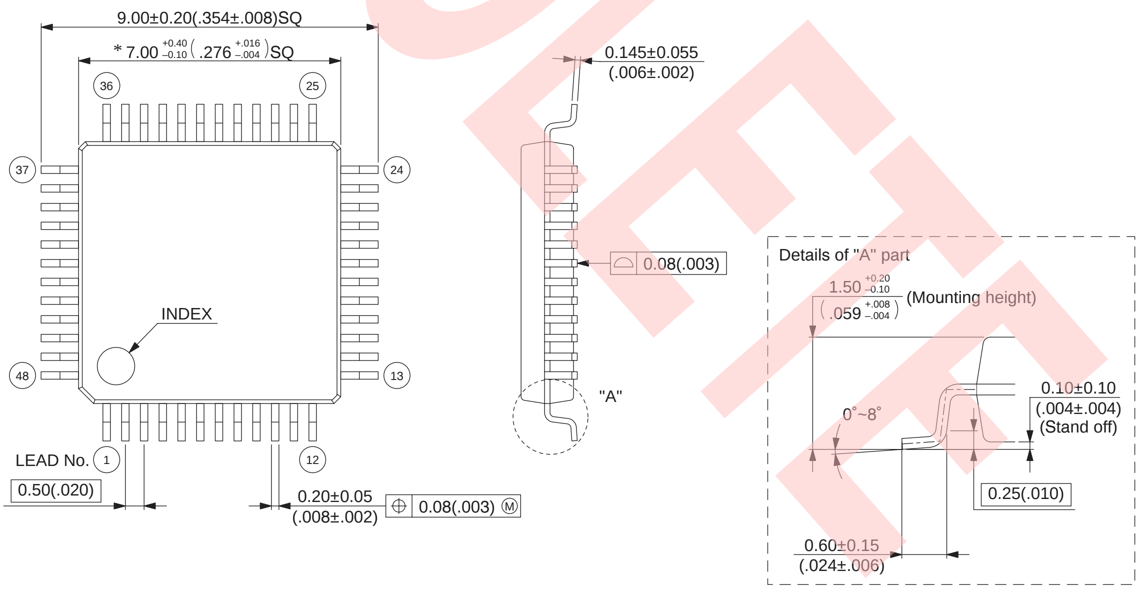
48-pin plastic LQFP	Lead pitch	0.50 mm
	Package width × package length	7 × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
(FPT-48P-M26)	Code (Reference)	P-LFQFP48-7×7-0.50

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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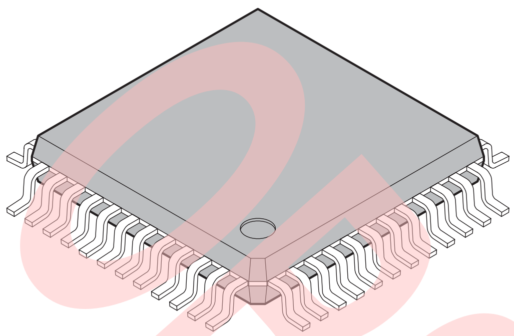
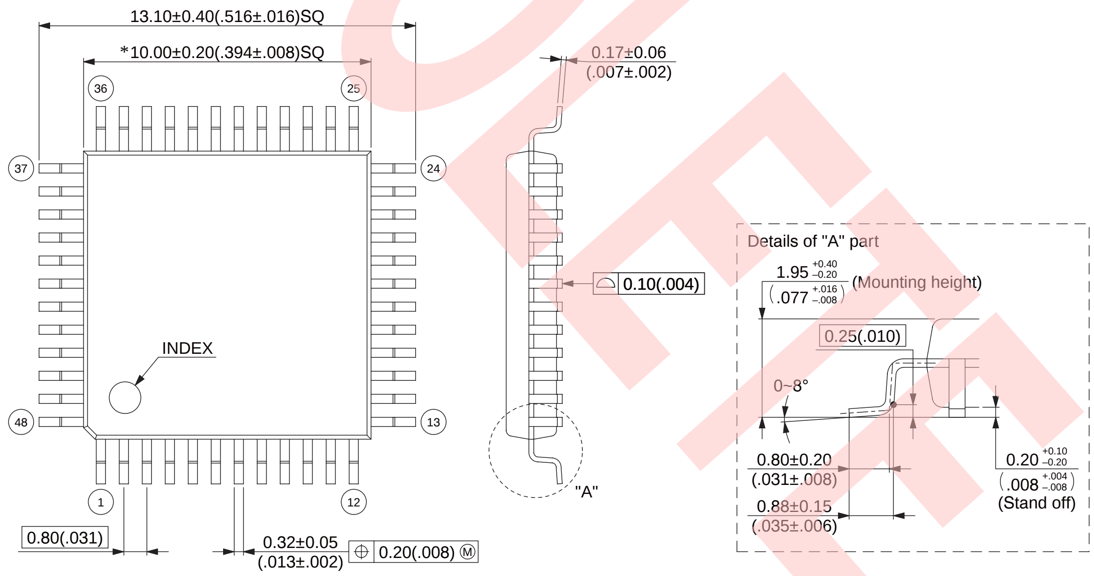
48-pin plastic QFP	Lead pitch	0.80 mm
	Package width × package length	10 × 10 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	2.35 mm MAX
	Code (Reference)	P-QFP44-10×10-0.80
(FPT-48P-M13)		

48-pin plastic QFP
(FPT-48P-M13)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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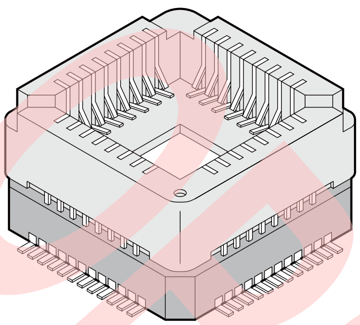
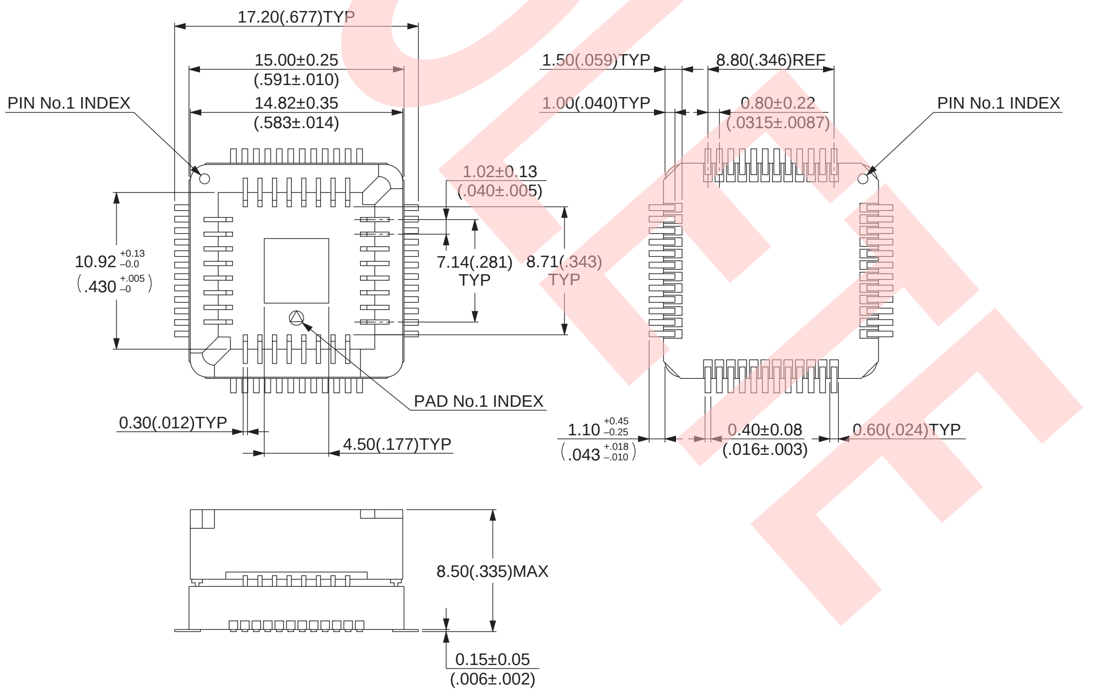
48-pin ceramic MQFP	Lead pitch	0.8 mm
	Lead shape	Straight
	Motherboard material	Ceramic
	Mounted package material	Plastic
(MQP-48C-P01)		

48-pin ceramic MQFP
(MQP-48C-P01)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Changed the package code. FPT-48P-M05 → FPT-48P-M26
15	■ PROGRAMMING OTPROM IN MB89P475 WITH PROGRAMMER	Changed the "2. ROM Writer Adapters and Recommended ROM Writers".
16	■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE	Deleted the “2. Programming Socket Adapter”
43	■ ORDERING INFORMATION	Order informations are changed. MB89475PFV → MB89475PMC MB89P475-101PFV → MB89P475-101PMC MB89P475-102PFV → MB89P475-102PMC MB89P475-201PFV → MB89P475-201PMC MB89P475-202PFV → MB89P475-202PMC
45	■ PACKAGE DIMENSIONS	Changed the package figure. FPT-48P-M05 → FPT-48P-M26

The vertical lines marked in the left side of the page show the changes.

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