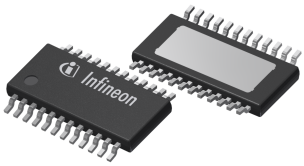
# LITIX™ Power H-Bridge DC-DC controller



RoHS

AEC Qualified

## Features

- Single inductor high power buck-boost controller
- Switching frequency range from 200 kHz to 700 kHz
- Maximum efficiency in every condition (up to 96%)
- Constant current (LED) and constant voltage regulation
- EMC optimized device: spread spectrum always activated
- Overvoltage, shorted LED fault and overtemperature diagnostic output
- Enhanced dimming features: Analog and PWM dimming (from digital input or sourced by embedded PWM engine)
- LED current accuracy ± 3%

## Potential applications

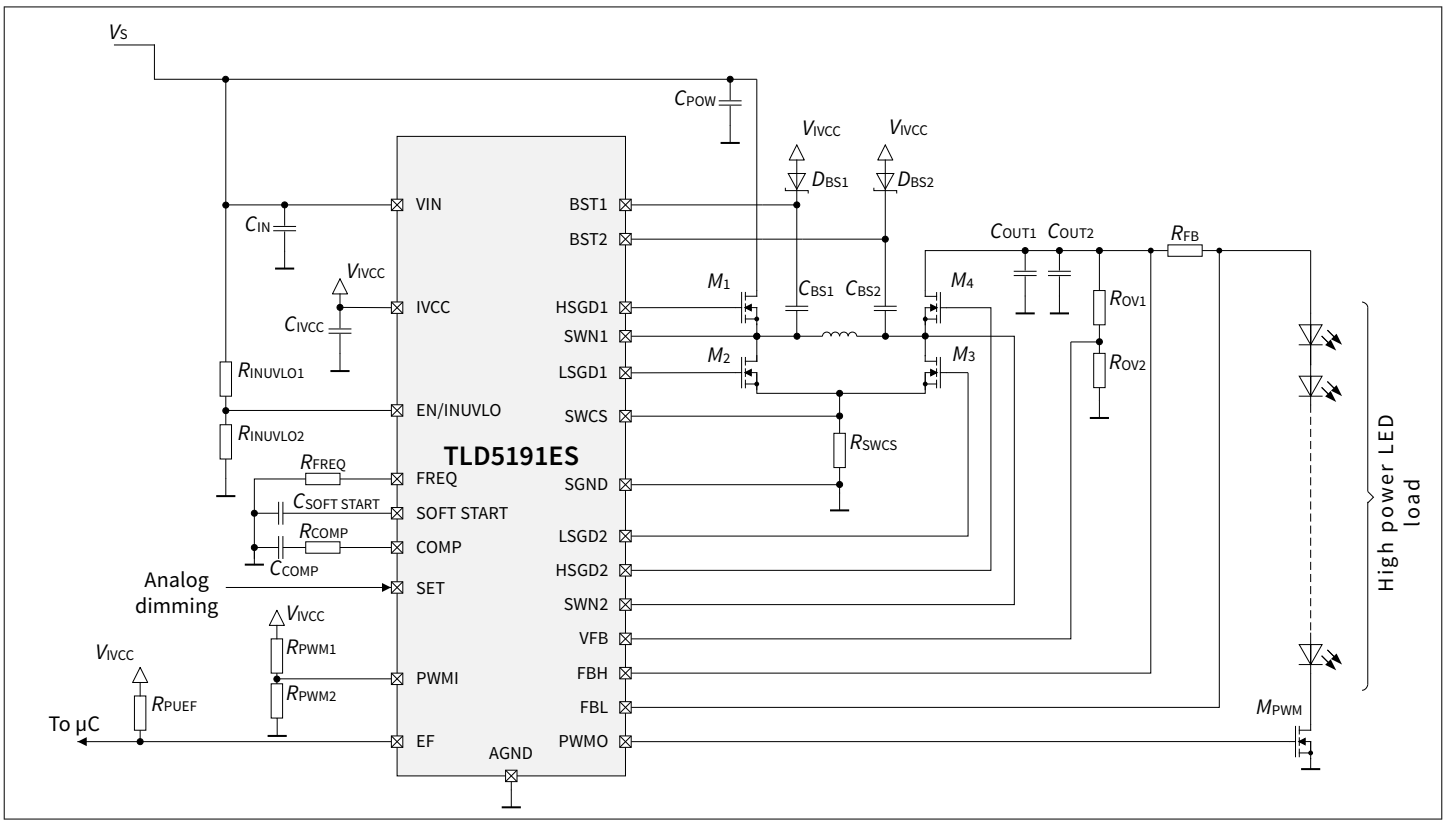
- Especially designed for driving high power LEDs in automotive applications
- Automotive exterior lighting: full LED headlamp assemblies (low beam, high beam, matrix beam, pixel light)
- Voltage pre-regulator for rear lamp assemblies
- General purpose DC-DC for constant current or constant voltage applications

## Product validation

Product validation according to AEC-Q100, Grade1. Qualified for automotive applications.

## Description

The TLD5191ES is a synchronous MOSFET H-Bridge DC-DC controller with built-in protection features. This concept is beneficial for driving high power LEDs with maximum system efficiency and minimum number of external components. The TLD5191ES offers analog and digital (PWM) dimming and embedded PWM engine. The switching frequency is adjustable in the range of 200 kHz to 700 kHz. A built-in spread spectrum switching frequency modulation and the forced continuous current regulation mode improve the overall EMC behavior. Furthermore the current mode regulation scheme provides a stable regulation loop maintained by small external compensation components. The adjustable soft start feature limits the current peak as well as voltage overshoot at start-up. The TLD5191ES is suitable for use in the automotive environment.



| Parameter | Symbol | Values |
|---|---|---|
| Power stage input voltage range | $V_{POW}$ | 4.5 V … 55 V |
| Device input supply voltage range | $V_{VIN}$ | 4.5 V … 40 V |
| Maximum output voltage (depending on the application conditions) | $V_{OUT(max)}$ | 55 V as LED driver boost mode<br>50 V as LED driver buck mode<br>50 V as voltage regulator |
| Switching frequency range | $f_{SW}$ | 200 kHz … 700 kHz |
| Typical H-Bridge NMOS driver on-state resistance at $T_J$ = 25°C (Gate pull-up) | $R_{DS(ON\_PU)}$ | 2.3 Ω |
| Typical H-Bridge NMOS driver on-state resistance at $T_J$ = 25°C (Gate pull-down) | $R_{DS(ON\_PD)}$ | 1.2 Ω |

**Protective functions**

- Overload protection of external MOSFETs
- Shorted load, output overvoltage protection
- Input undervoltage protection
- Thermal shutdown of device with autorestart behavior
- Electrostatic discharge protection (ESD)

**Diagnostic functions**

Diagnostic information via error flag: device overtemperature shutdown, output short to GND, output overvoltage

| Type | Package | Marking |
|---|---|---|
| TLD5191ES | PG-TSDSO-24 | TLD5191ES |

# Table of contents

# 1 Block diagram

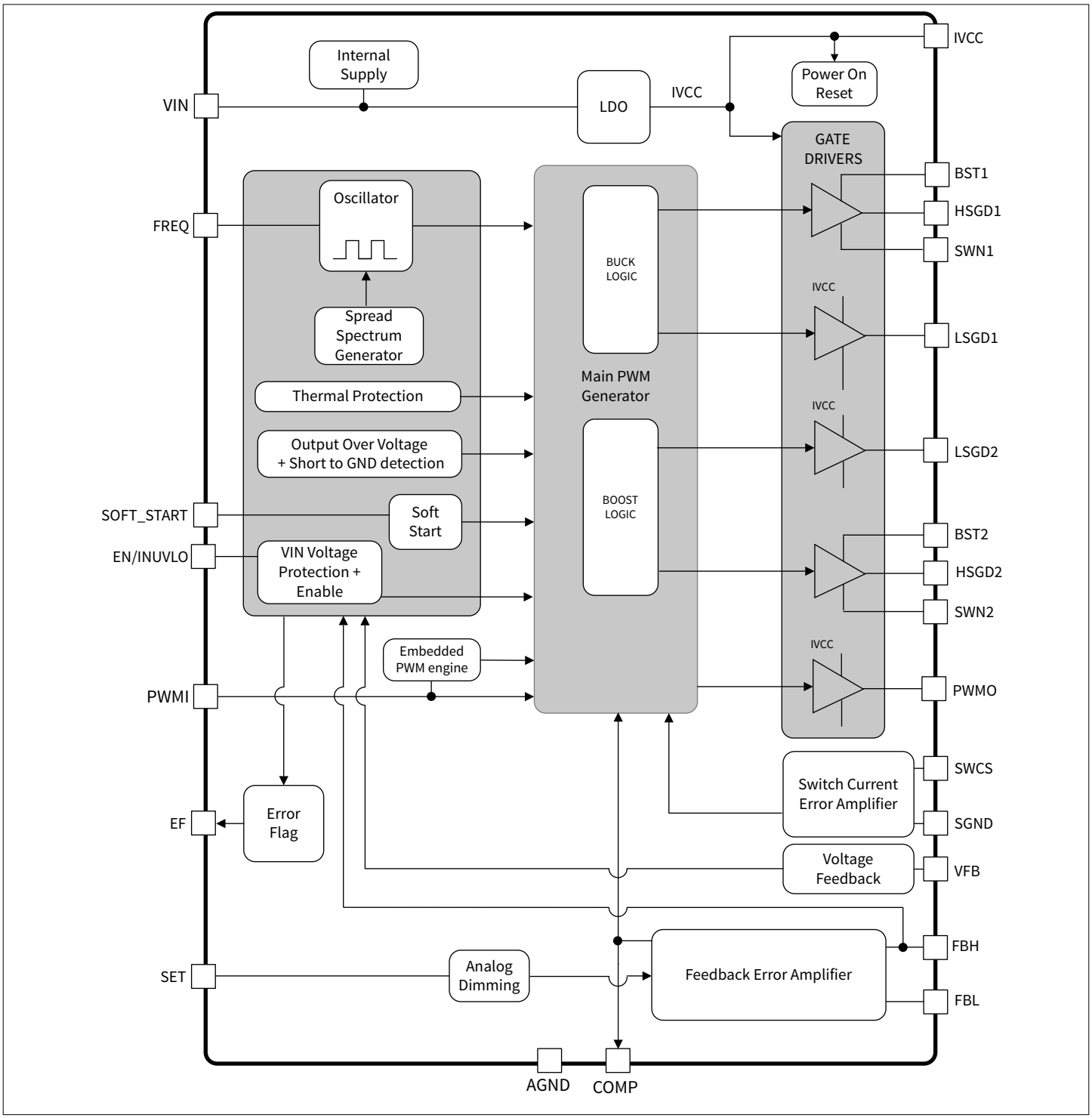



**Figure 1 Block diagram TLD5191ES**

# 2 Pin configuration

## 2.1 Pin assignment

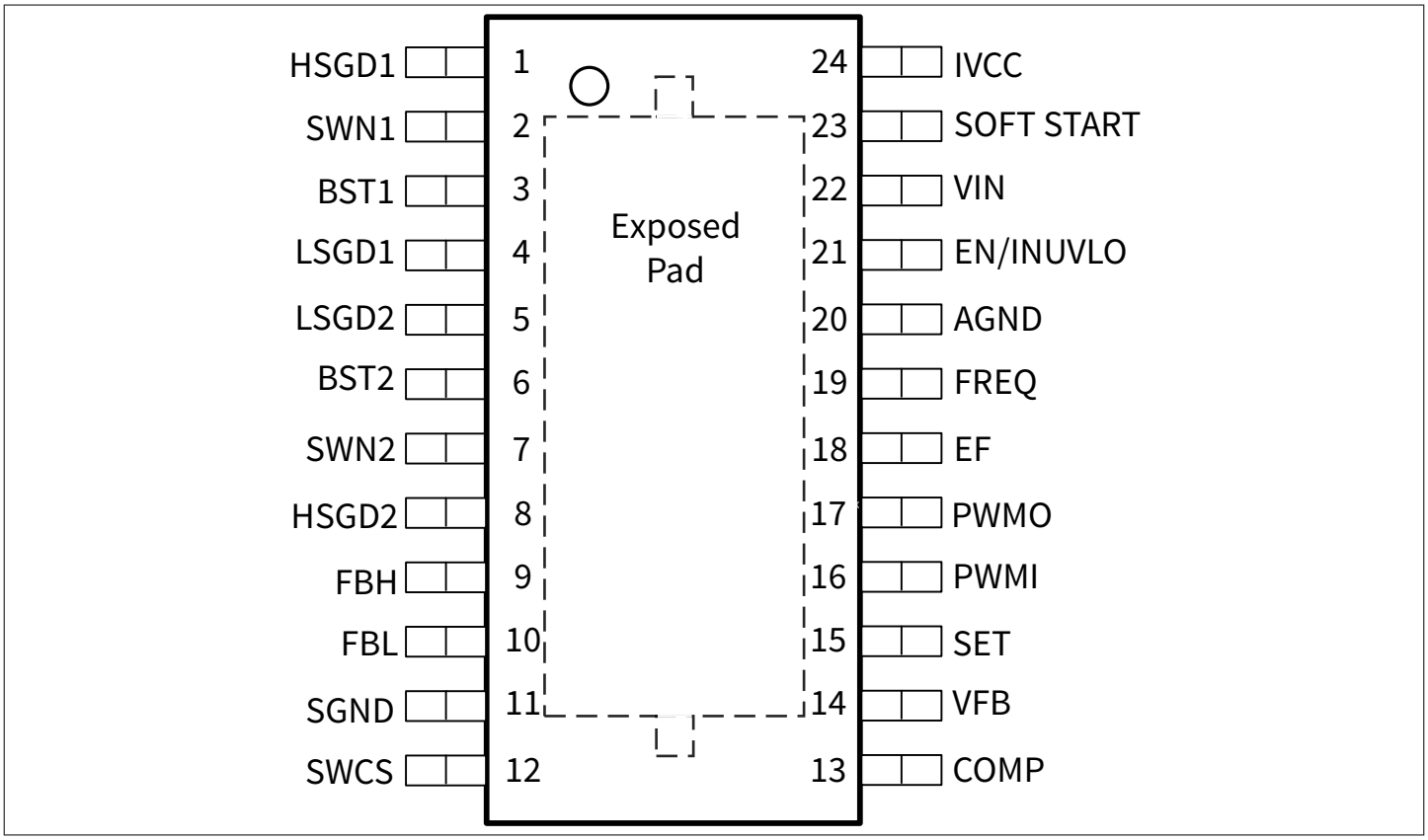



**Figure 2 Pin configuration PG-TSDSO-24**

## 2.2 Pin definitions and functions

**Table 1 Pin definitions and functions**

| Pin | Symbol | I/O[1)] | Function |
|---|---|---|---|
| 22 | VIN | - | **Power supply voltage**<br>Supply for internal biasing |
| 20 | AGND | - | **Analog ground**<br>Ground reference |
| - | EP | - | **Exposed pad**<br>Connect to external heatspreading Cu area (e.g. inner GND layer of multilayer PCB with thermal vias) |
| 1 | HSGD1 | O | **High-side gate driver output 1**<br>Drives the top n-channel MOSFET with a voltage equal to $V_{IVCC}$ superimposed on the switch node voltage SWN1. Connect to gate of external switching MOSFET |

**(table continues...)**

**Table 1 (continued) Pin definitions and functions**

| Pin | Symbol | I/O[1)] | Function |
|---|---|---|---|
| 8 | HSGD2 | O | **High-side gate driver output 2**<br>Drives the top n-channel MOSFET with a voltage equal to $V_{IVCC}$ superimposed on the switch node voltage SWN2. Connect to gate of external switching MOSFET |
| 4 | LSGD1 | O | **Low-side gate driver output 1**<br>Drives the low-side n-channel MOSFET between GND and $V_{IVCC.}$ Connect to gate of external switching MOSFET |
| 5 | LSGD2 | O | **Low-side gate driver output 2**<br>Drives the low-side n-channel MOSFET between GND and $V_{IVCC.}$ Connect to gate of external switching MOSFET |
| 2 | SWN1 | IO | **Switch node 1**<br>SWN1 pin swings from a diode voltage drop below ground up to $V_{IN}$ |
| 7 | SWN2 | IO | **Switch node 2**<br>SWN2 pin swings from ground up to a diode voltage drop above $V_{OUT}$ |
| 24 | IVCC | O | **Internal LDO output**<br>Used for internal biasing and gate driver supply. Bypass with external capacitor close to the pin. Pin must not be left open |
| 21 | EN/INUVLO | I, PD | **Enable/Input undervoltage lockout**<br>Used to put the device in a low current consumption mode, with additional capability to fix an undervoltage threshold via external components. Pin must not be left open |
| 19 | FREQ | I | **Frequency select input**<br>Connect external resistor to GND to set frequency |
| 16 | PWMI | I, PD | **PWM Control input**<br>Used to control the digital dimming via external PWM signal or via the embedded PWM engine |
| 9 | FBH | I | **Output current feedback positive**<br>Non inverting Input (+) |
| 10 | FBL | I | **Output current feedback negative**<br>Inverting Input (-) |
| 3 | BST1 | IO | **Bootstrap capacitor**<br>Used for internal biasing and to drive the high-side switch HSGD1. Bypass to SWN1 with external capacitor close to the pin. Pin must not be left open |
| 6 | BST2 | IO | **Bootstrap capacitor**<br>Used for internal biasing and to drive the high-side switch HSGD2. Bypass to SWN2 with external capacitor close to the pin. Pin must not be left open |
| 12 | SWCS | I | **Current sense input**<br>Inductor current measurement - Non-inverting input (+) |

**(table continues...)**

**Table 1 (continued) Pin definitions and functions**

| Pin | Symbol | I/O[1)] | Function |
|---|---|---|---|
| 11 | SGND | I | **Current sense / Power ground**<br>Inductor current sense - Inverting Input (-). Power ground, connect to GND |
| 13 | COMP | O | **Compensation network pin**<br>Connect R and C network to pin for stability phase margin adjustment |
| 23 | SOFT_START | O | **Softstart configuration pin**<br>Connect a capacitor $C_{SOFT\_START}$ to GND to fix a soft start ramp default time |
| 14 | VFB | I | **Output voltage feedback pin**<br>Output voltage feedback to set output overvoltage protection function |
| 15 | SET | I | **Analog current sense adjustment pin**<br>A voltage $V_{SET}$ between 0.2 V and 1.4 V will adjust the $I_{LED}$ or $V_{OUT}$ in a linear relation |
| 17 | PWMO | O | **PWM Digital dimming output**<br>Drives n-channel MOSFET between GND and $V_{IVCC}$ for dimming purposes |
| 18 | EF | O | **Error flag output**<br>An open drain output which is pulled to LOW when an output short to GND, an output overvoltage or IC overtemperature occurs |

1) O: Output, I: Input, PD: pull-down circuit integrated

# 3 General product characteristics

## 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings**

$T_J$ = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
Not subject to production test, specified by design

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Supply voltages** | | | | | | | |
| VIN Supply Input | $V_{VIN}$ | -0.3 | – | 60 | V | – | PRQ-32 |
| IVCC Internal linear voltage regulator output voltage | $V_{IVCC}$ | -0.3 | – | 6 | V | – | PRQ-33 |
| **Gate Driver Stages** | | | | | | | |
| LSGD1,2 Low-side gatedriver voltage | $V_{LSGD1,2}$ | -0.3 | – | 5.5 | V | – | PRQ-34 |
| HSGD1,2 - SWN1,2 High-side gate driver voltage | $V_{HSGD1,2-SWN1,2}$ | -0.3 | – | 5.5 | V | Differential signal (not referred to GND) | PRQ-35 |
| SWN1, SWN2 Switching node voltage | $V_{SWN1,\,2}$ | -1 | – | 60 | V | – | PRQ-36 |
| (BST1-SWN1), (BST2-SWN2) Boostrap voltage | $V_{BST1,2-SWN1,2}$ | -0.3 | – | 6 | V | Differential signal (not referred to GND) | PRQ-37 |
| BST1, BST2 Boostrap voltage related to GND | $V_{BST1,\,2}$ | -0.3 | – | 65 | V | – | PRQ-38 |
| SWCS Switch current sense input voltage | $V_{SWCS}$ | -0.3 | – | 0.3 | V | – | PRQ-39 |
| SGND Switch current sense GND voltage | $V_{SGND}$ | -0.3 | – | 0.3 | V | – | PRQ-40 |
| SWCS-SGND Switch current sense differential voltage | $V_{SWCS-SGND}$ | -0.5 | – | 0.5 | V | Differential signal (not referred to GND) | PRQ-41 |
| PWMO Output voltage | $V_{PWMO}$ | -0.3 | – | 5.5 | V | – | PRQ-46 |
| **High voltage pins** | | | | | | | |
| FBH, FBL Feedback error amplifier voltage | $V_{FBH,\,FBL}$ | -0.3 | – | 60 | V | – | PRQ-42 |
| FBH-FBL Feedback error amplifier differential voltage | $V_{FBH-FBL}$ | -0.5 | – | 0.5 | V | Differential signal (not referred to GND) | PRQ-43 |
| EN/INUVLO Device enable/input undervoltage lockout | $V_{EN/INUVLO}$ | -0.3 | – | 60 | V | – | PRQ-44 |

**(table continues...)**

**Table 2 (continued) Absolute maximum ratings**

$T_J$ = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
Not subject to production test, specified by design

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Analog pins** | | | | | | | |
| PWMI Input voltage | $V_{PWMI}$ | -0.3 | – | 5.5 | V | – | PRQ-45 |
| VFB Input voltage | $V_{VFB}$ | -0.3 | – | 5.5 | V | – | PRQ-47 |
| EF Error flag output voltage | $V_{EF}$ | -0.3 | – | 5.5 | V | – | PRQ-48 |
| SET Analog dimming input voltage | $V_{SET}$ | -0.3 | – | 5.5 | V | – | PRQ-49 |
| COMP Compensation input voltage | $V_{COMP}$ | -0.3 | – | 3.6 | V | – | PRQ-205 |
| SOFT_START Softstart voltage | $V_{SOFT\_START}$ | -0.3 | – | 3.6 | V | – | PRQ-50 |
| FREQ Voltage at frequency selection pin | $V_{FREQ}$ | -0.3 | – | 3.6 | V | – | PRQ-51 |
| **Temperatures** | | | | | | | |
| Junction Temperature | $T_J$ | -40 | – | 150 | °C | – | PRQ-52 |
| Storage Temperature | $T_{stg}$ | -55 | – | 150 | °C | – | PRQ-53 |
| **ESD susceptibility** | | | | | | | |
| ESD resistivity of all pins | $V_{ESD,HBM}$ | -2 | – | 2 | kV | HBM[1)] | PRQ-54 |
| ESD Resistivity to GND | $V_{ESD,CDM}$ | -750 | – | 750 | V | CDM[2)] | PRQ-55 |

1) ESD susceptibility, Human Body Model “HBM” according to AEC Q100-002
2) ESD susceptibility, Charged Device Model “CDM” according to AECQ100-011

*Notes:*

***1.*** *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

***2.*** *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 3.2 Functional range

**Table 3 Functional Range**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Device extended supply voltage range | $V_{VIN}$ | 4.5 | | 40 | V | 1) | PRQ-142 |
| Device nominal supply voltage range | $V_{VIN}$ | 8 | – | 36 | V | – | PRQ-57 |
| Power stage voltage range | $V_{POW}$ | 4.5 | – | 55 | V | 1) | PRQ-58 |
| Junction temperature | $T_J$ | -40 | – | 150 | °C | – | PRQ-59 |

1) Not subject to production test, specified by design.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to* www.jedec.org.

**Table 4 Thermal Resistance**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to case | $R_{thJC}$ | – | 7.78 | – | K/W | 1) 2) | PRQ-60 |
| Junction to ambient | $R_{thJA}$ | – | 38.2 | – | K/W | 3) 2s2p | PRQ-61 |

1) Not subject to production test, specified by design
2) Specified $R_{thJC}$ value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). $T_A$ = 25°C; The IC is dissipating 1 W
3) Specified $R_{thJA}$ value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 µm Cu) and 2 inner copper layers (2 x 35 µm Cu). A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. $T_A$ = 25°C; The IC is dissipating 1 W

# 4 Power supply

## 4.1 Description

The TLD5191ES is supplied by the VIN (main supply voltage) pin.

The VIN supply provides internal supply voltages for the analog and digital blocks.

IVCC supplies the low side driver stages and the PWMO driver.

This supply is used also to charge, through external Schottky diodes, the bootstrap capacitors which provide supply voltages to the high-side driver stages.

The supply pins VIN and IVCC have undervoltage detections.

If the voltage on IVCC goes below $V_{IVCC\_RTH,d}$, driver stages are deactivated, thus stopping the switching activity.

The EN/INUVLO pin can be used as input undervoltage protection by placing a resistor divider from VIN to GND.

If the voltage on EN/INUVLO pin goes below $V_{EN/INUVLOth}$, IVCC voltage regulator is switched off, and switching activity is stopped.

Figure 3 shows a basic concept drawing of the supply domains and interactions among pins VIN and IVCC.

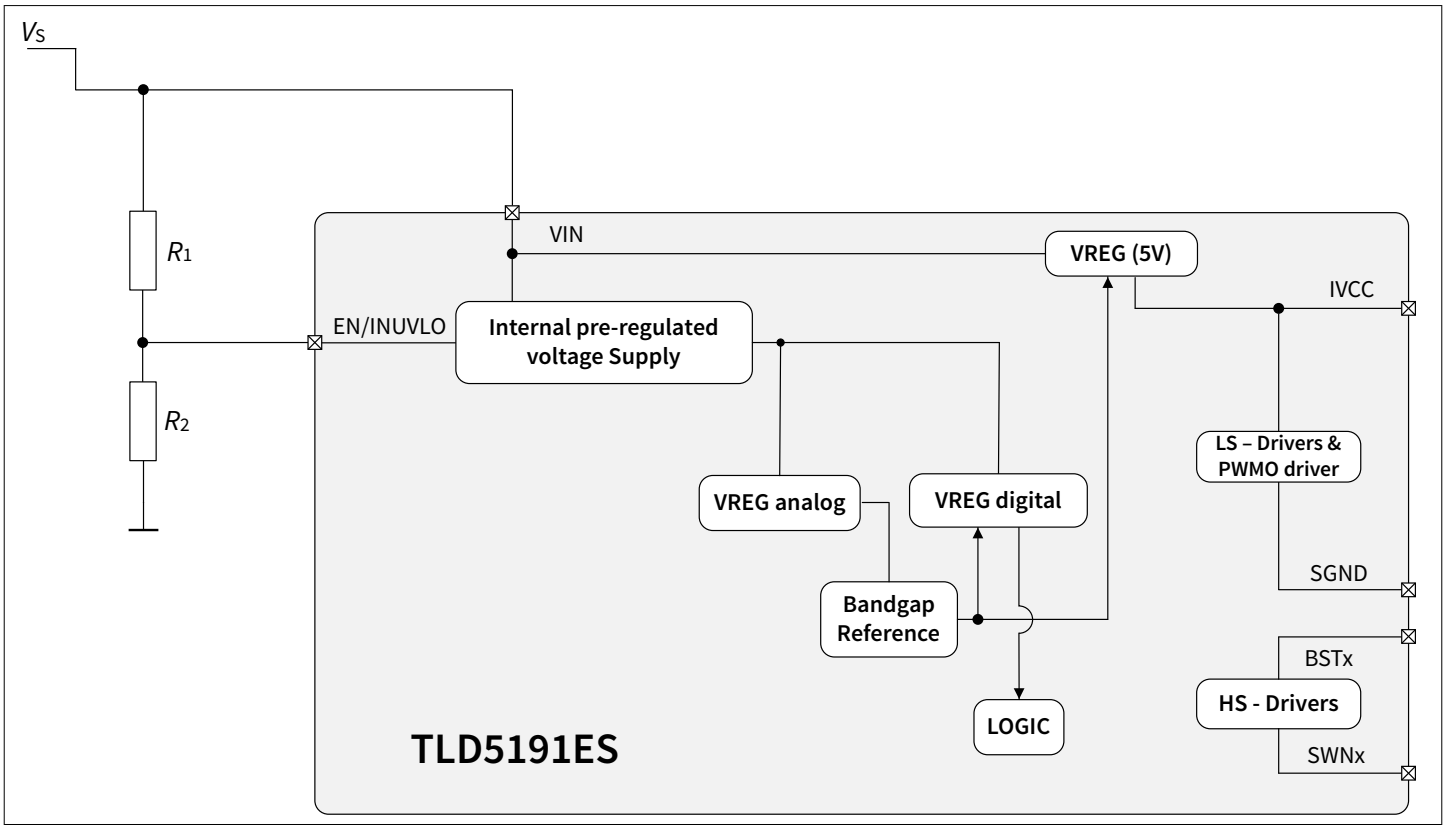



**Figure 3 Power supply concept diagram**

### Usage of EN/INUVLO pin in different applications

The pin EN/INUVLO is a double function pin and can be used to put the device into a low current consumption mode. An undervoltage threshold should be fixed by placing an external resistor divider (A) in order to avoid low voltage operating conditions. This pin can be driven by a µC-port as shown in (B) and (C) or directly connected to the input voltage supply as shown in (D).

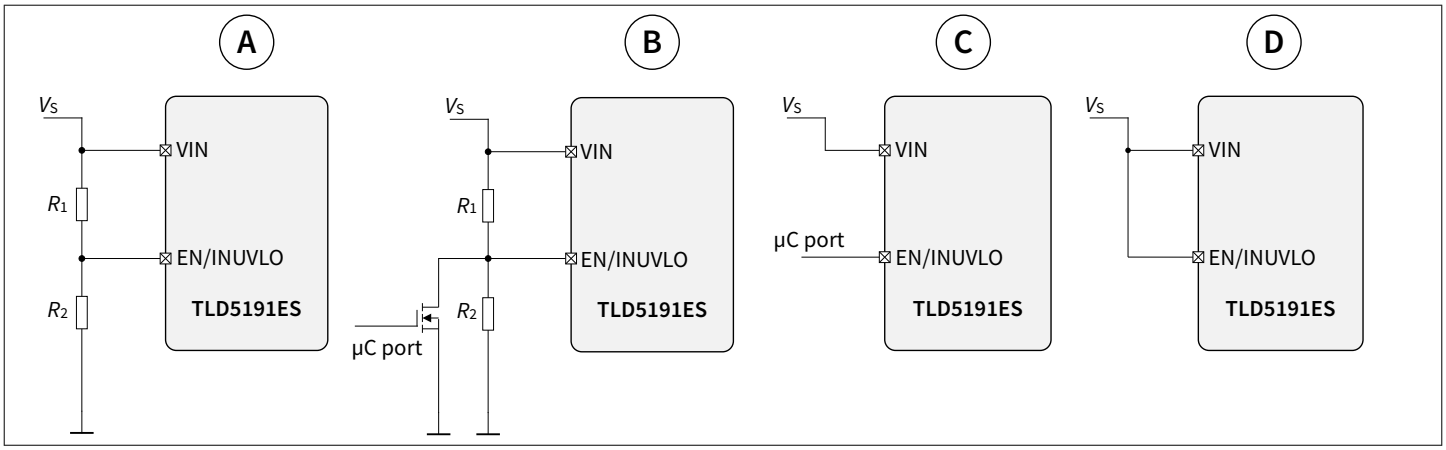



**Figure 4 Usage of EN/INUVLO pin in different applications**

## 4.2 Different power states

TLD5191ES has the following power states:

- SLEEP state
- IDLE state
- ACTIVE state

The transition between the power states is determined according to these variables:

- VIN level
- EN/INUVLO level
- IVCC level

The state diagram including the possible transitions is shown in Figure 5

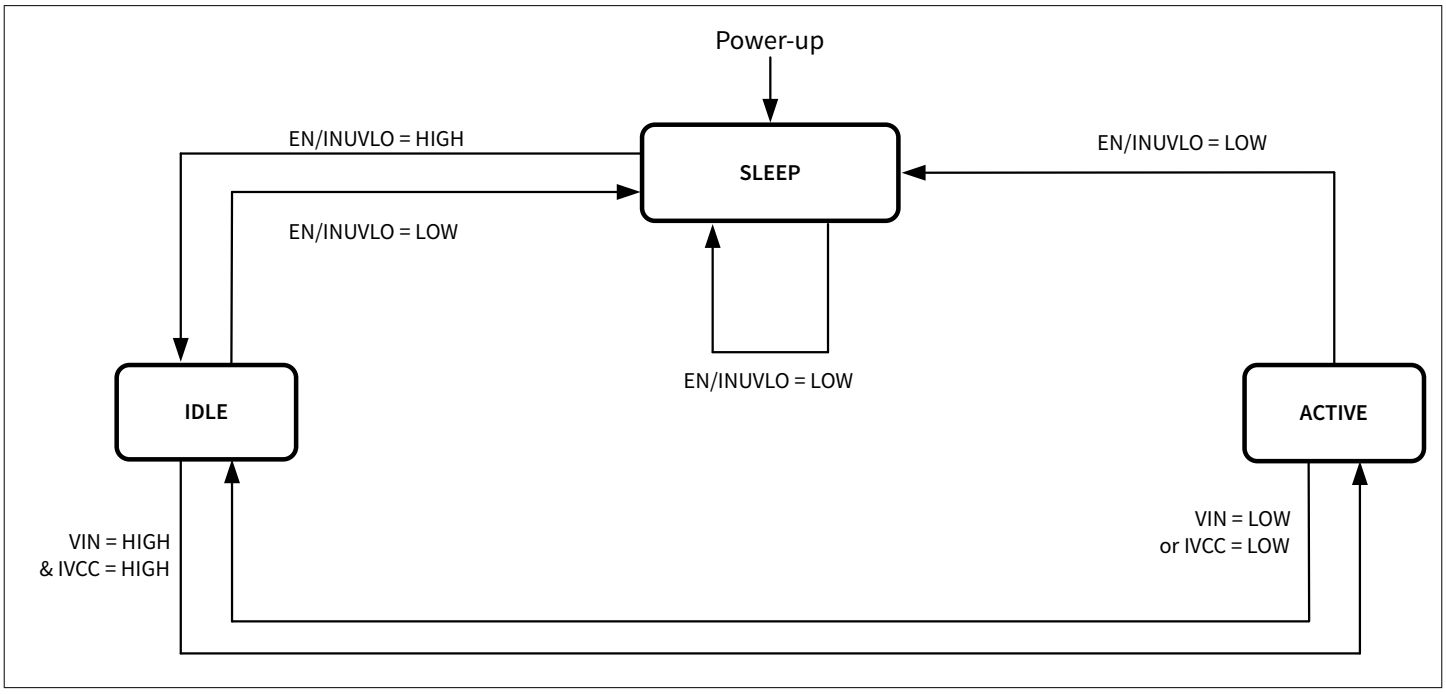



**Figure 5 Simplified state diagram**

The Power-up condition is entered when the supply voltage $V_{VIN}$ exceeds its minimum supply voltage threshold $V_{VIN(ON)}$.

### SLEEP

When the TLD5191ES is in the SLEEP state, all gate drivers and error flag are in OFF state, independently from the supply voltages $V_{IN}$, IVCC. The current consumption is lower than $I_{VIN(SLEEP)}$.

The transition from SLEEP to ACTIVE state requires a specified time: $t_{ACTIVE}$.

### IDLE

In IDLE state the internal voltage regulator is working. The output drivers are switched OFF.

Diagnosis functions are not available.

### ACTIVE

In active state the device will start switching activity to provide power at the output only when PWMI = HIGH or PWMI is in a valid range to enable the embedded PWM engine.

If the voltage between pins BST1,2 and SWN1,2 is higher than $V_{BST1,2\text{ - }VSWN1,2\_Uvth}$, high side gate drivers are enabled, otherwise they are disabled and no switching activity is permitted.

In active state the device current consumption via $V_{IN}$ is dependent on the external MOSFETs used and the switching frequency $f_{SW}$.

Digital dimming PWM activity is mirrored on the PWMO output pin unless a fault condition is detected (for details see Chapter 6.1).

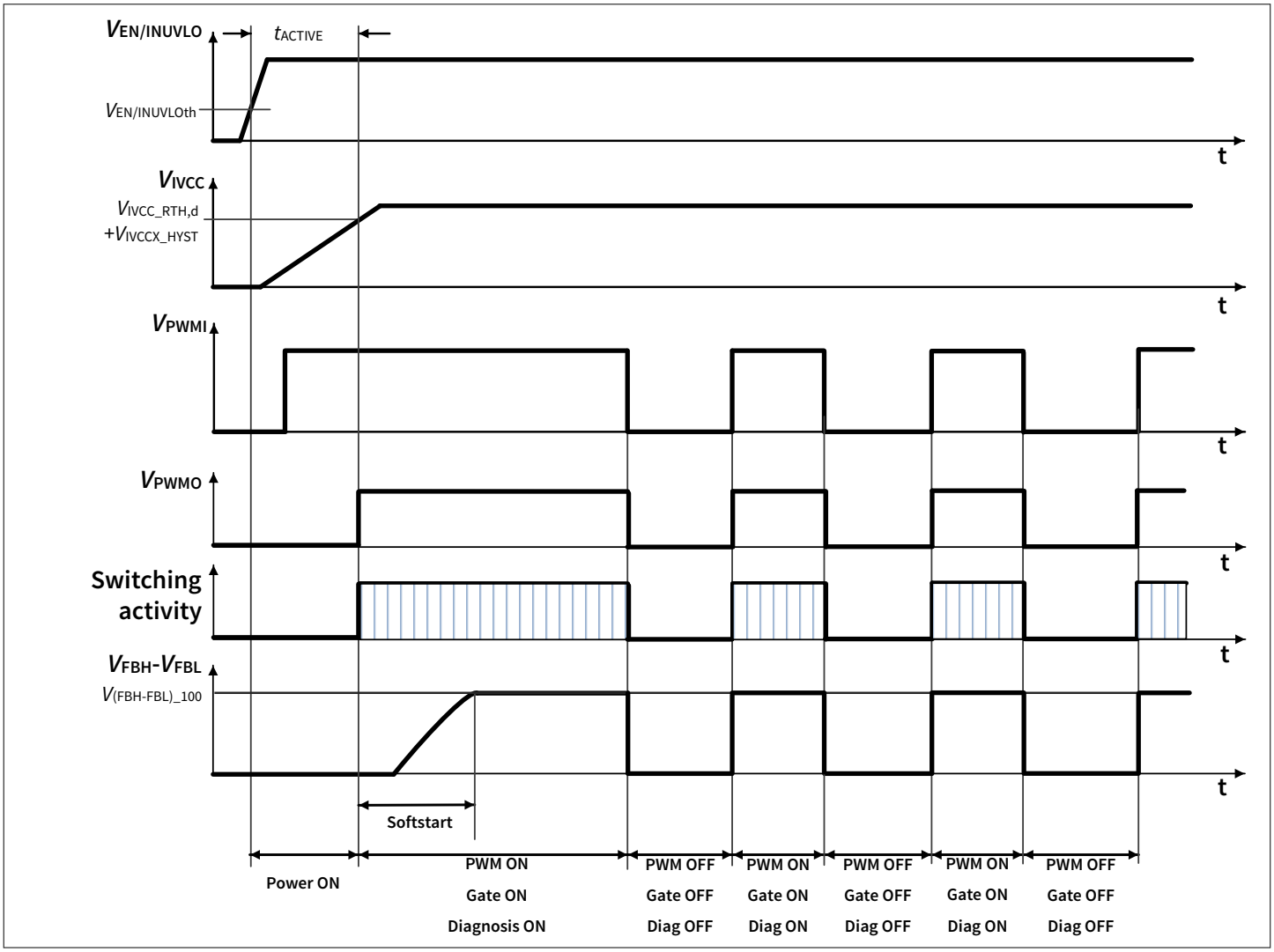



**Figure 6 Timing diagram LED dimming and startup behavior example ($V_{VIN}$ stable in the functional range and not during startup)**

## 4.3 Electrical characteristics

**Table 5 Electrical Characteristics**

$V_{IN}$ = 8V to 36V, $T_J$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Input voltage startup | $V_{VIN(ON)}$ | – | – | 4.7 | V | $V_{VIN}$ increasing; $V_{EN/INUVLO}$ = HIGH; $I_{IVCC}$ = 0 mA | PRQ-64 |
| Input undervoltage switch OFF | $V_{VIN(OFF)}$ | – | – | 4.5 | V | $V_{VIN}$ decreasing; $V_{EN/INUVLO}$ = HIGH; $I_{IVCC}$ = 10 mA | PRQ-65 |
| Device operating current | $I_{VIN(ACTIVE)}$ | – | 5 | 7 | mA | 1) ACTIVE mode; $V_{PWMI}$ = 0 V | PRQ-66 |
| VIN Sleep mode supply current | $I_{VIN(SLEEP)}$ | – | – | 1.5 | µA | $V_{EN/INUVLO}$ = 0 V; $V_{VIN}$ = 13.5 V; $V_{IVCC}$ = 0 V | PRQ-67 |
| Input undervoltage falling threshold | $V_{EN/INUVLOth}$ | 1.6 | 1.75 | 1.9 | V | – | PRQ-68 |
| EN/INUVLO rising hysteresis | $V_{EN/INUVLO(hyst)}$ | – | 90 | – | mV | 1) | PRQ-69 |
| EN/INUVLO input current LOW | $I_{EN/INUVLO(LOW)}$ | 0.45 | 0.89 | 1.34 | µA | $V_{EN/INUVLO}$ = 0.8 V; | PRQ-70 |
| EN/INUVLO input current HIGH | $I_{EN/INUVLO(HIGH)}$ | 1.1 | 2.2 | 3.3 | µA | $V_{EN/INUVLO}$ = 2 V; | PRQ-71 |
| SLEEP mode to ACTIVE time | $t_{ACTIVE}$ | – | – | 0.7 | ms | 1) $C_{IVCC}$ = 10 µF; $V_{VIN}$= 13.5 V | PRQ-72 |

1) Not subject to production test, specified by design

# 5 Regulator

The TLD5191ES includes all of the functions necessary to provide constant current to the output as usually required to drive LEDs. A constant voltage regulation can also be implemented (refer to Chapter 5.5).

It is designed to control 4 gate driver outputs in a H-Bridge topology by using only one inductor and 4 external MOSFETs. This topology is able to operate in high power BOOST, BUCK-BOOST and BUCK mode applications with maximum efficiency.

The transition between the different regulation modes is done automatically by the device itself, with respect to the application boundary conditions.

The transition phase between modes is seamless.

## 5.1 Regulator diagram

An analog current control loop (with total gain = $IFBx_{gm}$) connected to the sensing pins FBL, FBH regulates the output current.

The regulator function is implemented by a pulse width modulated (PWM) current mode controller. The error in the output current loop is used to determine the appropriate duty cycle to get a constant output current.

An external compensation network (RCOMP, CCOMP) is used to adjust the control loop to various application boundary conditions. The inductor current for the current mode loop is sensed by the RSWCS resistor. $R_{SWCS}$ is used also to limit the maximum external switches / inductor current.

If the voltage across $R_{SWCS}$ exceeds its overcurrent threshold ($V_{SWCS\_buck}$ or $V_{SWCS\_boost}$ for buck or boost operation respectively) the device reduces the duty cycle in order to bring the switches current below the imposed limit.

The current mode controller has a built-in slope compensation as well to prevent sub-harmonic oscillations.

The control loop logic block (LOGIC) provides a PWM signal to four internal gate drivers. The gate drivers (HSGD1,2 and LSGD1,2) are used to drive external MOSFETs in an H-Bridge setup.

Once $V_{SOFT\_START}$ exceeds $V_{Soft\_Start\_LOFF}$ or $V_{FBH-FBL}$ exceeds $V_{FBH\_FBL\_VALID}$, TLD5191ES forces CCM regulation mode.

The control loop block diagram displayed in Figure 7 shows a typical constant current application. The voltage across $R_{FB}$ sets the output current.

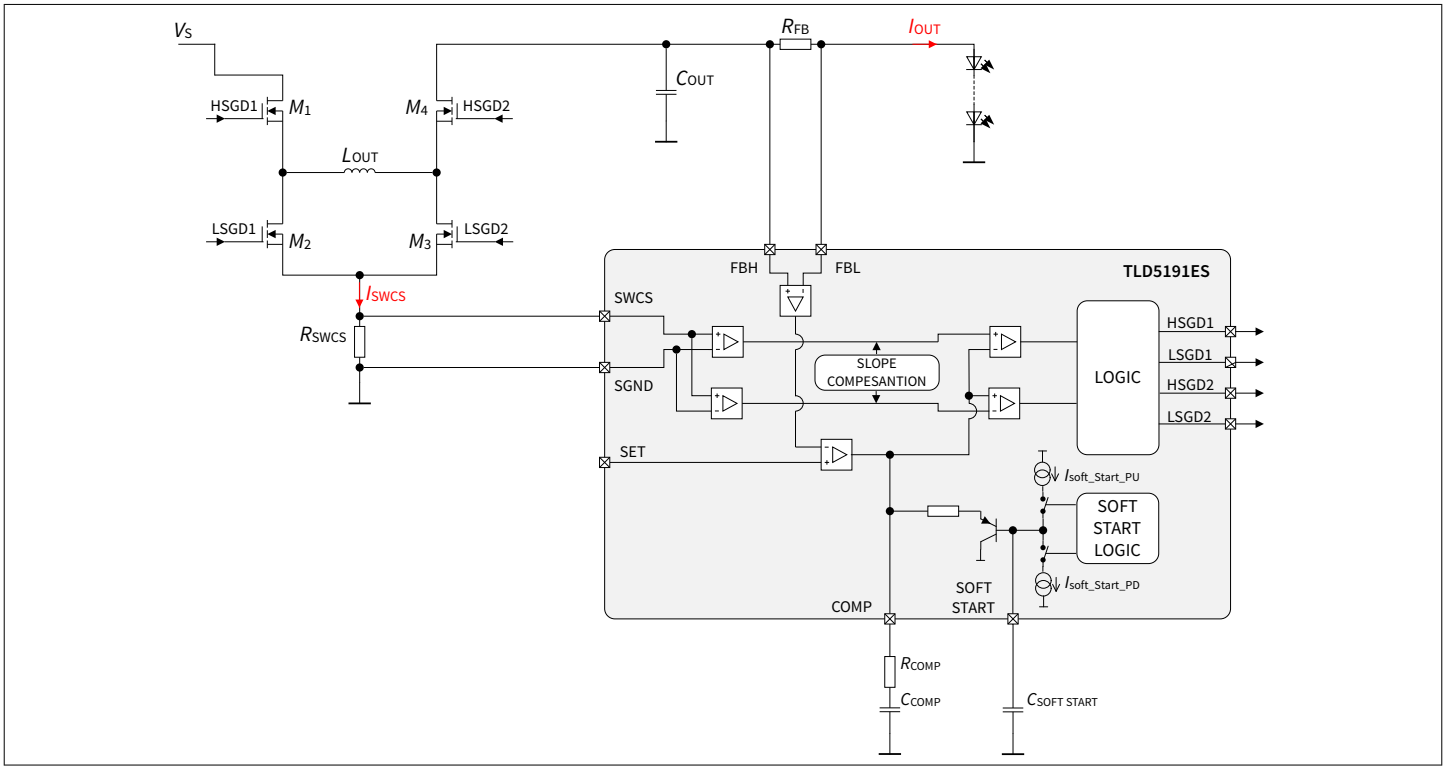



**Figure 7 Regulator block diagram - TLD5191ES**

## 5.2 Adjustable soft-start ramp

The soft-start routine limits the current through the inductor and the external MOSFET switches during initialization to minimize potential overshoots at the output.

The SOFT START pin is also used to implement a fault mask and wait-before-retry time, on rising and falling edge respectively.

See Figure 8 and Chapter 9.2 for details.

The soft start routine is applied if PWMI is above $V_{PWMI,ON}$ or PWMI is in a valid range to enable the embedded PWM engine, if one of the following conditions is verified:

- after IDLE to ACTIVE power state transition
- after PWMI has been kept below $V_{PWMI,DC\_0}$ for more than $t_{PWMI,OFF}$
- after output short to GND detection

The soft start routine is active during the rising and falling edge of $V_{SOFT\_START}$. The soft start timing is defined by a capacitor placed on the SOFT_START pin and both the soft start pull-up and pull-down current sources ($I_{Soft\_Start\_PU}$, $I_{Soft\_Start\_PD}$). Soft start rising edge time is approximately:

$$t_{Soft\_Start,r} = V_{Soft\_Start\_LOFF} \cdot \frac{C_{Soft\_Start}}{I_{Soft\_Start\_PU}} \quad (1)$$

*Note: Minimum value of soft start capacitor has to be designed such that, during startup, the output voltage exceeds the short to ground threshold ($V_{FBH} > V_{FBH\_S2G\_inc}$), before the soft start voltage reaches $V_{SOFT\_START\_LOFF}$. Minimum temperature and minimum input voltage shall be considered as worst case condition for the dimensioning.*

The soft start routine limits the inrush current by clamping the COMP pin through a buffer like depicted in Figure 7. Therefore this functionality is effective only when soft start capacitor is sufficiently larger than the COMP capacitor and its effect is visible mainly in buck-boost or boost regulation mode.

If a short circuit on the output is detected the pull-down current source $I_{Soft\_Start\_PD}$ is activated. This current discharges the $V_{SOFT\_START}$ until $V_{Soft\_Start\_RESET}$ is reached. Afterwards the pull-up current source $I_{Soft\_Start\_PU}$ turns on again only if the PWMI signal is higher than $V_{PWMI,DC\_0}$. If the fault condition hasn't been removed before $V_{Soft\_Start\_LOFF}$ is reached, the pull-down current source is reactivated initiating a new cycle.

During soft start rise time switching activity is observed, during the fall time instead the switching activity is halted like shown in Figure 8. This hiccup mode will continue until the fault is removed.

It is possible to latch the fault condition on the TLD5191ES by sourcing a current higher than $I_{Soft\_Start\_PD}$ through an external pull-up resistor connected from IVCC to the SOFT START pin. In this condition the device will restart regulating only if EN/INUVLO pin is toggled or if PWMI is toggled after having kept it low for more than $t_{PWMI,OFF}$.

During rising edge of soft start, the internal PWM is extended till one of the 2 following condition is reached:

- Until $V_{SOFT\_START}$ exceeds $V_{Soft\_Start\_LOFF}$
- Until $V_{FBH-FBL}$ exceeds $V_{FBH\_FBL\_VALID}$

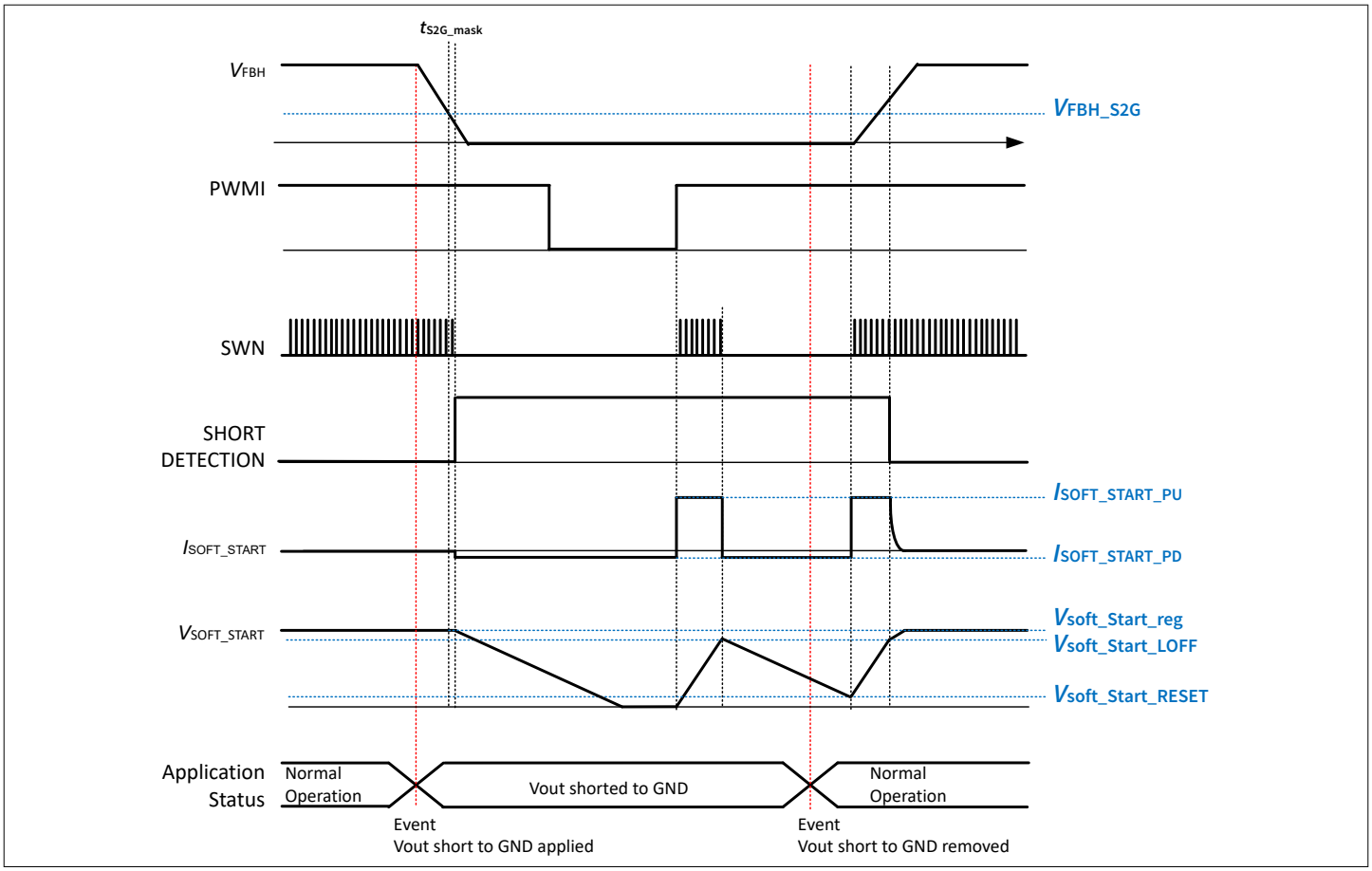



**Figure 8 Soft start timing diagram on a short to ground detected by the FBH pin**

## 5.3 Switching frequency setup

The switching frequency can be set from 200 kHz to 700 kHz by an external resistor connected from the FREQ pin to GND. Select the switching frequency with an external resistor according to the graph in Figure 9 or the following approximated formulas.

$$f_{SW}[kHz] = 5375 * \left(R_{FREQ}[k\Omega]\right)^{-0.8} \quad (2)$$

$$R_{FREQ}\,[k\Omega] = 46023 * \left(f_{SW}[kHz]\right)^{-1.25} \quad (3)$$

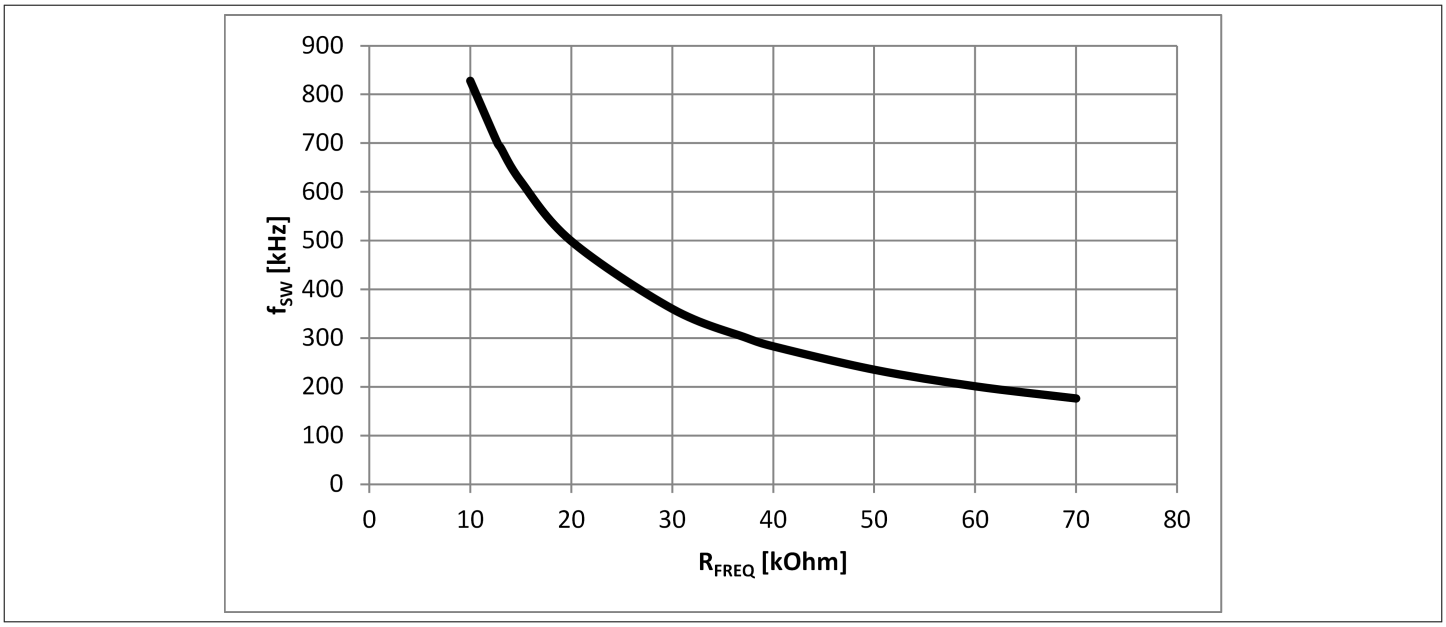



**Figure 9 Switching frequency $f_{SW}$ versus frequency select resistor to GND $R_{FREQ}$**

## 5.4 Operation of 4 switches H-Bridge architecture

Inductor $L_{OUT}$ connects in an H-Bridge configuration with 4 external n-channel MOSFETs ($M_1$, $M_2$, $M_3$ & $M_4$)

- Transistor $M_1$ and $M_3$ provides a path between $V_{IN}$ and ground through $L_{OUT}$ in one direction (Driven by top and bottom gate drivers HSGD1 and LSGD2)
- Transistor $M_2$ and $M_4$ provides a path between $V_{OUT}$ and ground through $L_{OUT}$ in the other direction (Driven by top and bottom gate drivers HSGD2 and LSGD1)
- Nodes SWN1, SWN2, voltage across $R_{SWCS}$ and load current are also monitored by the TLD5191ES

**Table 6 4 switches H-Bridge architecture transistor status summary**

| | BOOST mode | BUCK-BOOST mode | BUCK mode |
|---|---|---|---|
| M1 | ON | PWM | PWM |
| M2 | OFF | PWM | PWM |
| M3 | PWM | PWM | OFF |
| M4 | PWM | PWM | ON |

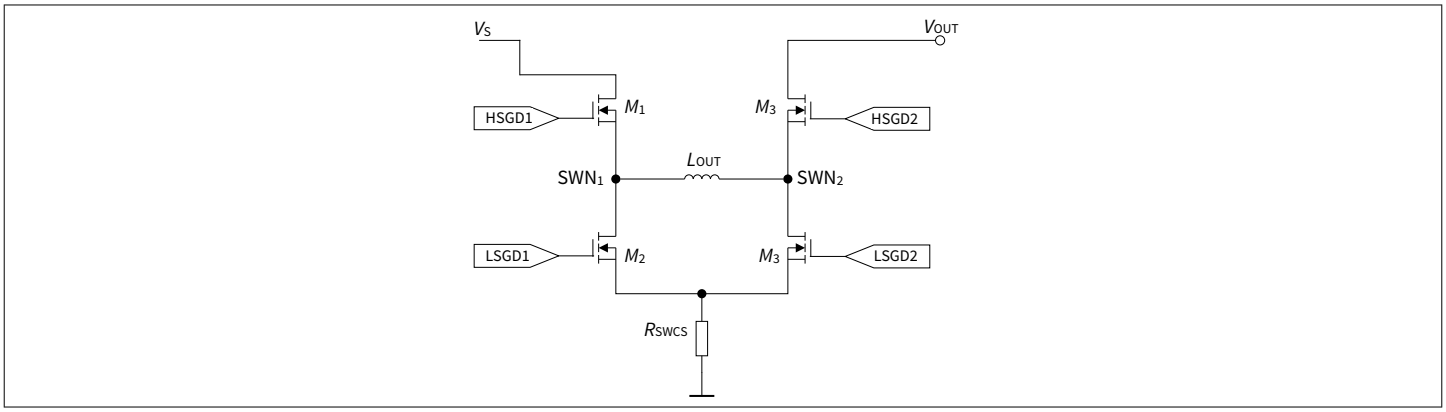



**Figure 10 4 switches H-Bridge architecture overview**

### 5.4.1 Boost mode (VIN < VOUT)

- $M_1$ is always ON, $M_2$ is always OFF
- Every cycle $M_3$ turns ON first and inductor current is sensed (peak current control)
- $M_3$ stays ON until the upper reference threshold is reached across $R_{SWCS}$ (Energizing)
- $M_3$ turns OFF, M4 turns ON until the end of the cycle (Recirculation)
- Switches $M_3$ and $M_4$ alternate, behaving like a typical synchronous boost regulator

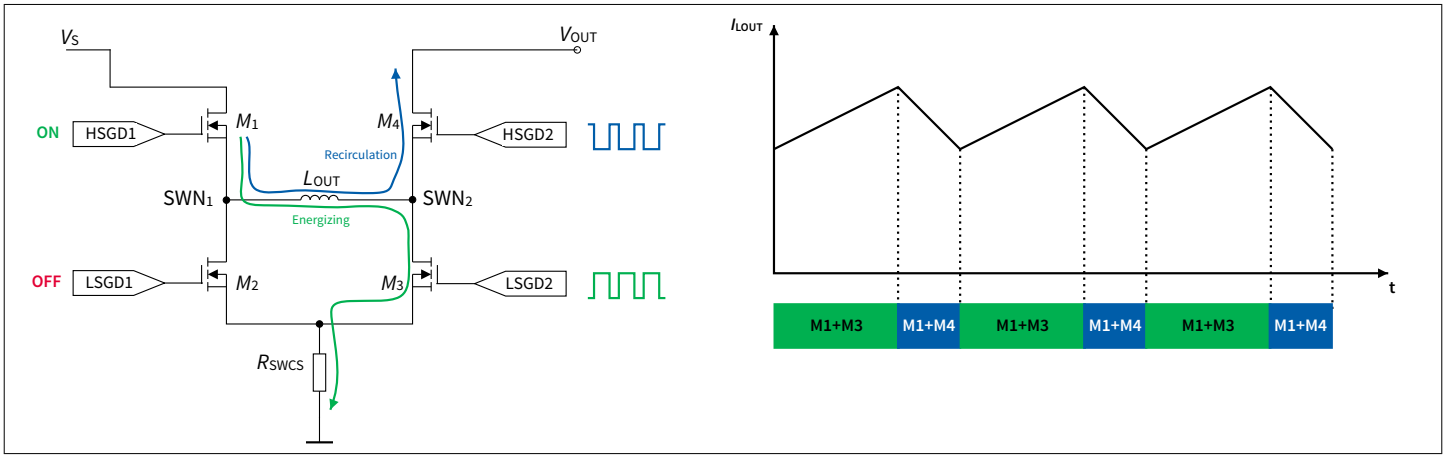



**Figure 11 4 switches H-Bridge architecture in BOOST mode**

**Simplified comparison of 4 switches H-Bridge architecture to traditional asynchronous Boost approach**

- $M_2$ is always OFF in this mode (open)
- $M_1$ is always ON in this mode (closed connection of inductor to $V_{IN}$)
- $M_4$ acts as a synchronous diode, with significantly lower conduction power losses ($I^2$ x $R_{DSON}$ vs. 0.7 V x $I$)

*Note: Diode is source of losses and lower system efficiency!*

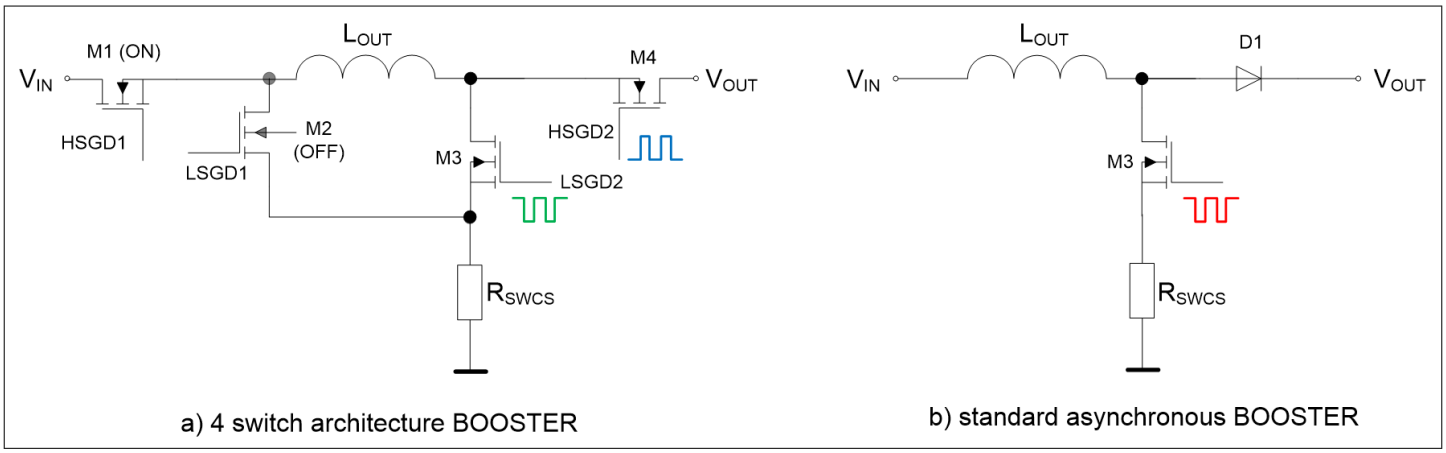



**Figure 12 4 switches H-Bridge architecture in BOOST mode compared to standard async booster**

### 5.4.2 Buck mode (VIN > VOUT)

- $M_4$ is always ON, $M_3$ is always OFF
- Every cycle $M_2$ turns ON and inductor current is sensed (valley current control)
- $M_2$ stays ON until the lower reference threshold is reached across $R_{SWCS}$ (Recirculation)
- $M_2$ turns OFF, $M_1$ turns ON until the end of the cycle (Energizing)
- Switches $M_1$ and $M_2$ alternate, behaving like a typical synchronous BUCK Regulator

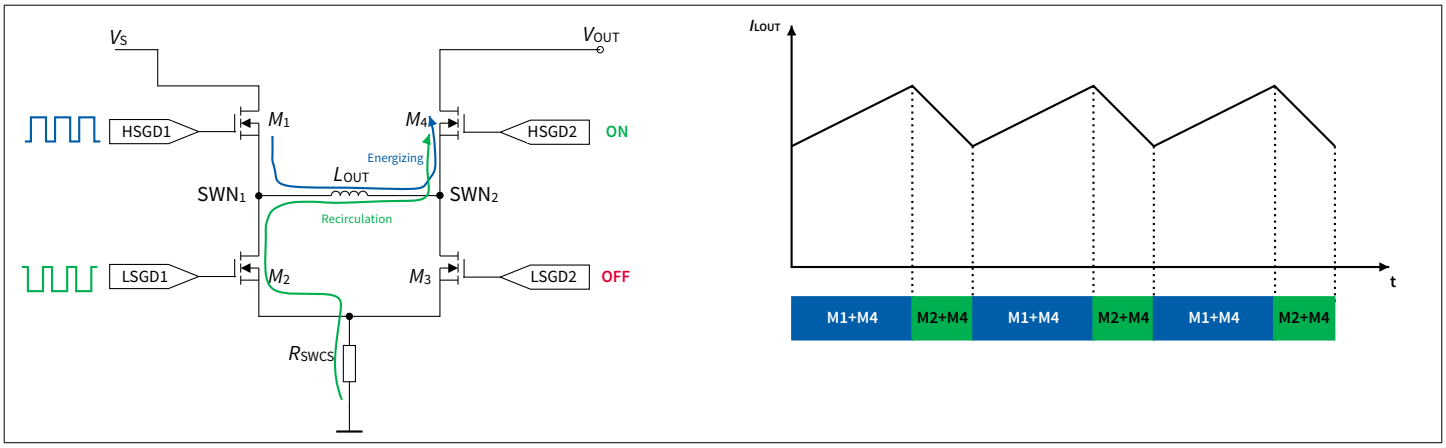



**Figure 13 4 switches H-Bridge architecture in BUCK mode**

**Simplified comparison of 4 switches architecture to traditional asynchronous Buck approach**

- $M_3$ is always OFF in this mode (open)
- $M_4$ is always ON in this mode (closed connection inductor to $V_{OUT}$)
- $M_2$ acts as a synchronous diode, with significantly lower conduction losses ($I^2$ x $R_{DSON}$ vs. 0.7 V x $I$)

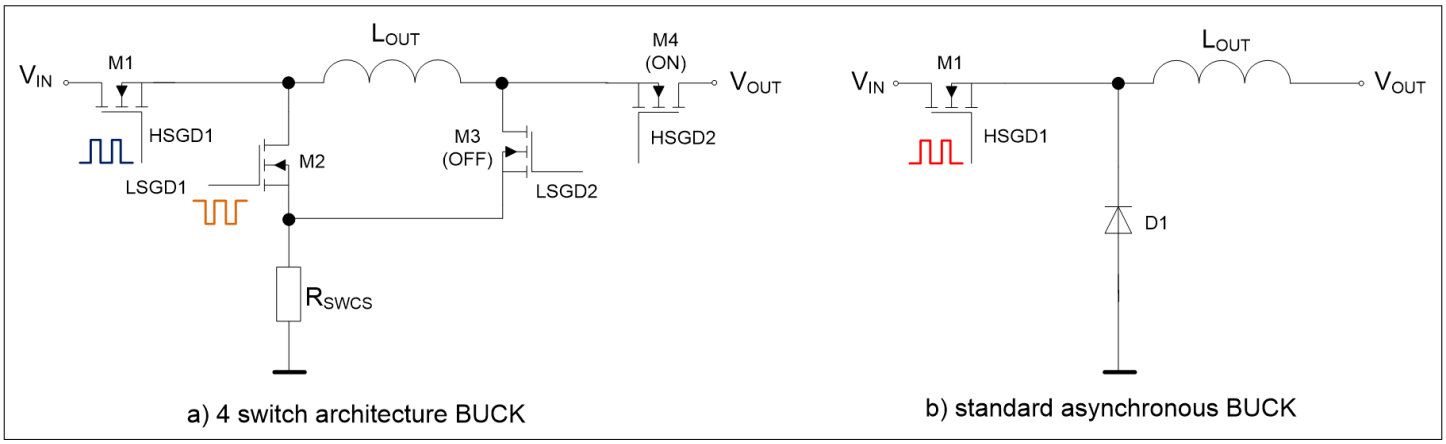



**Figure 14 4 switches H-Bridge architecture in BUCK mode compared to standard async BUCK**

## 5.4.3 Buck-Boost mode (VIN ~ VOUT)

- When $V_{IN}$ is close to $V_{OUT}$ the controller is in Buck-Boost operation
- All switches are switching in buck-boost operation. The direct energy transfer from the input to the output ($M_1$+$M_4$ = ON) is beneficial to reduce ripple current and improves the energy efficiency of the buck-boost control scheme
- The two buck boost waveforms and switching behaviors are displayed in Figure 15 below

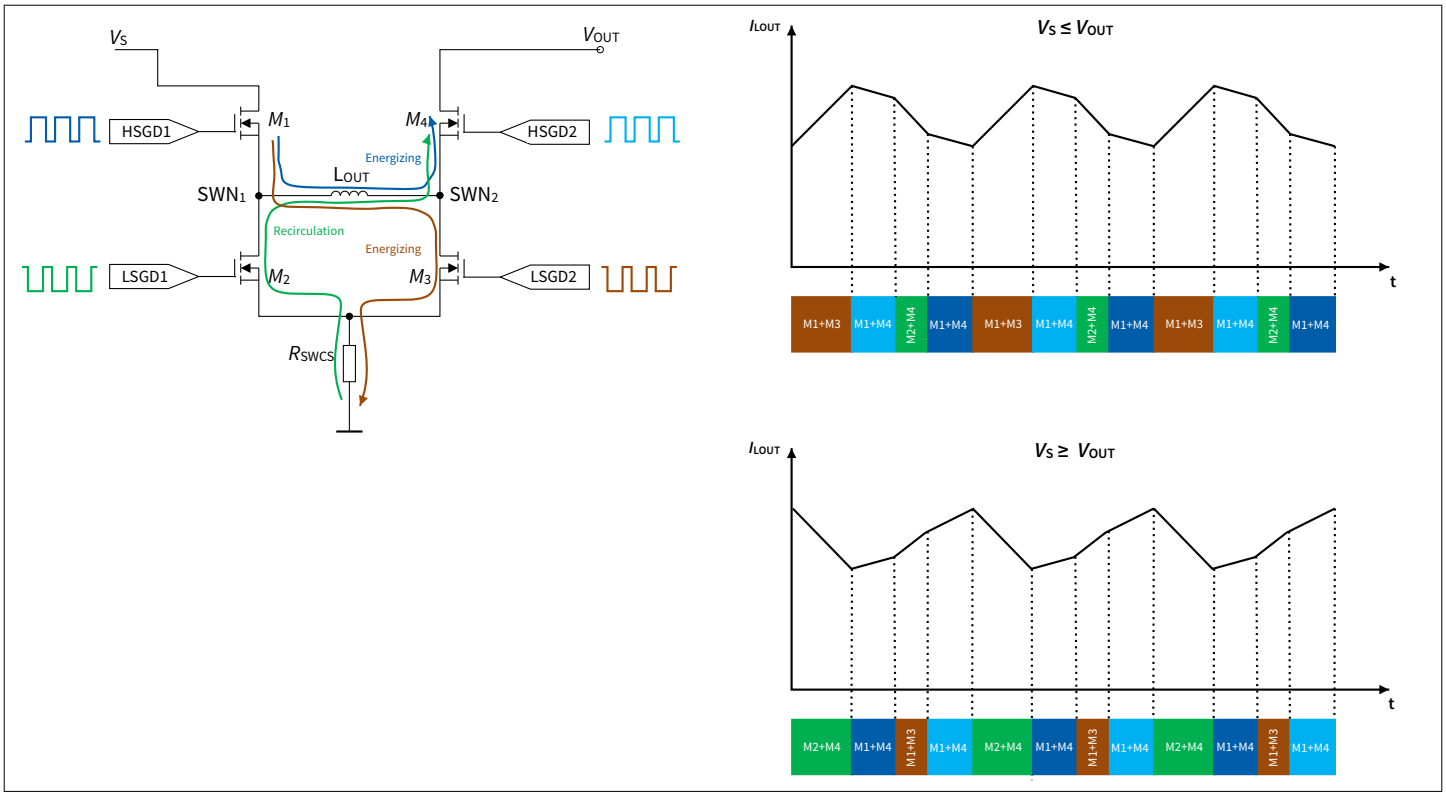



**Figure 15 4 switches H-Bridge architecture in BUCK_BOOST mode**

## 5.5 Programming output voltage (constant voltage regulation)

For a voltage regulator, the output voltage can be set by selecting the values $R_{FB1}$ and $R_{FB2}$ according to the following equation:

$$V_{OUT} = \left(\frac{V_{FBH-FBL}}{R_{FB1}} - I_{FBL}\right) \cdot R_{FB2} + V_{FBH-FBL} \quad (4)$$

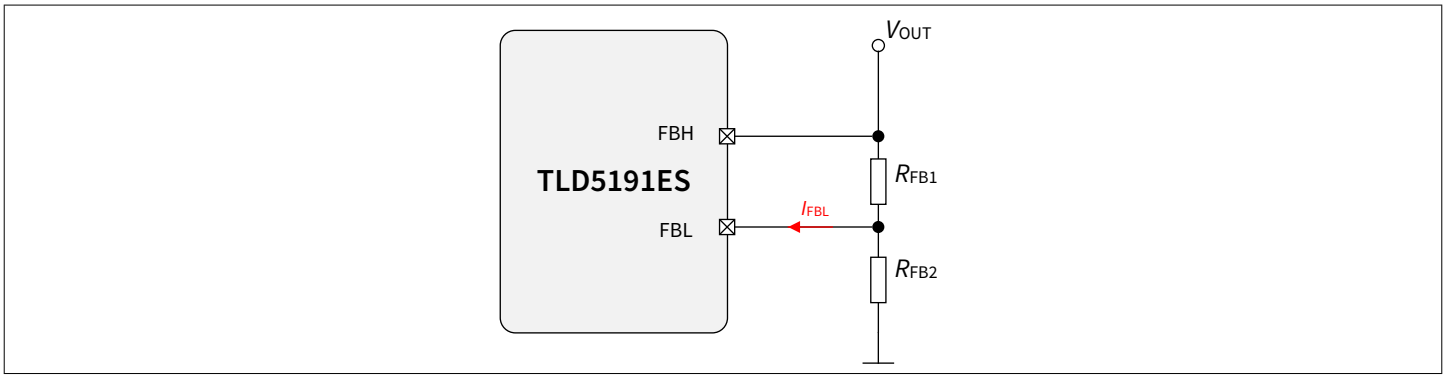



**Figure 16 Programming output voltage (Constant voltage regulation)**

## 5.6 Electrical characteristics

**Table 7 Electrical characteristics**

$V_{IN}$ = 8 V to 36 V, $T_J$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| V(FBH-FBL) threshold @ analog dimming 100% | $V_{(FBH-FBL)\_100}$ | 145.5 | 150 | 154.5 | mV | $V_{SET}$ = 2 V; $V_{FBH}$ = 2 V to 60 V; | PRQ-73 |
| V(FBH-FBL) threshold @ analog dimming 10% | $V_{(FBH-FBL)\_10}$ | 10 | 15 | 20 | mV | $V_{SET}$ = 0.32 V; $V_{FBH}$ = 2 V to 60 V | PRQ-74 |
| FBH Bias current | $I_{FBH}$ | 65 | 110 | 155 | µA | 1) $V_{FBL}$ = 7 V; $V_{FBH\ -FBL}$ = 150 mV | PRQ-75 |
| FBL Bias current | $I_{FBL}$ | 17 | 30 | 43 | µA | 1) $V_{FBL}$ = 7 V; $V_{FBH-FBL}$ = 150 mV | PRQ-76 |
| V(FBH-FBL) valid range threshold | $V_{FBH\_FBL\_VALID}$ | 110 | 120 | 130 | mV | $V_{SET}$ > 1.5 V | PRQ-198 |
| OUT Current sense amplifier gain | $IFBx_{gm}$ | – | 890 | – | µS | 1) | PRQ-77 |
| Maximum BOOST duty cycle | $D_{BOOST\_MAX}$ | 89 | 91 | 93 | % | 1) $f_{sw}$ = 300 kHz | PRQ-80 |
| Switch peak over current threshold - BOOST | $V_{SWCS\_boost}$ | 70 | 76 | 82 | mV | 1) | PRQ-81 |
| Switch peak over current threshold - BUCK | $V_{SWCS\_buck}$ | -60 | -50 | -40 | mV | 1) | PRQ-82 |
| Soft Start pull up current | $I_{Soft\_Start\_PU}$ | 22 | 26 | 32 | µA | $V_{Soft\_Start}$ = 1 V | PRQ-83 |
| Soft Start pull down current | $I_{Soft\_Start\_PD}$ | 2.2 | 2.6 | 3.2 | µA | $V_{Soft\_Start}$ = 1 V | PRQ-84 |
| Soft start latch-OFF threshold | $V_{Soft\_Start\_LOFF}$ | 1.65 | 1.75 | 1.85 | V | – | PRQ-85 |
| Soft start reset threshold | $V_{Soft\_Start\_RESET}$ | 0.1 | 0.2 | 0.3 | V | – | PRQ-86 |
| Soft start voltage during regulation | $V_{Soft\_Start\_reg}$ | 1.9 | 2 | 2.1 | V | 1) No Faults | PRQ-87 |
| Average switching frequency | $f_{SW}$ | 280 | 300 | 320 | kHz | $T_J$ = 25°C; $R_{FREQ}$= 37.4 kΩ; Average value (spread spectrum modulator always on) | PRQ-88 |
| Gate driver undervoltage threshold | $V_{BST1,2-VSWN1,2\_UVth}$ | 3.4 | – | 4 | V | $V_{BST1,2\ -\ VSWN1,2}$ decreasing; Differential signal (not referred to GND) | PRQ-89 |

**(table continues...)**

**Table 7 (continued) Electrical characteristics**

$V_{IN}$ = 8 V to 36 V, $T_J$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| HSGD1,2 NMOS driver on-state resistance (Gate Pull Up) | $R_{DS(ON\_PU)HS}$ | 1.4 | 2.3 | 3.7 | Ω | $V_{BST1,2 - VSWN1,2}$ = 5 V; $I_{source}$ = 100 mA | PRQ-90 |
| HSGD1,2 NMOS driver on-state resistance (Gate Pull Down) | $R_{DS(ON\_PD)HS}$ | 0.6 | 1.2 | 2.2 | Ω | $V_{BST1,2 - VSWN1,2}$ = 5 V; $I_{sink}$ = 100 mA | PRQ-91 |
| LSGD1,2 NMOS driver on-state resistance (Gate Pull Up) | $R_{DS(ON\_PU)LS}$ | 1.4 | 2.3 | 3.7 | Ω | $V_{IVCC}$ = 5 V; $I_{source}$ = 100 mA | PRQ-92 |
| LSGD1,2 NMOS driver on-state resistance (Gate Pull Down) | $R_{DS(ON\_PD)LS}$ | 0.4 | 1.2 | 2.5 | Ω | $V_{IVCC}$ = 5 V; $I_{sink}$ = 100 mA | PRQ-93 |
| HSGD1,2 Gate driver peak sourcing current | $I_{HSGD1,2\_SRC}$ | 380 | – | – | mA | [1] $V_{HSGD1,2 - VSWN1,2}$ = 1 V to 4 V; $V_{BST1,2 - VSWN1,2}$ = 5 V | PRQ-161 |
| HSGD1,2 Gate driver peak sinking current | $I_{HSGD1,2\_SNK}$ | 410 | – | – | mA | [1] $V_{HSGD1,2}$ - $V_{SWN1,2}$ = 4 V to 1 V; $V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V | PRQ-162 |
| LSGD1,2 Gate driver peak sourcing current | $I_{LSGD1,2\_SRC}$ | 370 | – | – | mA | [1] $V_{LSGD1,2}$ = 1 V to 4 V; $V_{IVCC}$ = 5 V | PRQ-163 |
| LSGD1,2 Gate driver peak sinking current | $I_{LSGD1,2\_SNK}$ | 550 | – | – | mA | [1] $V_{LSGD1,2}$ = 4 V to 1 V; $V_{IVCC}$ = 5 V | PRQ-164 |
| LSGD1,2 OFF to HSGD1,2 ON delay | $t_{LSOFF-HSON\_delay}$ | 15 | 30 | 40 | ns | [1] | PRQ-98 |
| HSGD1,2 OFF to LSGD1,2 ON delay | $t_{HSOFF-LSON\_delay}$ | 35 | 60 | 75 | ns | [1] | PRQ-99 |

1) Not subject to production test, specified by design

# 6 Digital dimming function

PWM dimming is adopted to vary LEDs brightness with greatly reduced chromaticity shift. PWM dimming achieves brightness reduction by varying the duty cycle of a constant current in the LED string.

## 6.1 Description

**PWM via direct interface**

Pulse width modulated (PWM) signals can be applied to the PWMI pin. The gate drivers are enabled if the signal is on high level and they are disabled if the the signal is at low level.

The applied PWM signal shall have a frequency above $f_{PWM,min.}$

PWMO pin replicates PWMI pin HIGH or LOW state, unless one of the following conditions occur:

- Output overvoltage event
- Output short to ground event
- Thermal shutdown

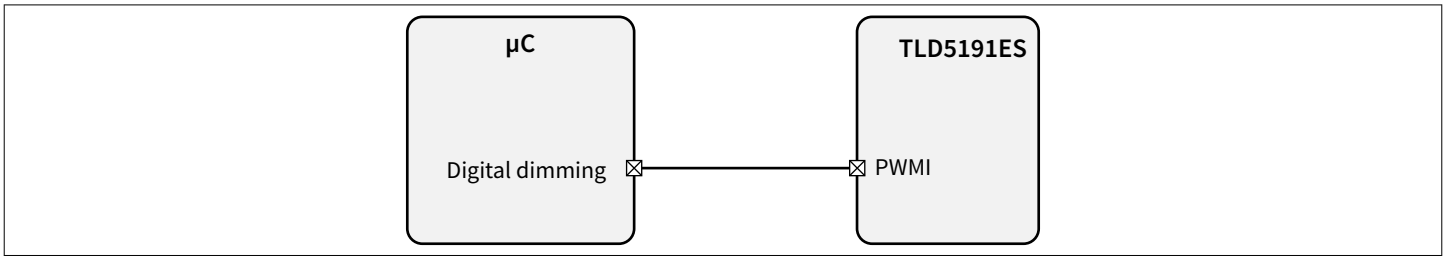



**Figure 17 Digital dimming overview**

PWM dimming in LOW states can be used to suspend the output current for long time intervals in a safe manner. Indeed a soft start routine is applied once the channel is enabled if the PWM input signal has been kept below $V_{PWMI,DC\_0}$ for at least $t_{PWMI,OFF}$.

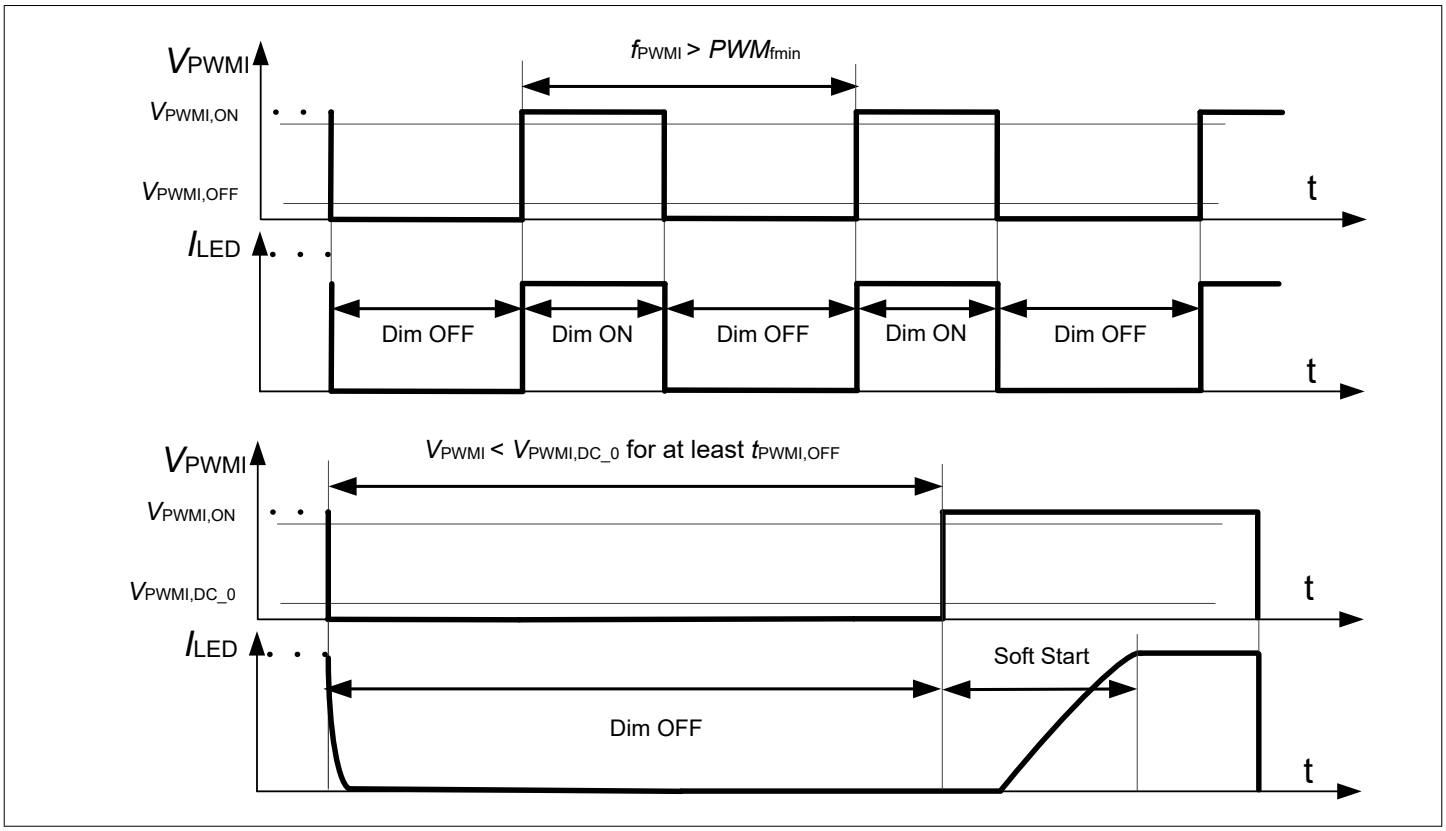



**Figure 18 PWMI timings diagrams**

### PWM via embedded PWM engine

If an analog signal in between $V_{PWMI,DC\_0}$ and $V_{PWMI,DC\_100}$ is applied, embedded PWM is activated.
The embedded PWM engine has an 8 bit resolution with a fixed internal frequency of $f_{PWM}$.

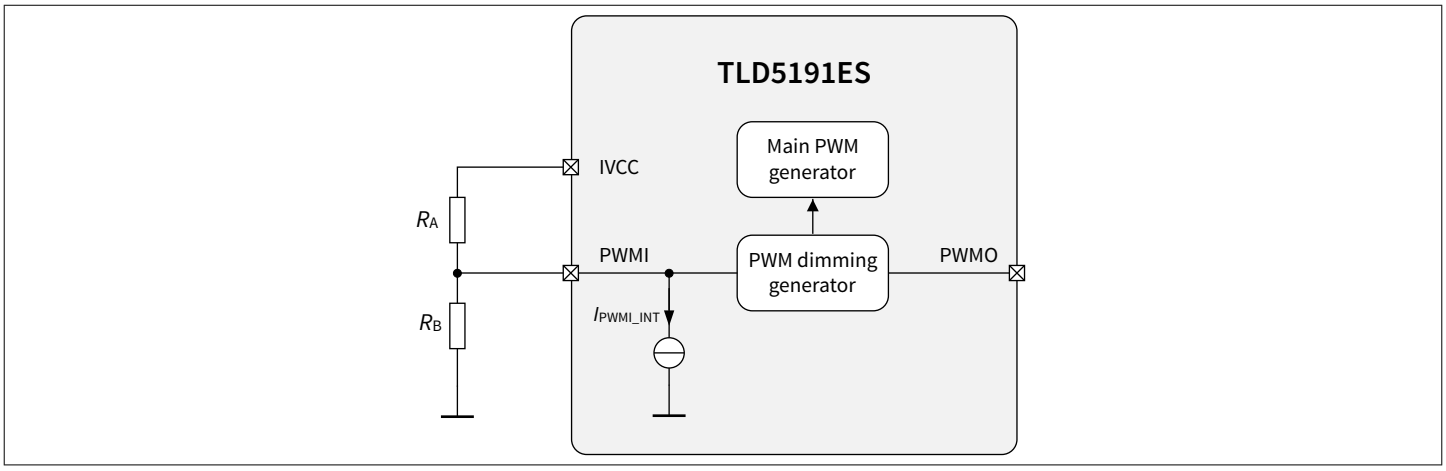



**Figure 19 Block diagram of embedded PWM generator**

*Note: A non linear embedded PWM engine is implemented to guarantee high accuracy for low values of duty cycle. It helps the headlamp designers to achieve high LED brightness accuracy when dimming to low duty cycle values. Moreover it helps to produce smooth fading curve, compensating the logarithmic change in the perceived brightness.*

PWMO pin replicates the frequency and duty cycle of the embedded PWM engine, unless one of the following conditions occur:

- Output overvoltage event
- Output short to ground event
- Thermal shutdown

The duty cycle produced by the embedded PWM engine is a function of the voltage applied on PWMI pin.
The duty cycle is quantized with different LSB step values in the following $V_{PWMI}$ ranges:

- 0.142% for $V_{PWMI,DC\_0} \le V_{PWMI} \le 0.23 \cdot V_{IVCC}$
- 0.284% for $0.23 \cdot V_{IVCC} < V_{PWMI} \le 0.28 \cdot V_{IVCC}$
- 0.569% for $0.28 \cdot V_{IVCC} < V_{PWMI} \le V_{PWMI,DC\_100}$

and can be calculated by the following formulas:

$$DC\,\% = 63 \cdot \left( \frac{V_{PWMI} - 0.18 \cdot V_{IVCC}}{0.05 \cdot V_{IVCC}} \right) \cdot 0.142\,\% \quad for \quad V_{PWMI,DC\_0} \le V_{PWMI} \le 0.23 \cdot V_{IVCC} \tag{5}$$

$$DC\,\% = 8.95\,\% + 64 \cdot \left( \frac{V_{PWMI} - 0.23 \cdot V_{IVCC}}{0.05 \cdot V_{IVCC}} \right) \cdot 0.284\,\% \quad for \quad 0.23 \cdot V_{IVCC} < V_{PWMI} \le 0.28 \cdot V_{IVCC} \tag{6}$$

$$DC\,\% = 27.13\,\% + 128 \cdot \left( \frac{V_{PWMI} - 0.28 \cdot V_{IVCC}}{0.1 \cdot V_{IVCC}} \right) \cdot 0.569\,\% \quad for \quad 0.28 \cdot V_{IVCC} < V_{PWMI} \le V_{PWMI,DC\_100} \tag{7}$$

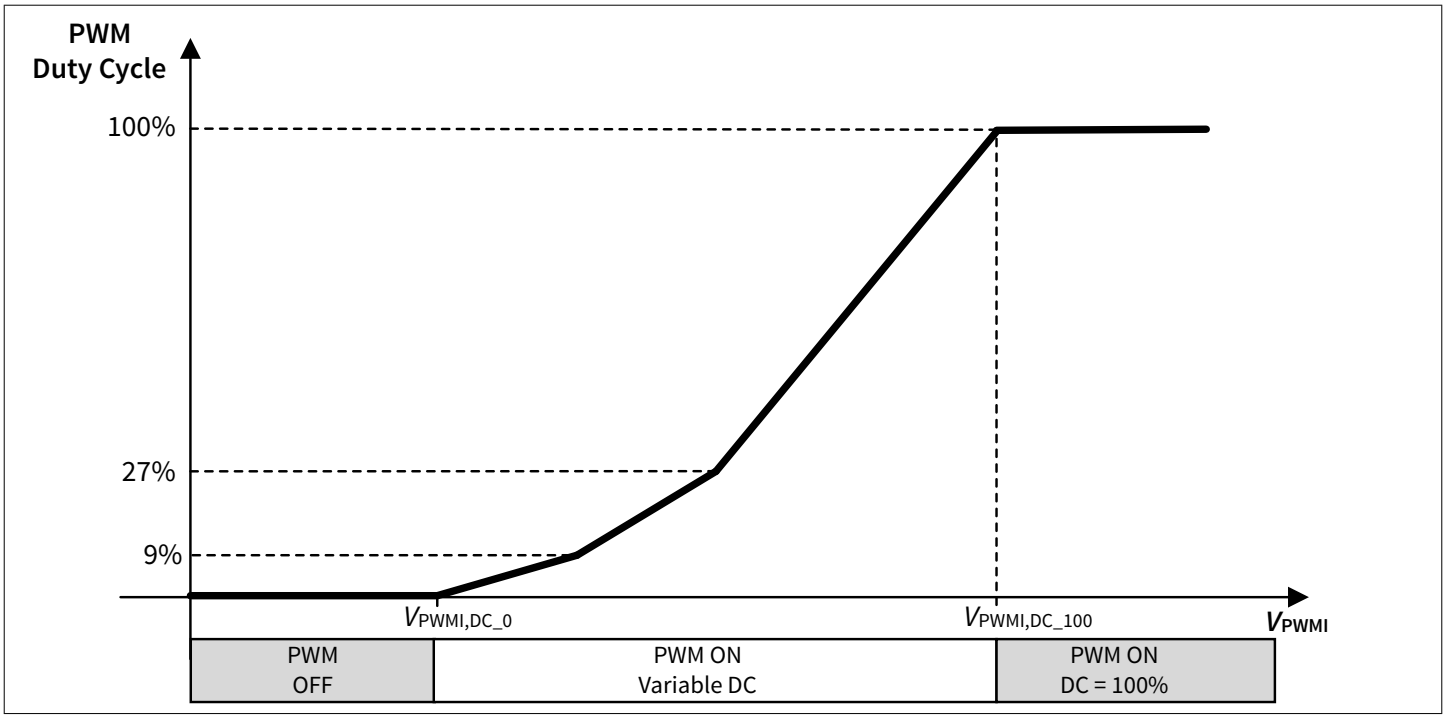



**Figure 20 Analog PWM DC curve**

## 6.2 Electrical characteristics

**Table 8 Electrical characteristics**

$V_{IN}$ = 8 V to 36 V, $T_J$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| PWMI Turn on threshold | $V_{PWMI,ON}$ | – | – | 2 | V | – | PRQ-100 |
| PWMI Turn off threshold | $V_{PWMI,OFF}$ | 0.8 | – | – | V | – | PRQ-101 |
| PWMI Off time threshold | $t_{PWMI,OFF}$ | – | – | 25 | ms | 1) | PRQ-199 |
| PWMI Minimum frequency | $f_{PWM,min}$ | 75 | – | – | Hz | 1) | PRQ-202 |
| PWM Engine minimum voltage | $V_{PWMI,DC\_0}$ | 0.176* $V_{IVCC}$ | 0.18* $V_{IVCC}$ | – | V | – | PRQ-102 |
| PWM Engine maximum voltage | $V_{PWMI,DC\_100}$ | – | 0.38* $V_{IVCC}$ | 0.387* $V_{IVCC}$ | V | – | PRQ-103 |
| PWM Engine DC | $PWM_{DC\_15\%}$ | 14.25 | 15 | 15.75 | % | $V_{PWMI}$ = 0.246*$V_{IVCC}$ | PRQ-104 |
| PWM Engine frequency | $f_{PWM}$ | 220 | 275 | 330 | Hz | – | PRQ-105 |
| PWMI Internal pull down current | $I_{PWMI\_INT}$ | 1.5 | – | 3.5 | uA | 1) $V_{PWMI}$ = 0.2*$V_{IVCC}$ | PRQ-106 |
| PWMO Gate driver sourcing current | $I_{PWMO\_SRC}$ | -40 | -22 | -10 | mA | 1) $V_{PWMO}$ = 2.5 V; $V_{IVCC}$ = 5 V | PRQ-109 |

**(table continues...)**

**Table 8 (continued) Electrical characteristics**

$V_{IN}$ = 8 V to 36 V, $T_J$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| PWMO Gate driver sinking current | $I_{PWMO\_SNK}$ | 10 | 25 | 40 | mA | 1) $V_{PWMO}$ = 2.5 V; $V_{IVCC}$ = 5 V | PRQ-110 |
| PWMO Gate driver rise time | $t_{R,PWMO}$ | 200 | 450 | 700 | ns | 1) $C_{gate}$ = 2.2 nF; $V_{PWMO}$ = 1 V to 4 V | PRQ-111 |
| PWMO Gate driver fall time | $t_{F,PWMO}$ | 150 | 375 | 600 | ns | 1) $C_{gate}$ = 2.2 nF; $V_{PWMO}$ = 4 V to 1 V | PRQ-112 |
| PWMO Gate driver supply voltage | $V_{PWMO}$ | 4.8 | 5 | 5.2 | V | – | PRQ-113 |

1) Not subject to production test, specified by design

# 7 Analog dimming

The analog dimming feature allows further control of the output current. This approach is used to:

- Reduce the default current in a narrow range to adjust to different binning classes of the used LEDs
- Adjust the load current to enable the usage of one hardware for several LED types where different current levels are required
- Reduce the current at high temperatures (protect LEDs from overtemperature)
- Reduce the current at low input voltages (for example, cranking-pulse breakdown of the supply or power derating)

## 7.1 Description

The analog dimming feature is adjusting the average load current level via the control of the feedback error amplifier voltage ($V_{FBH-FBL}$).

The SET pin is used to adjust the mean output current/voltage. The $V_{SET}$ range where analog dimming is enabled is from 200 mV to 1.5 V.

Different application scenarios are described in Figure 22.

**Using the SET pin to adjust the output current:**

For the calculation of the output current IOUT the following equation is used:

$$I_{OUT} = \frac{V_{FBH-FBL}}{R_{FB}} \tag{8}$$

A decrease of the average output current can be achieved by controlling the voltage at the SET pin ($V_{SET}$) between 0.2 V and 1.4 V. The mathematical relation is given in the formula below:

$$I_{OUT} = \frac{V_{SET} - 200mV}{R_{FB} \cdot 8} \tag{9}$$

If $V_{SET}$ is 200 mV (typ.) the LED current is only determined by the internal offset voltages of the comparators.

To assure the switching activity is stopped and $I_{OUT} = 0$, $V_{SET}$ has to be < 100 mV.

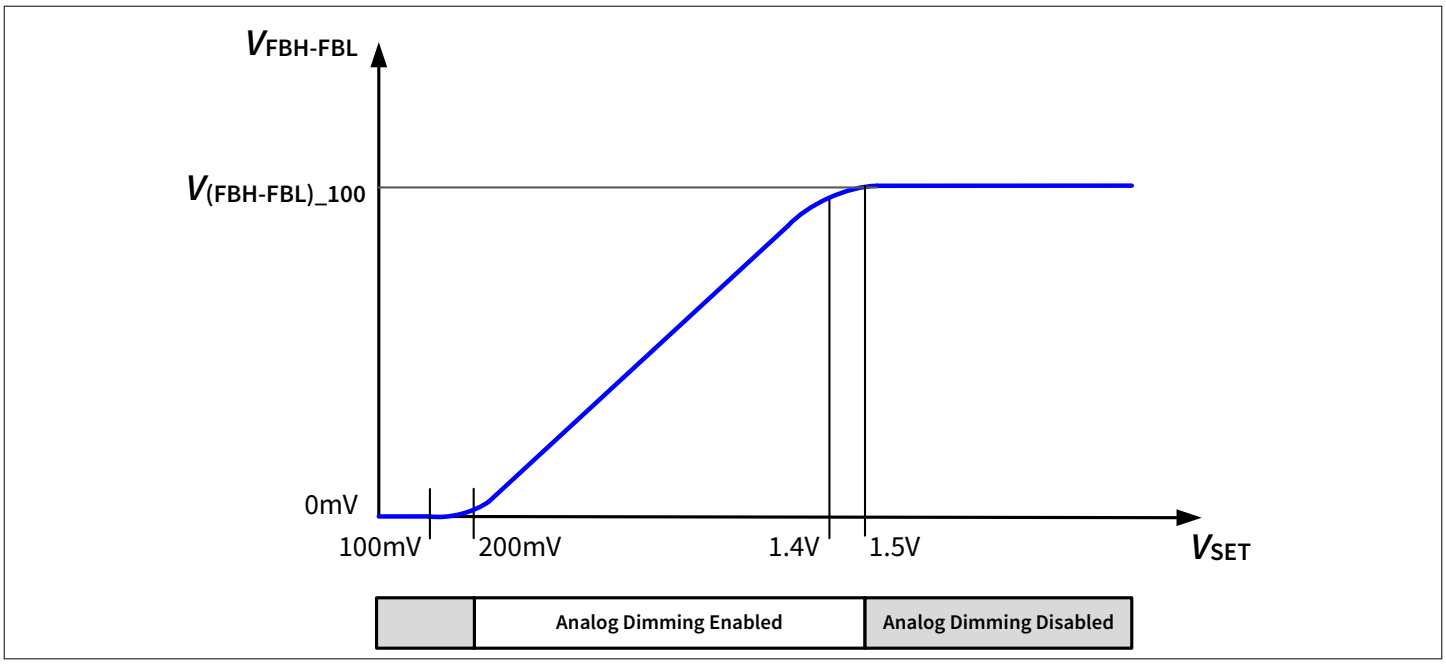



**Figure 21 Analog dimming overview**

### Multi-purpose usage of the analog dimming feature

1. A µC integrated digital analog converter (DAC) output or a stand alone DAC can be used to supply the SET pin of the TLD5191ES.
2. The usage of an external resistor divider connected between IVCC, SET and GND can be chosen for systems without µC on board. The concept allows control of the LED current by placing low power resistors.
3. Furthermore a temperature sensitive resistor (thermistor) to protect the LED loads from thermal destruction can be connected.
4. If the analog dimming feature is not needed, the SET pin should be connected to the IVCC pin.
5. Instead of a DAC, the µC can provide a PWM signal and an external R-C filter to produce a constant voltage for the analog dimming. The voltage level depends on the duty cycle which can be controlled by the µC software after reading the coding resistor placed on the LED module.

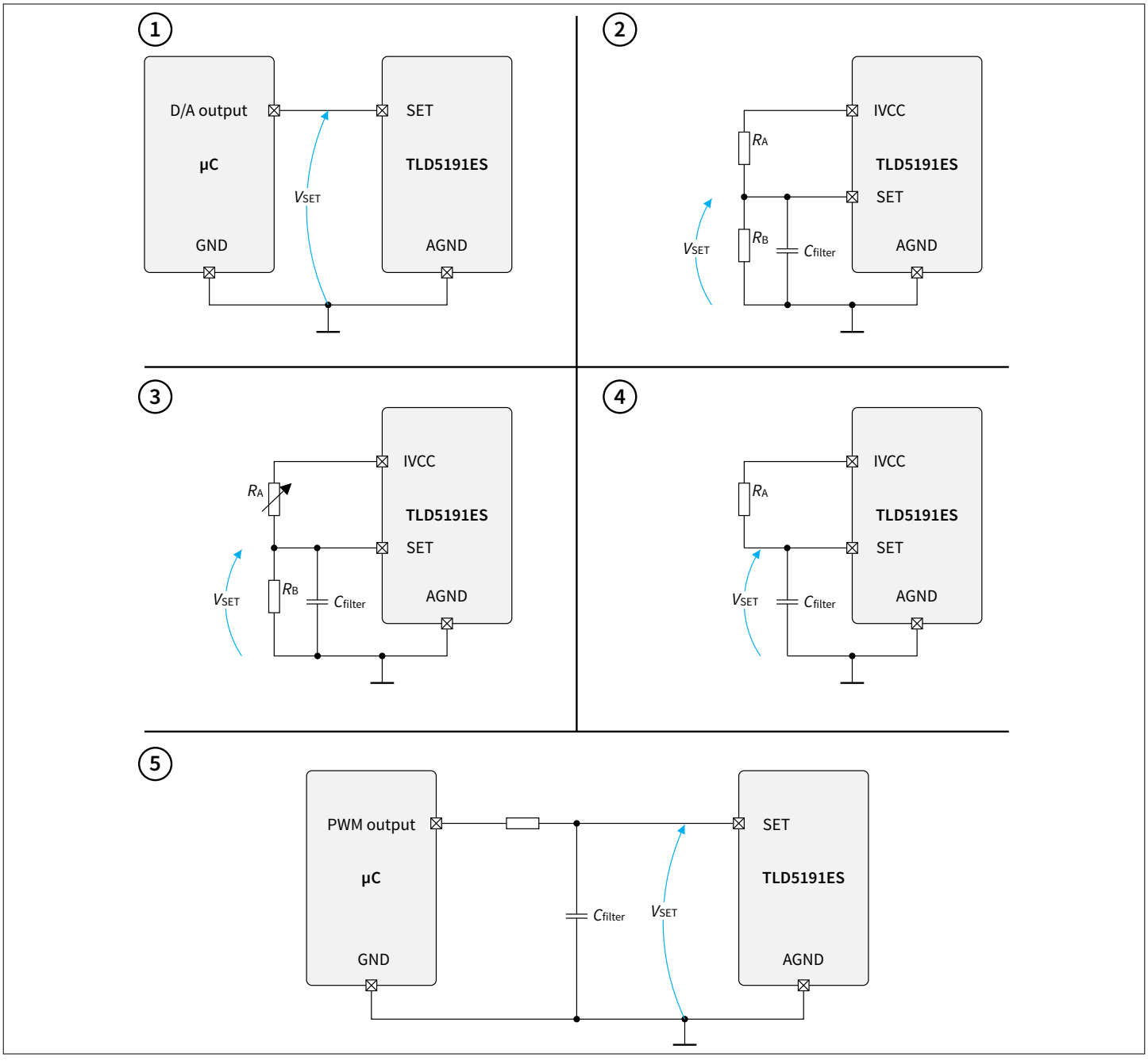



**Figure 22 Different use cases for analog dimming pin SET**

## 7.2 Electrical characteristics

**Table 9 Electrical characteristics**

$V_{IN}$ = 8V to 36V, $T_J$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Source current on SET pin | $I_{SET\_source}$ | – | – | 1 | µA | 1) $V_{SET}$ = 0.2 V to 1.4 V | PRQ-114 |

1) Not subject to production test, specified by design

# 8 Linear regulator

The TLD5191ES features an integrated voltage regulator for the supply of the internal gate driver stages.

## 8.1 IVCC description

Internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to $I_{LIM}$. An external output capacitor with low ESR is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches. A minimum capacitance value is given in parameter $C_{IVCC}$.

**Integrated undervoltage protection for the external switching MOSFET**

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage. If the voltage on IVCC pin falls below $V_{IVCC\_RTH,d}$ the gate drivers are turned OFF.

The undervoltage reset threshold for the IVCC pin helps to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of the external logic level n-channel MOSFETs.

## 8.2 Electrical characteristics

**Table 10 Electrical characteristics**

$V_{IN}$ = 8V to 36V, $T_J$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Output voltage | $V_{IVCC}$ | 4.8 | 5 | 5.2 | V | $V_{VIN}$ = 13.5 V; 0.1 mA ≤ $I_{IVCC}$ ≤ 50 mA | PRQ-134 |
| Output current limitation | $I_{LIM}$ | 70 | 90 | 110 | mA | 1) $V_{IVCC}$ = 4 V | PRQ-135 |
| Drop out voltage | $V_{DR}$ | – | 200 | 350 | mV | $V_{VIN}$ = 5 V; $I_{IVCC}$ = 10 mA | PRQ-136 |
| IVCC buffer capacitor | $C_{IVCC}$ | 10 | – | – | µF | 1) 2) | PRQ-137 |
| IVCC undervoltage reset switch OFF threshold | $V_{IVCC\_RTH,d}$ | 3.7 | 3.9 | 4.1 | V | 3) $V_{IVCC}$ decreasing | PRQ-138 |
| IVCC undervoltage hysterisis | $V_{IVCC\_HYST}$ | 0.31 | 0.34 | 0.37 | V | $V_{IVCC}$ increasing; | PRQ-139 |

1) not subject to production test, specified by design
2) minimum value given is needed for regulator stability; application might need higher capacitance than the minimum. Use capacitors with LOW ESR
3) selection of external switching MOSFET is crucial and the $V_{IVCC,RTH,d}$ min, as worst case the threshold voltage of MOSFET must be considered

# 9 Protection and diagnostic functions

## 9.1 Description

The TLD5191ES has integrated circuits to diagnose and protect against overvoltage, short circuits of the load and overtemperature faults.

In IDLE state only the overtemperature shut-down is reported according to specifications.

In Figure 23 a summary of the protection, diagnostic and monitor functions is displayed.

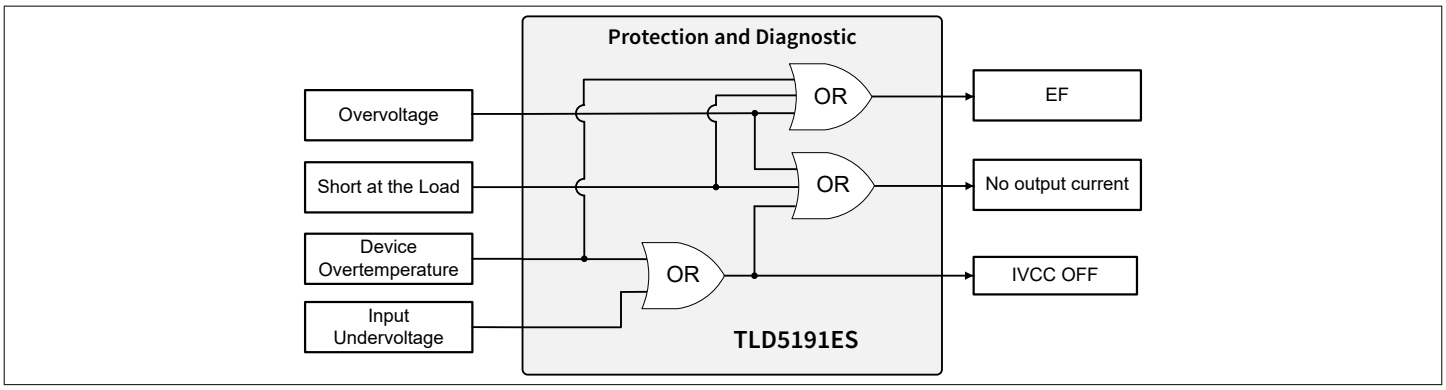



**Figure 23 Protection and diagnostic overview - TLD5191ES**

## 9.2 Output overvoltage, short circuit protection

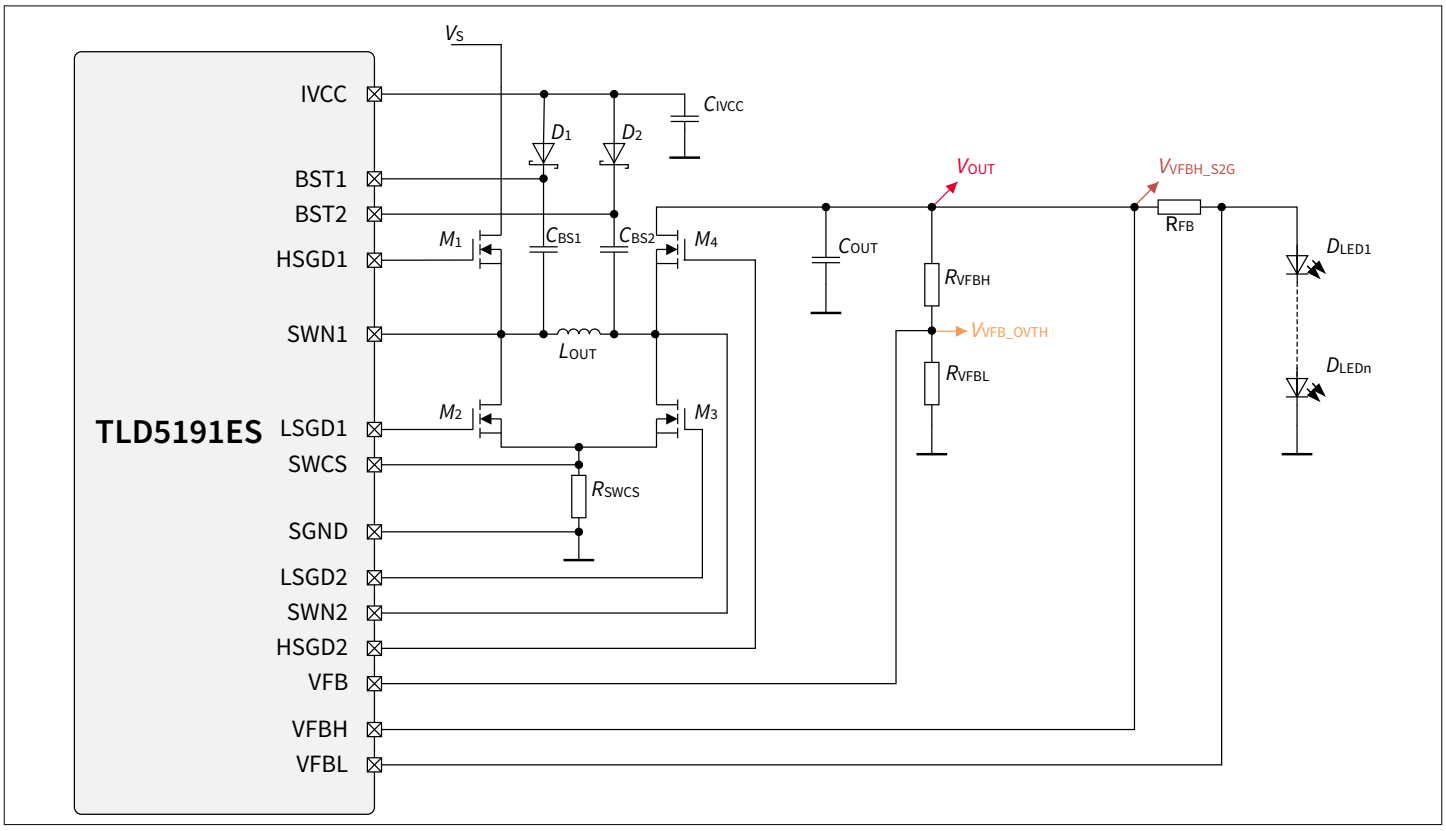



**Figure 24 Protections pins - overview**

### 9.2.1 Short circuit protection

The device detects a short circuit at the output if this condition is verified:

- The pin $V_{FBH}$ falls below the threshold voltage $V_{VFBH\_S2G\_dec}$ for at least $t_{S2G\_mask}$.

During the rising edge of the soft-start the short circuit detection is ignored until $V_{SOFT\_START\_LOFF}$.

The TLD5191ES provides an open-drain status pin, EF, which pulls low when the short circuit is detected.

In case of short circuit detection, the SOFT START pin is used to implement a fault mask and wait-before-retry time, on rising and falling edge respectively. See Figure 8 for more details.

*Note: If the short circuit condition disappears, the device will re-start with the soft start routine as described in Chapter 5.2.*

### 9.2.2 Overvoltage protection

TLD5191ES integrates an output overvoltage protection by monitoring the voltage on the VFB pin.

A voltage divider between VOUT, VFB pin and AGND is used to adjust the overvoltage protection threshold.

To fix the overvoltage protection threshold the following equation is used:

$$V_{OUT\_OV\_protected} = V_{VFB\_OVTH} \cdot \frac{R_{VFBH} + R_{VFBL}}{R_{VFBL}} \quad (10)$$

An overvoltage event is detected when $V_{VFB} > V_{VFB\_OVTH}$ and the device reacts as described below:

- Switching activity is disabled
- Mosfet $M_1$, $M_3$ and $M_4$ are kept OFF while mosfet $M_2$ is kept ON to discharge the inductor current to the output

Once the voltage $V_{VFB} < V_{VFB\_OVTH} - V_{VFB\_OVTH,HYS}$ the switching activity is resumed.

In case of overvoltage event at the output, the open-drain status pin EF will toggle to LOW. After the overvoltage event disappeared the device will auto restart and the status pin EF will toggle to HIGH.

*Note: During the overvoltage event the inductor current is discharged to the output, thus an output voltage increase may be observed based on the $L_{OUT}$ and $C_{OUT}$ design. The overvoltage threshold must be designed to avoid to exceed the device maximum absolute ratings.*

## 9.3 Device temperature monitoring

A temperature sensor is integrated on the chip. The temperature monitoring circuit compares the measured temperature to the shutdown threshold.

If the internal temperature sensor reaches the shut-down temperature $T_{J,SD}$, the IVCC regulator is shut down and the gate driver outputs are set to LOW.

The device exits from thermal shutdown condition with a soft start routine after the temperature measured by the integrated sensor decreases below $T_{J,SD} - T_{J,SD,hyst.}$

The TLD5191ES provides an open-drain status pin, EF, which pulls low when the shut-down temperature is reached.

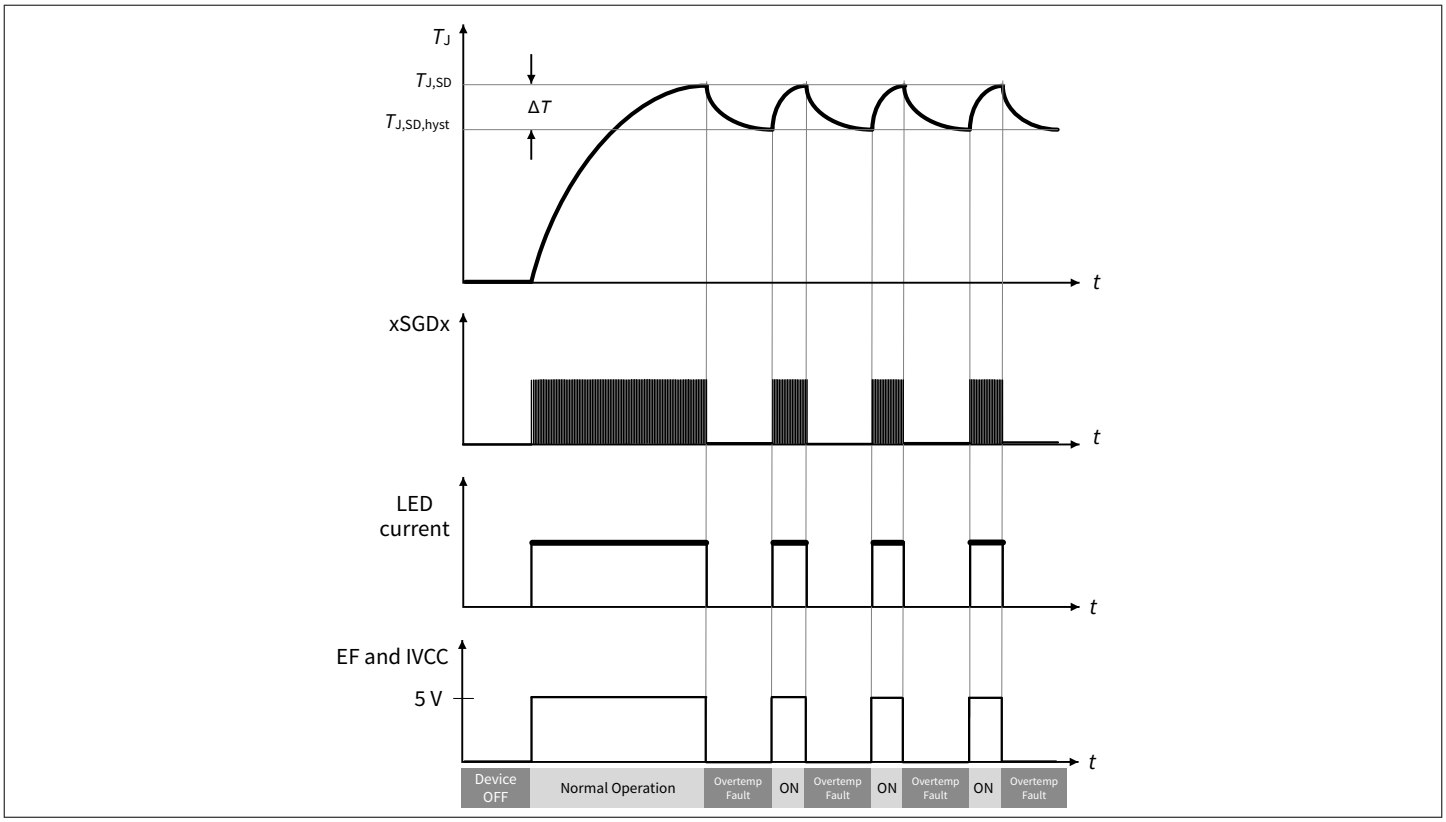



**Figure 25 Device overtemperature protection behavior**

## 9.4 Electrical characteristics

**Table 11 Electrical characteristics**

$V_{IN}$ = 8V to 36V, $T_J$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Short to GND exit threshold | $V_{FBH\_S2G\_inc}$ | 1.9 | 2 | 2.15 | V | $V_{FBH}$ increasing | PRQ-127 |
| Short to GND entry threshold | $V_{FBH\_S2G\_dec}$ | 1.65 | 1.75 | 1.85 | V | $V_{FBH}$ decreasing | PRQ-128 |
| Short to GND masking time | $t_{S2G\_mask}$ | – | 42 | 50 | µs | 1) | PRQ-203 |
| Over temperature shutdown | $T_{J,SD}$ | 160 | 175 | 190 | °C | 1) | PRQ-129 |
| Over temperature shutdown hysteresis | $T_{J,SD,hyst}$ | – | 10 | – | °C | 1) | PRQ-130 |
| VFB over voltage feedback threshold | $V_{VFB\_OVTH}$ | 1.42 | 1.46 | 1.50 | V | – | PRQ-131 |
| Output over voltage feedback hysteresis | $V_{VFB\_OVTH,HYS}$ | 25 | 40 | 58 | mV | Output Voltage decreasing | PRQ-132 |

**(table continues...)**

**Table 11 (continued) Electrical characteristics**

$V_{IN}$ = 8V to 36V, $T_J$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| EF pin output impedance | $R_{EF}$ | – | 2.1 | – | kΩ | 1) Fault Condition<br>$I$ = 100 µA | PRQ-133 |

1) specified by design; not subject to production test

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

# 10 Infineon FLAT SPECTRUM feature

## 10.1 Description

The Infineon FLAT SPECTRUM feature has the target to minimize external additional filter circuits.

## 10.2 Spread spectrum

The spread spectrum modulation technique significantly improves the lower frequency range of the spectrum ($f$ < 30 MHz).

By using the spread spectrum technique, it is possible to optimize the input filter only for the peak limits, and also pass the average limits (average emission limits are -20 dB lower than the peak emission limits). By using spread spectrum, the need for low ESR input capacitors is relaxed because the input capacitor series resistor is important for the low frequency filter characteristic. This can be an economic benefit if there is a strong requirement for average limits.

The TLD5191ES features a built in spread spectrum function always activated with modulation frequency $f_{FM}$ and a frequency deviation $f_{dev}$.

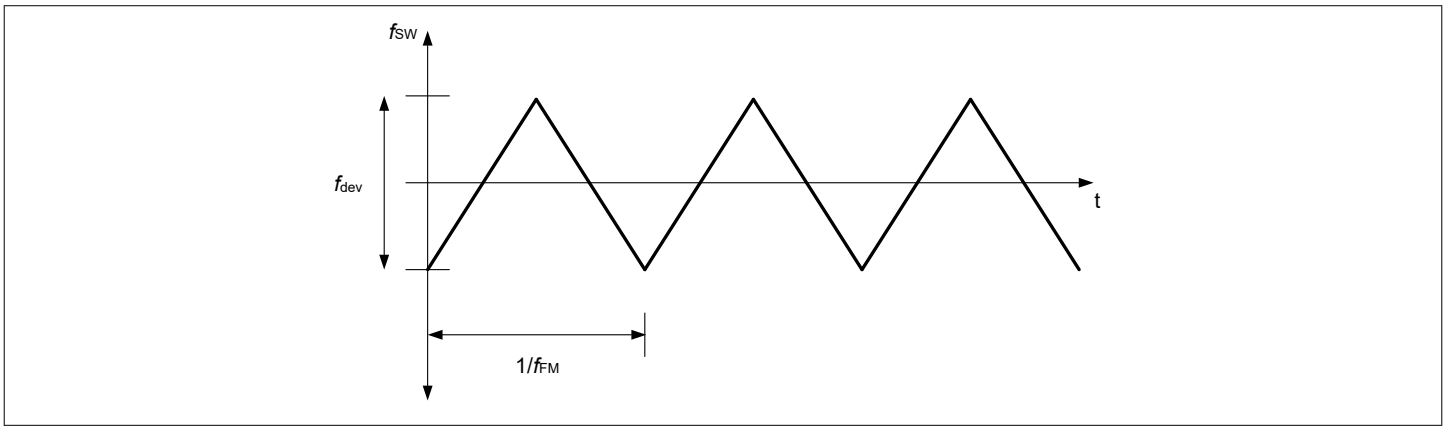



**Figure 26 Spread spectrum overview**

## 10.3 Electrical characteristics

**Table 12 Electrical Characteristics**

$V_{IN}$ = 8V to 36V, $T_J$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Frequency deviation | $f_{dev}$ | – | ±20 | – | % | 1) | PRQ-140 |
| Frequency modulation | $f_{FM}$ | – | 12 | – | kHz | 1) | PRQ-141 |

1) specified by design; not subject to production test

# 11 Application information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

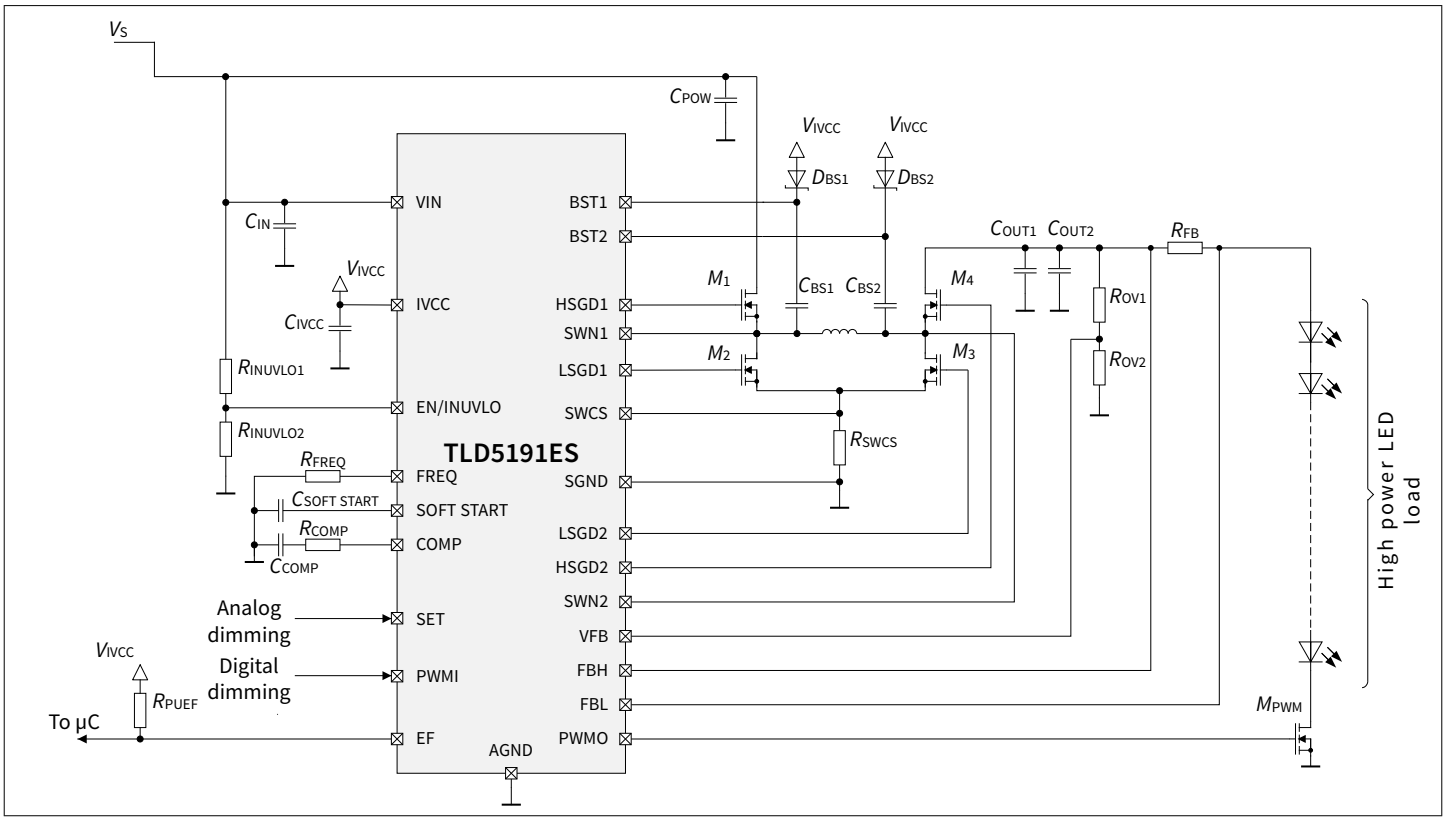



**Figure 27 Application drawing - TLD5191ES as current regulator**

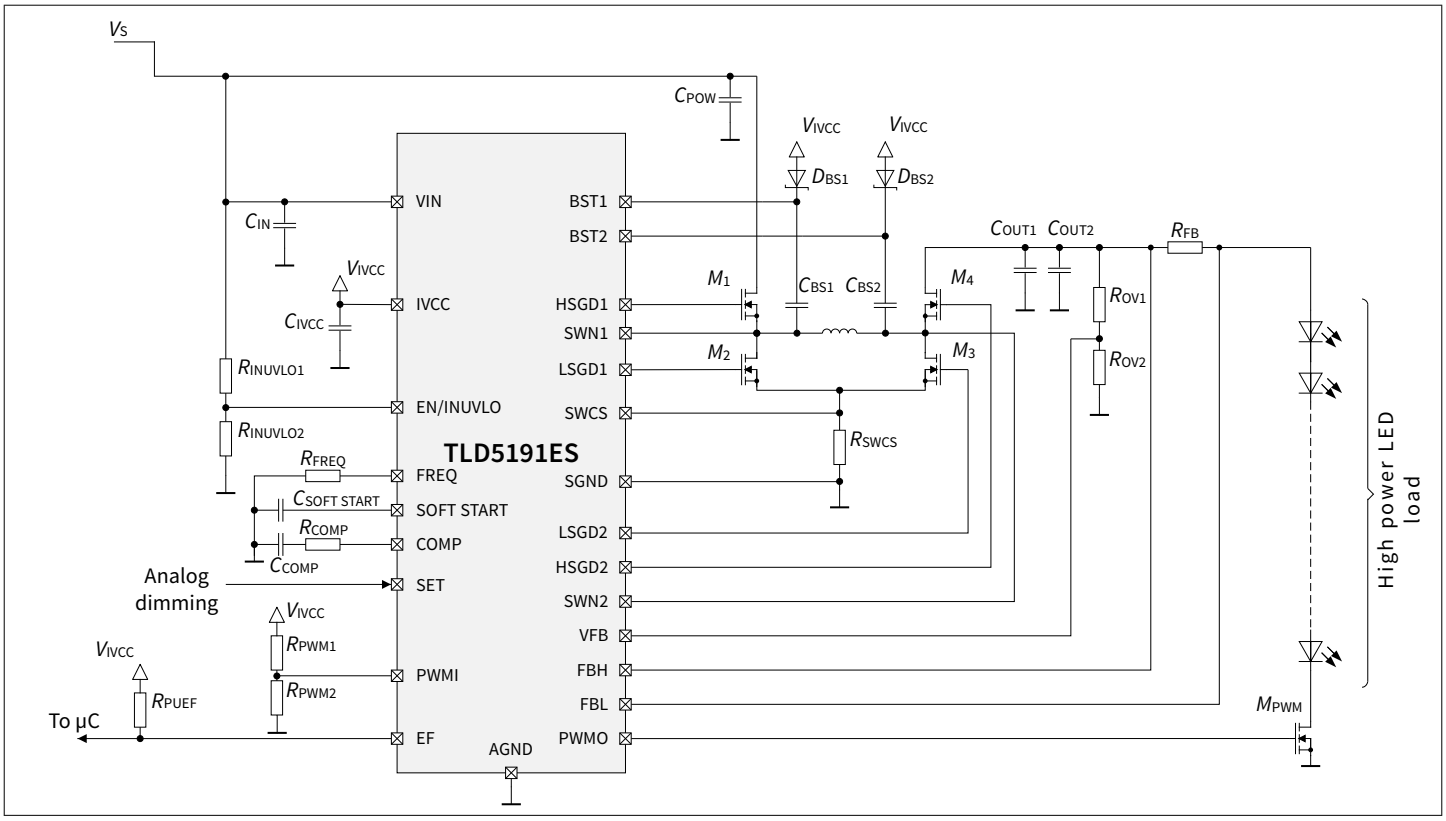



**Figure 28 Application drawing - TLD5191ES as current regulator with PWM engine**

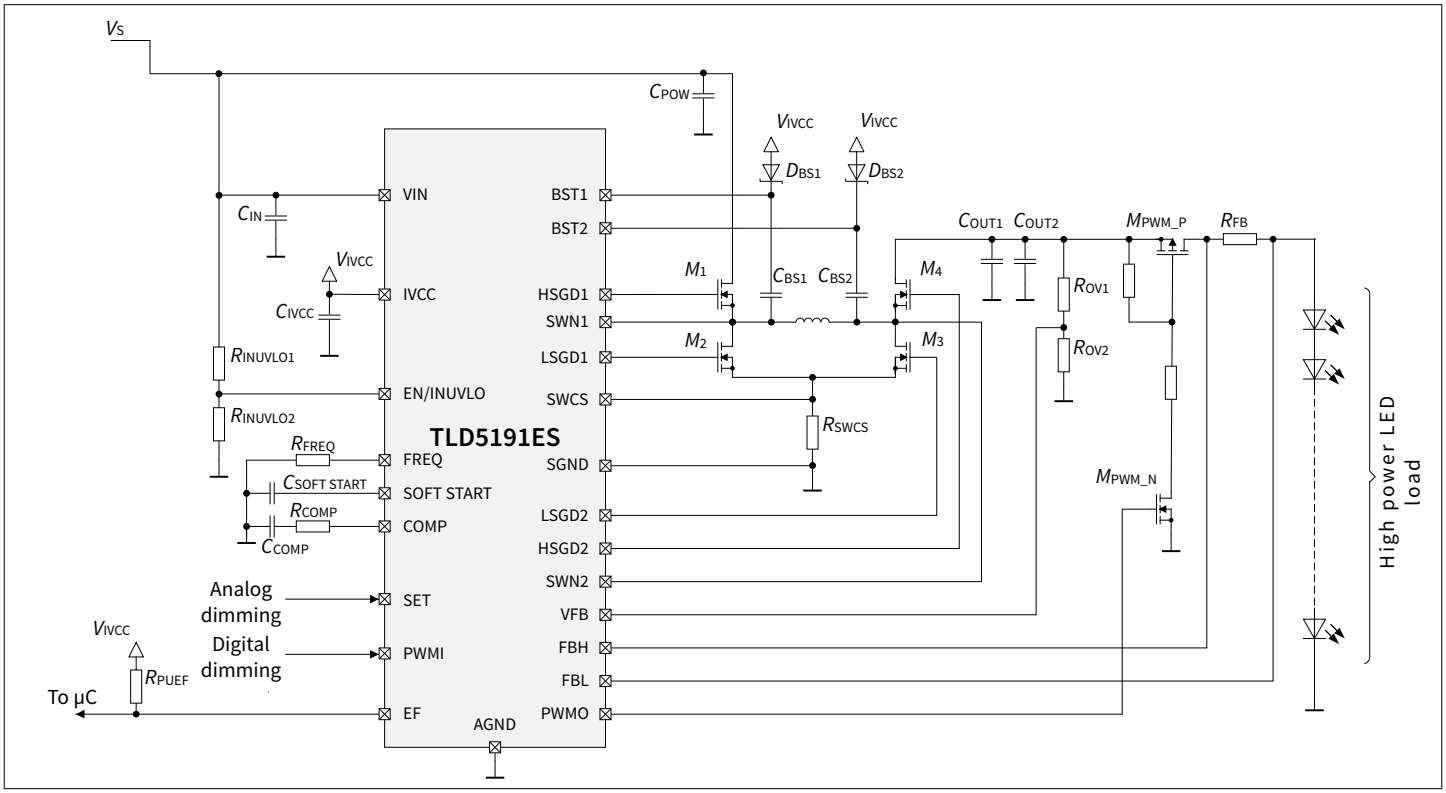



**Figure 29 Application drawing - TLD5191ES as current regulator with dimming PMOS**

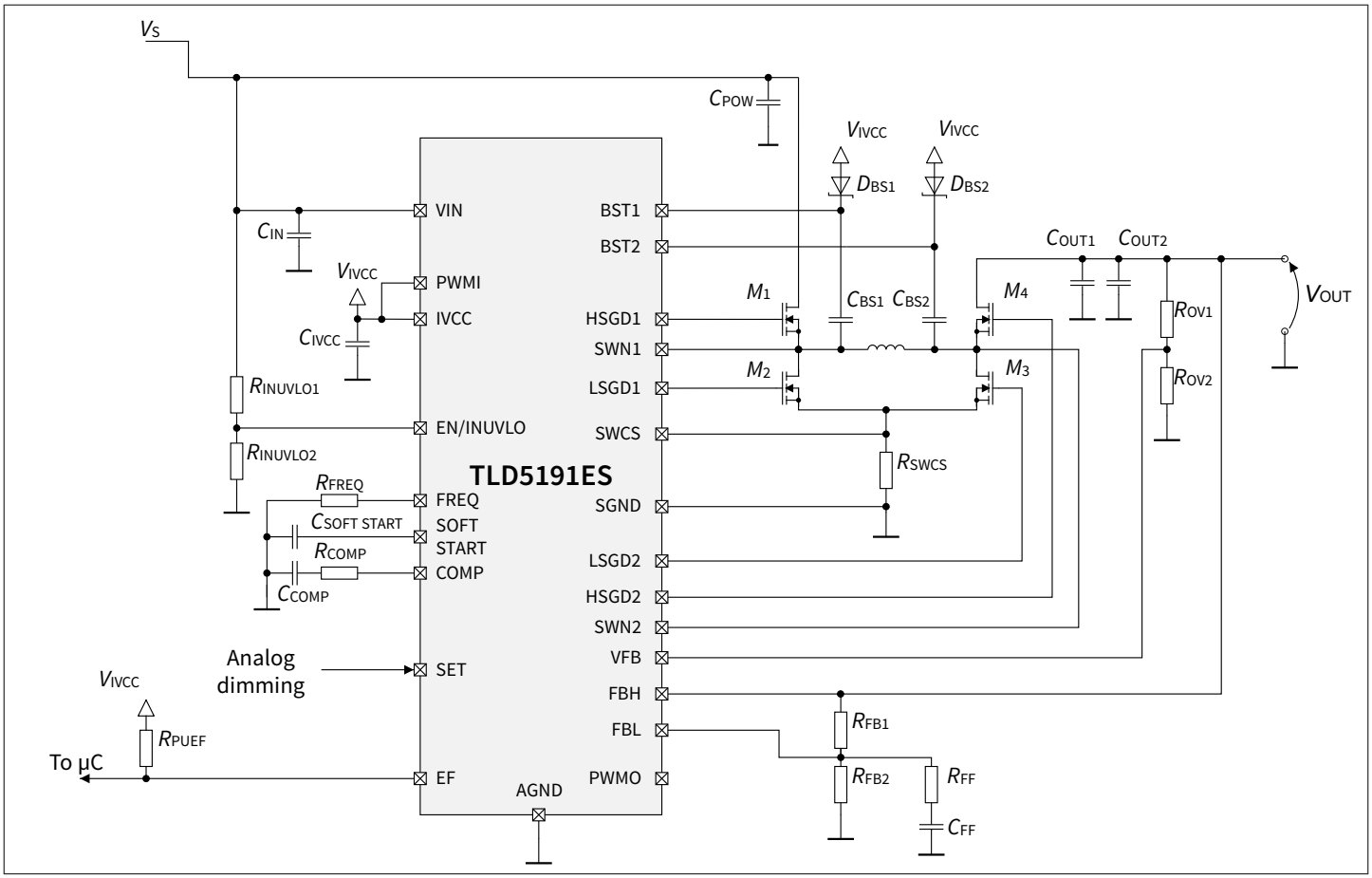



**Figure 30 Application drawing - TLD5191ES voltage mode**

# 12 Package dimensions

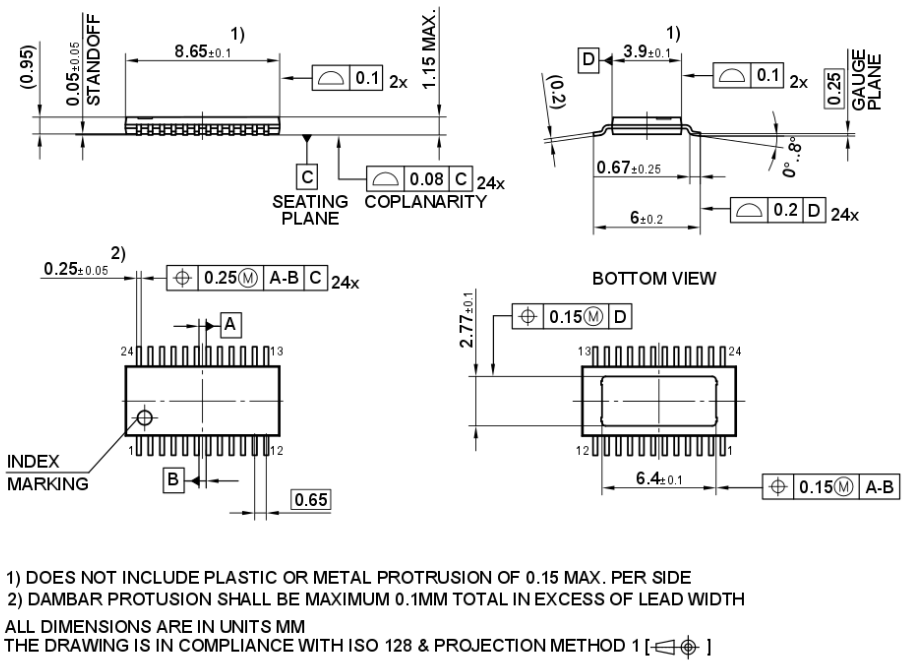



**Figure 31 PG-TSDSO-24 package outline**

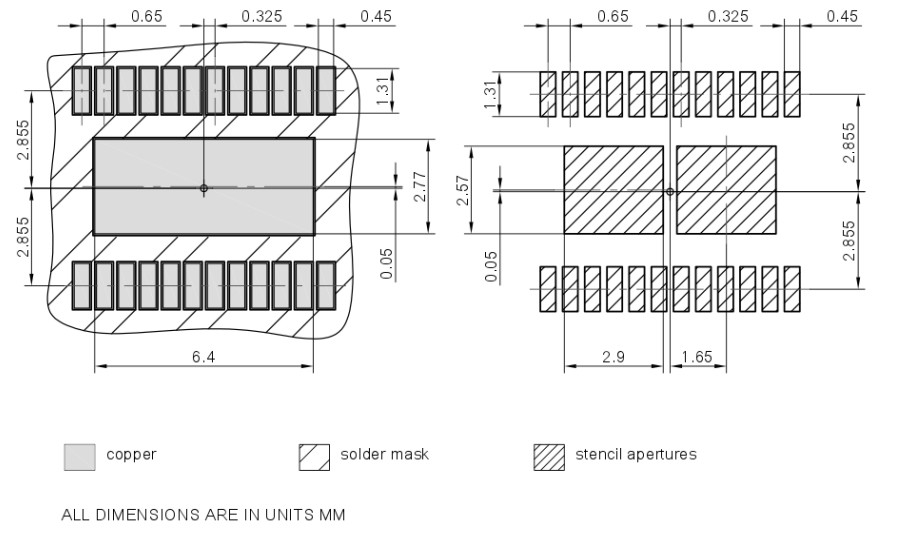



**Figure 32 PG-TSDSO-24 package pads and stencil**

**Green Product (RoHS compliant)** To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website: https://www.infineon.com/packages

# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| Rev.1.00 | 2022-02-18 | Datasheet release |

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