

# RF LDMOS Wideband Integrated Power Amplifiers

The MDE6IC7120N/GN wideband integrated circuit is designed with on-chip matching that makes it usable from 728 to 768 MHz. This multi-stage structure is rated for 26 to 32 Volt operation and covers all typical cellular base station modulation formats.

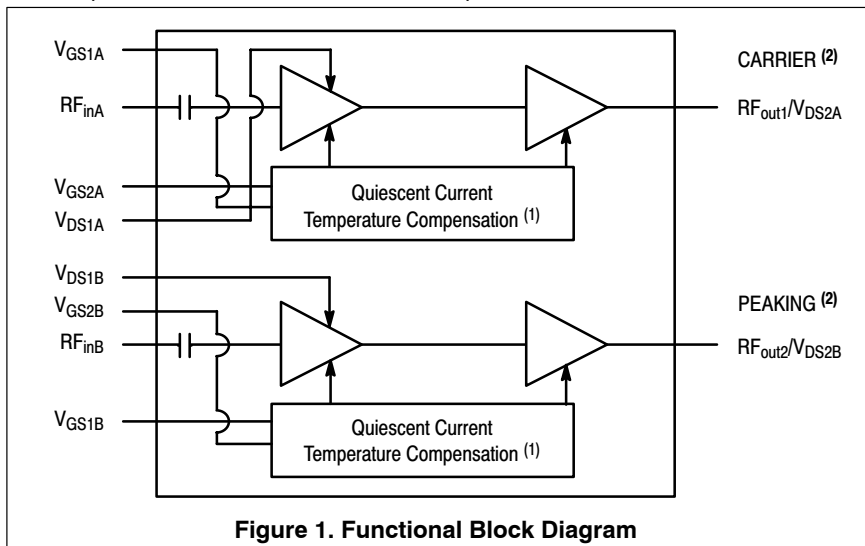
- Typical Doherty Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ1A} = I_{DQ1B} = 80$  mA,  $I_{DQ2A} = 550$  mA,  $V_{G2B} = 2.3$  Vdc,  $P_{out} = 25$  Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
728 MHz	35.0	42.0	6.2	-39.0
748 MHz	34.4	40.6	6.8	-41.3
768 MHz	33.8	39.1	6.9	-37.3

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 748 MHz, 104 Watts CW Output Power (2 dB Input Overdrive from Rated  $P_{out}$ ), Designed for Enhanced Ruggedness
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 100 mW to 120 Watts CW  $P_{out}$
- Typical  $P_{out}$  @ 1 dB Compression Point  $\approx$  120 Watts CW

### Features

- Production Tested in a Symmetrical Doherty Configuration
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel

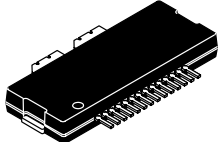


**Figure 1. Functional Block Diagram**

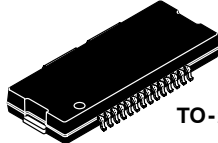
**MDE6IC7120NR1**  
**MDE6IC7120GNR1**

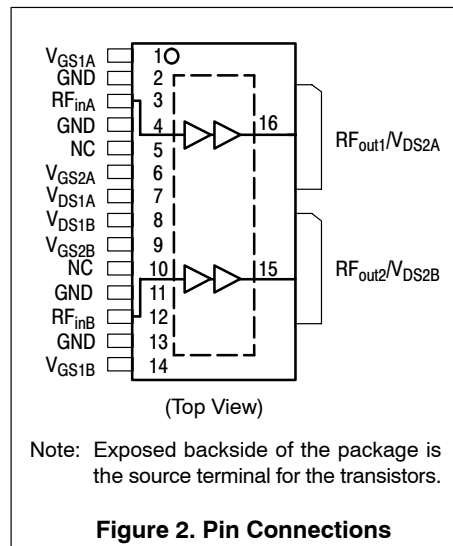
**728-768 MHz, 25 W AVG., 28 V**  
**SINGLE W-CDMA**  
**RF LDMOS WIDEBAND**  
**INTEGRATED POWER AMPLIFIERS**

**CASE 1866-02**  
**TO-270 WBL-16**  
**PLASTIC**  
**MDE6IC7120NR1**



**CASE 1867-02**  
**TO-270 WBL-16 GULL**  
**PLASTIC**  
**MDE6IC7120GNR1**





**Figure 2. Pin Connections**

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.  
 2. Peaking and Carrier orientation is determined by the test fixture design.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +66	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (1,2)	$T_J$	225	°C
Input Power	$P_{in}$	30	dBm

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
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**Final Doherty Application**

Thermal Resistance, Junction to Case Case Temperature 81°C, $P_{out} = 28$ W CW Stage 1A, 27 Vdc, $I_{DQ1A} = 60$ mA Stage 1B, 27 Vdc, $I_{DQ1B} = 60$ mA Stage 2A, 27 Vdc, $I_{DQ2A} = 550$ mA Stage 2B, 27 Vdc, $V_{G2B} = 2.3$ Vdc	$R_{\theta JC}$	4.7 3.7 0.90 0.76	°C/W
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**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 1 — Off Characteristics</b> <sup>(1)</sup>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 66\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{A}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{A}$
Gate-Source Leakage Current ( $V_{GS} = 1.5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{A}$

**Stage 1 — On Characteristics** <sup>(1)</sup>

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 20\ \mu\text{A}$ )	$V_{GS(th)}$	1	1.7	3	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ1A} = I_{DQ1B} = 80\text{ mA}$ )	$V_{GS(Q)}$	—	2.8	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ1A} = I_{DQ1B} = 80\text{ mA}$ , Measured in Functional Test)	$V_{GG(Q)}$	8	11	14	Vdc

**Stage 2 — Off Characteristics** <sup>(1)</sup>

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 66\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{A}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{A}$
Gate-Source Leakage Current ( $V_{GS} = 1.5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{A}$

**Stage 2 — On Characteristics** <sup>(1)</sup>

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 160\ \mu\text{A}$ )	$V_{GS(th)}$	1	1.7	3	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ2A} = 550\text{ mA}$ )	$V_{GS(Q)}$	—	2.8	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ2A} = 550\text{ mA}$ , Measured in Functional Test)	$V_{GG(Q)}$	6.6	8.8	11.1	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 407\text{ mA}$ )	$V_{DS(on)}$	0.2	0.3	0.8	Vdc

**Functional Tests** <sup>(2,3,4)</sup> (In Freescale Doherty Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1A} = I_{DQ1B} = 80\text{ mA}$ ,  $I_{DQ2A} = 550\text{ mA}$ ,  $V_{G2B} = 2.3\text{ Vdc}$ ,  $P_{out} = 25\text{ W Avg.}$ ,  $f = 748\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Power Gain	$G_{ps}$	32.0	34.4	37.0	dB
Power Added Efficiency	PAE	38.0	40.6	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.2	6.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	-41.3	-38.0	dBc

**Typical Broadband Performance** <sup>(3)</sup> (In Freescale Doherty Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1A} = I_{DQ1B} = 80\text{ mA}$ ,  $I_{DQ2A} = 550\text{ mA}$ ,  $V_{G2B} = 2.3\text{ Vdc}$ ,  $P_{out} = 25\text{ W Avg.}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Frequency	$G_{ps}$ (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
728 MHz	35.0	42.0	6.2	-39.0
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768 MHz	33.8	39.1	6.9	-37.3

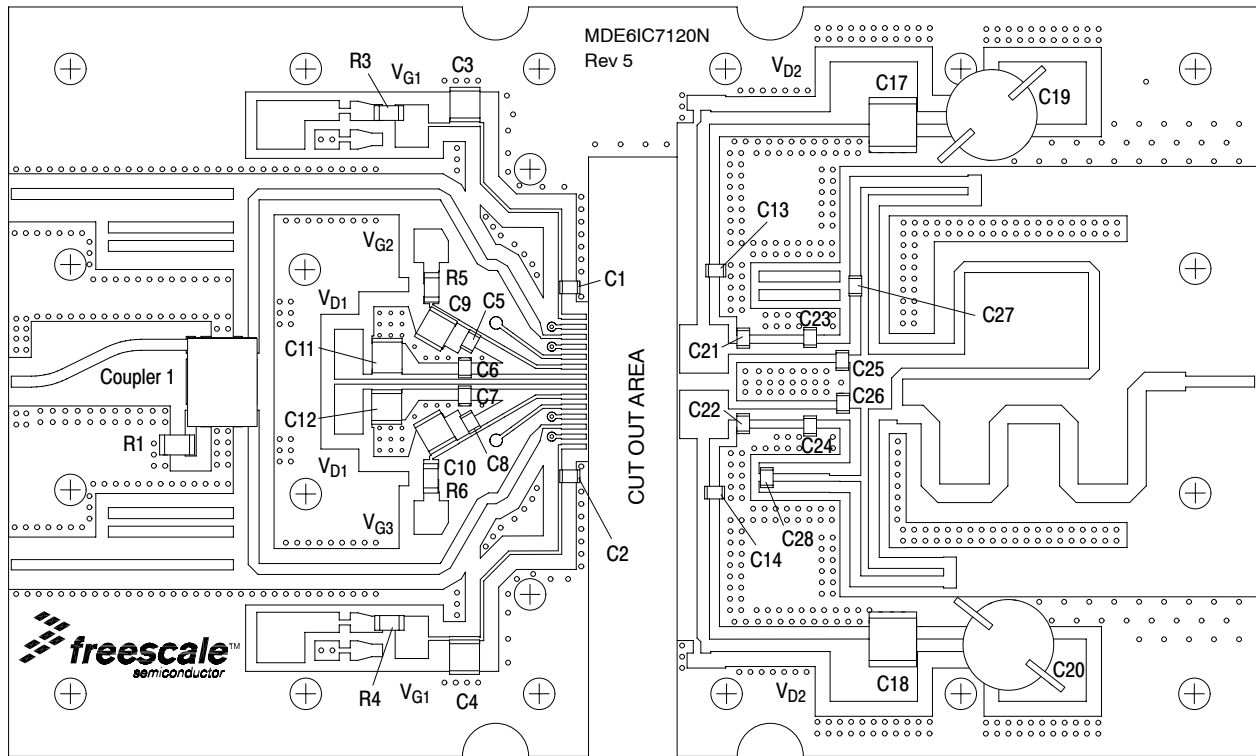
- Each side of device measured separately.
- Part internally matched both on input and output.
- Measurement made with device in a Symmetrical Doherty configuration.
- Measurement made with device in straight lead configuration before any lead forming operation is applied.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical Performances</b> <sup>(1)</sup> (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ1A} = I_{DQ1B} = 80\text{ mA}$ , $I_{DQ2A} = 550\text{ mA}$ , $V_{G2B} = 2.3\text{ Vdc}$ , 728-768 MHz Bandwidth					
$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	120	—	W
IMD Symmetry @ 90 W PEP, $P_{out}$ where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD <sub>sym</sub>	—	3	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	65	—	MHz
Quiescent Current Accuracy over Temperature <sup>(2)</sup> with 4.3 k $\Omega$ Gate Feed Resistors (-30 to 85°C)	$\Delta I_{QT}$	—	0.012 0.031	—	%
Gain Flatness in 40 MHz Bandwidth @ $P_{out} = 25\text{ W Avg.}$	G <sub>F</sub>	—	1.2	—	dB
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.034	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1\text{dB}$	—	0.005	—	dBm/°C

1. Measurement made with device in a Symmetrical Doherty configuration.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

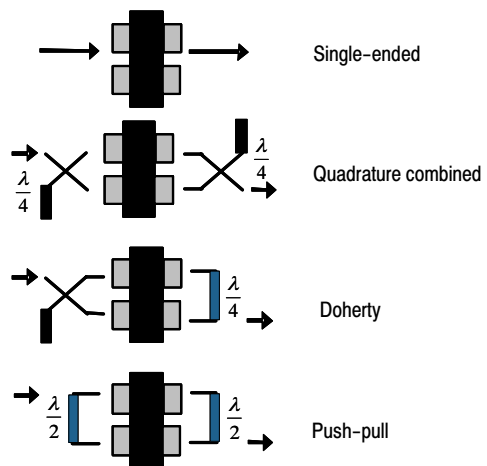


Note: Component numbers C15, C16 and R2 are not used.

**Figure 3. MDE6IC7120NR1(GNR1) Test Circuit Component Layout**

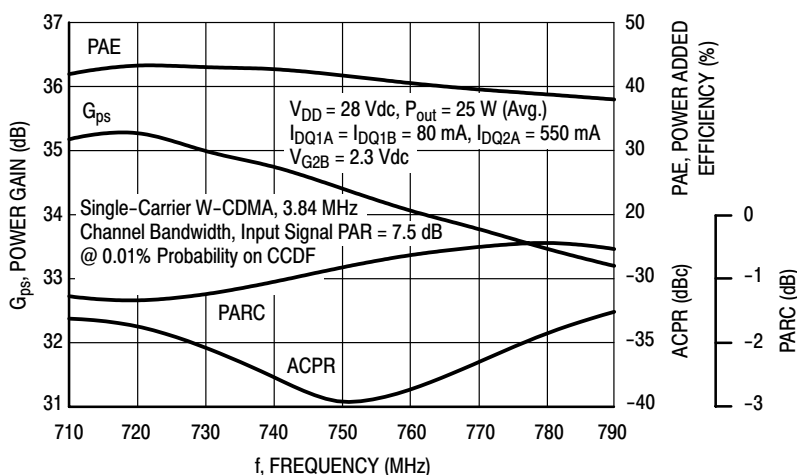
**Table 6. MDE6IC7120NR1(GNR1) Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1, C2, C5, C6, C7, C8	0.01 $\mu$ F, 50 V Chip Capacitors	GCM2195C1H103JA16D	Murata
C3, C4, C9, C10, C11, C12	1.0 $\mu$ F, 35 V Chip Capacitors	GRM32RR71H105KA01K	Murata
C13, C14, C27, C28	68 pF Chip Capacitors	ATC600F680JT250XT	ATC
C17, C18	10 $\mu$ F, 35 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C19, C20	220 $\mu$ F, 50 V Electrolytic Capacitors	EMVY500ADA221MJA0G	Nippon Chemi-Con
C21, C22	18 pF Chip Capacitors	ATC600F180GT250XT	ATC
C23, C24	1.0 pF Chip Capacitors	ATC600F1R0JT250XT	ATC
C25, C26	8.2 pF Chip Capacitors	ATC600F8R2JT250XT	ATC
Coupler 1	50 $\Omega$ , 3 dB Hybrid Coupler	GSC268-HYB0750	Soshin
R1	50 $\Omega$ , 10 W Termination	RFP-060120A15Z50-2	Anaren
R3, R4, R5, R6	4.3 K $\Omega$ , 1/4 W Chip Resistors	CRCW12064K30FKEA	Vishay
PCB	0.020", $\epsilon_r = 3.50$	RO4350B	Rogers

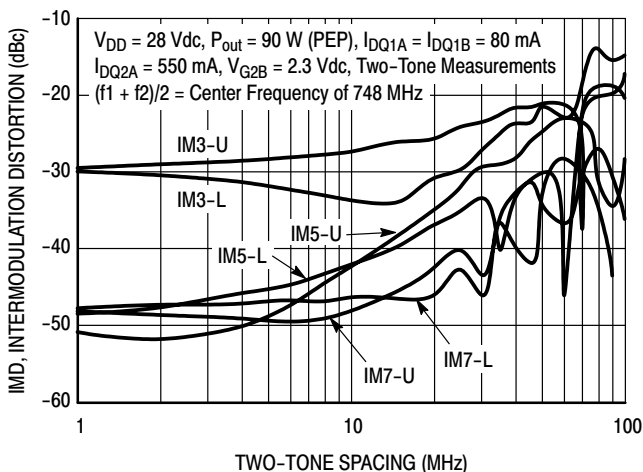


**Figure 4. Possible Circuit Topologies**

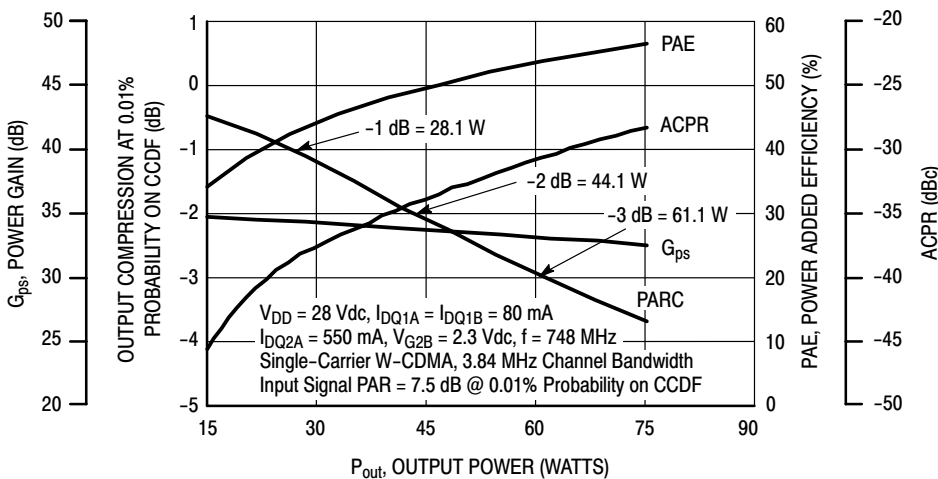
### TYPICAL CHARACTERISTICS



**Figure 5. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 25$  Watts Avg.**

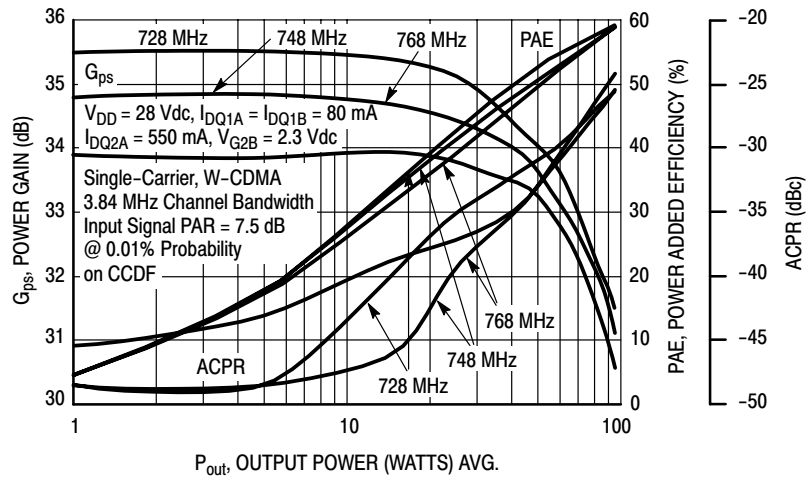


**Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing**

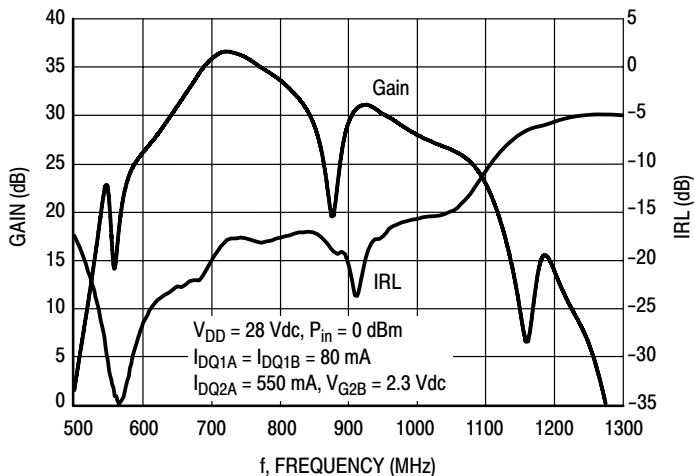


**Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

### TYPICAL CHARACTERISTICS

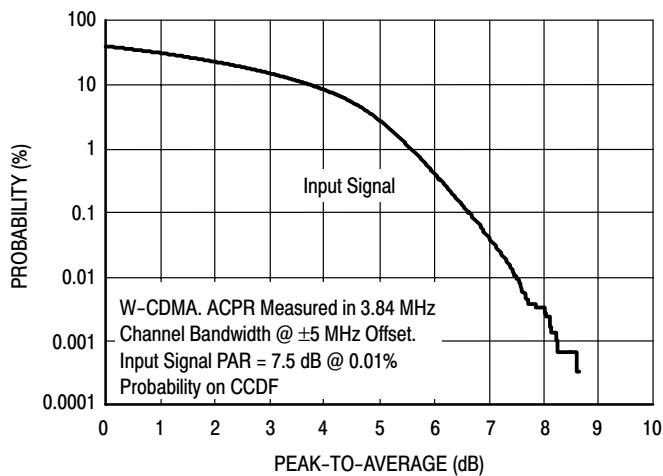


**Figure 8. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power**

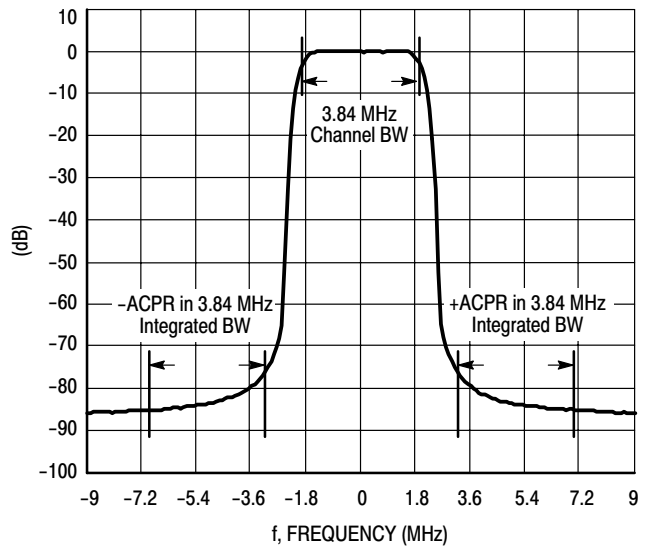


**Figure 9. Broadband Frequency Response**

### W-CDMA TEST SIGNAL



**Figure 10. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal**



**Figure 11. Single-Carrier W-CDMA Spectrum**



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1A} = I_{DQB} = 80 \text{ mA}$ ,  $I_{DQ2A} = 550 \text{ mA}$ ,  $V_{G2B} = 2.3 \text{ Vdc}$ ,  $P_{out} = 25 \text{ W Avg.}$

f MHz	$Z_{in}$ $\Omega$	$Z_{load}$ $\Omega$
710	63.51 - j17.96	2.26 + j2.92
720	63.51 - j16.36	2.43 + j3.05
730	63.27 - j14.61	2.61 + j3.17
740	62.90 - j12.86	2.81 + j3.20
750	62.60 - j11.26	3.04 + j3.21
760	62.50 - j9.83	3.33 + j3.13
770	62.73 - j8.61	3.56 + j2.96
780	63.29 - j7.55	3.73 + j2.75
790	64.11 - j6.70	3.86 + j2.53

Note: Measured with Peaking side open.

$Z_{in}$  = Device input impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

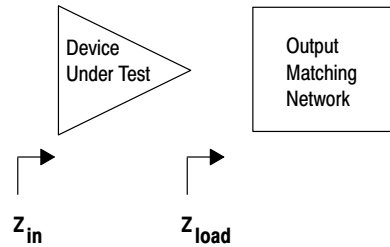


Figure 12. Series Equivalent Input and Load Impedance — Carrier Side

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1A} = I_{DQB} = 80 \text{ mA}$ ,  $I_{DQ2A} = 550 \text{ mA}$ ,  $V_{G2B} = 2.3 \text{ Vdc}$ ,  $P_{out} = 25 \text{ W Avg.}$

f MHz	$Z_{in}$ $\Omega$	$Z_{load}$ $\Omega$
710	63.51 - j17.96	1.58 - j0.62
720	63.51 - j16.36	1.35 - j0.33
730	63.27 - j14.61	1.16 - j0.05
740	62.90 - j12.86	0.95 + j0.19
750	62.60 - j11.26	0.79 + j0.44
760	62.50 - j9.83	0.68 + j0.66
770	62.73 - j8.61	0.56 + j0.87
780	63.29 - j7.55	0.38 + j1.15
790	64.11 - j6.70	0.30 + j1.46

Note: Measured with Carrier side open.

$Z_{in}$  = Device input impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

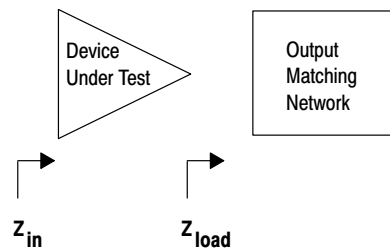
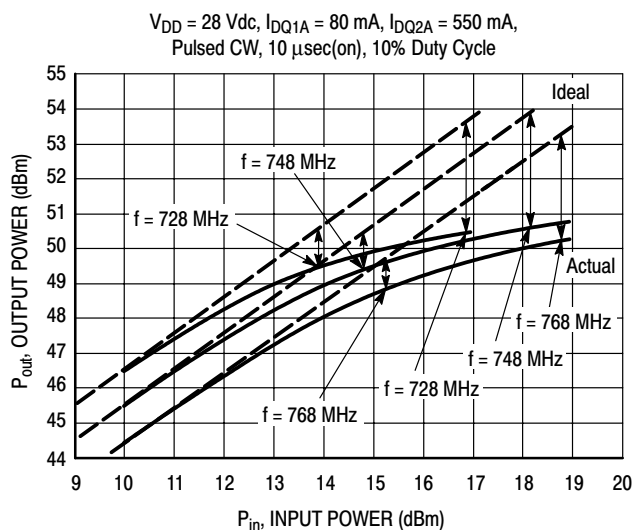


Figure 13. Series Equivalent Input and Load Impedance — Peaking Side

## ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
728	89	49.5	110	50.4
748	87	49.4	115	50.6
768	78	48.9	105	50.2

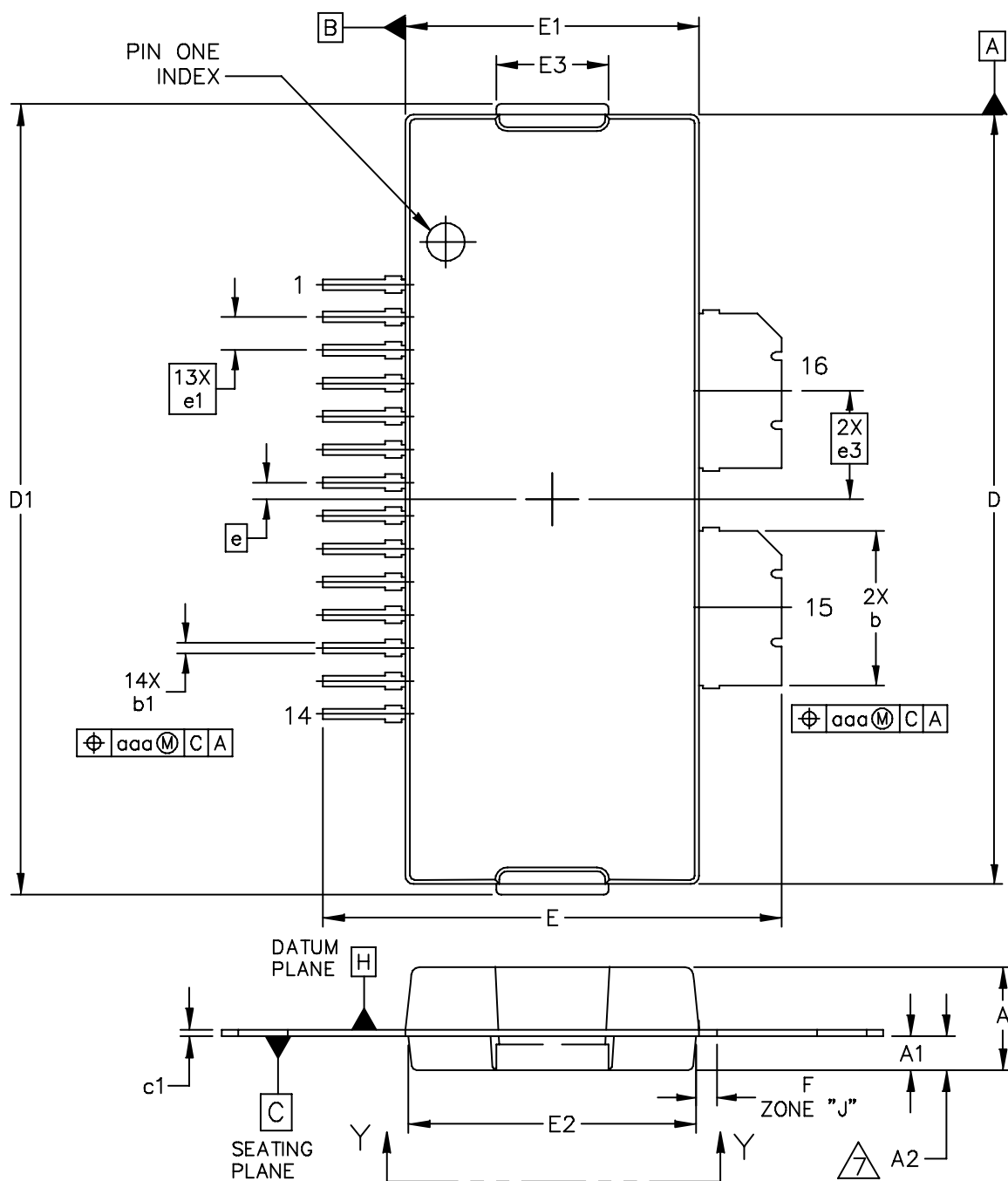
Test Impedances per Compression Level

f (MHz)		$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
728	P1dB	50.23 - j0.14	1.88 + j0.60
748	P1dB	50.23 + j1.83	1.92 + j0.10
768	P1dB	48.78 - j1.26	1.25 + j0.19

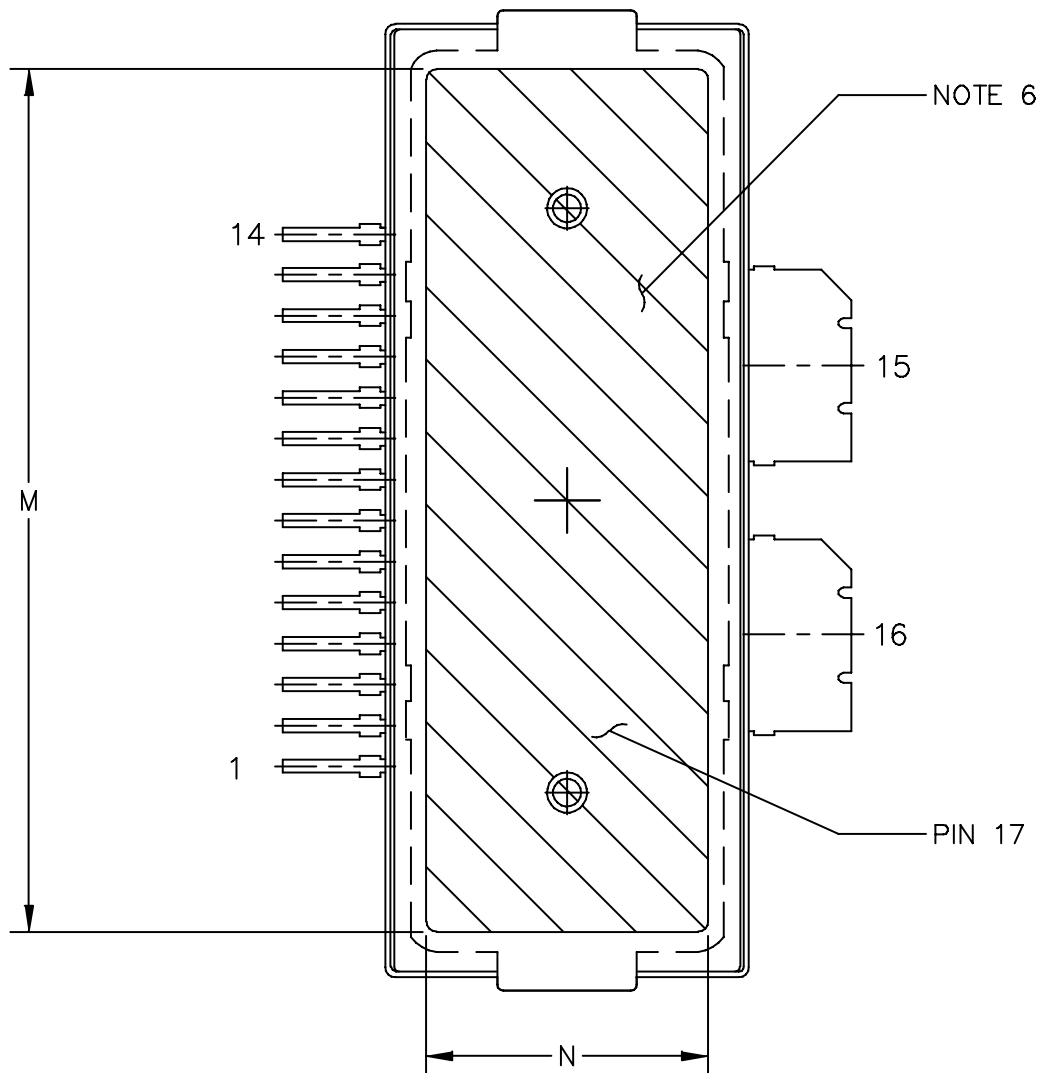
**Figure 14. Pulsed CW Output Power versus Input Power @ 28 V**

NOTE: Measurement made on the Class AB, carrier side of the device.

### PACKAGE DIMENSIONS



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TITLE: TO-270 WIDE BODY LONG, 16 LEAD, PLASTIC	DOCUMENT NO: 98ASA10739D	REV: A	
	CASE NUMBER: 1866-02	02 AUG 2007	
	STANDARD: NON-JEDEC		



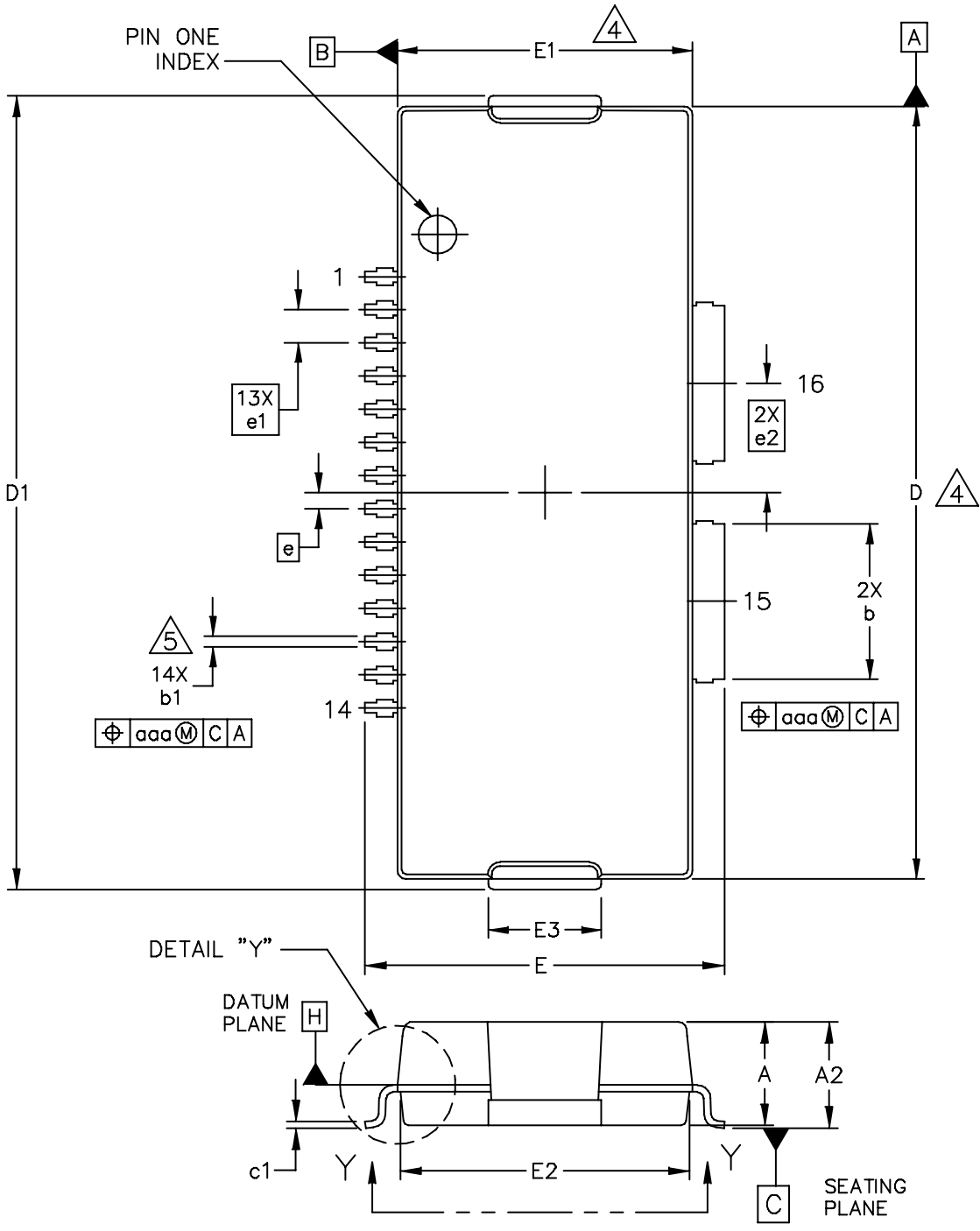
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TITLE: TO-270 WIDE BODY LONG, 16 LEAD, PLASTIC	DOCUMENT NO: 98ASA10739D	REV: A	
	CASE NUMBER: 1866-02	02 AUG 2007	
	STANDARD: NON-JEDEC		

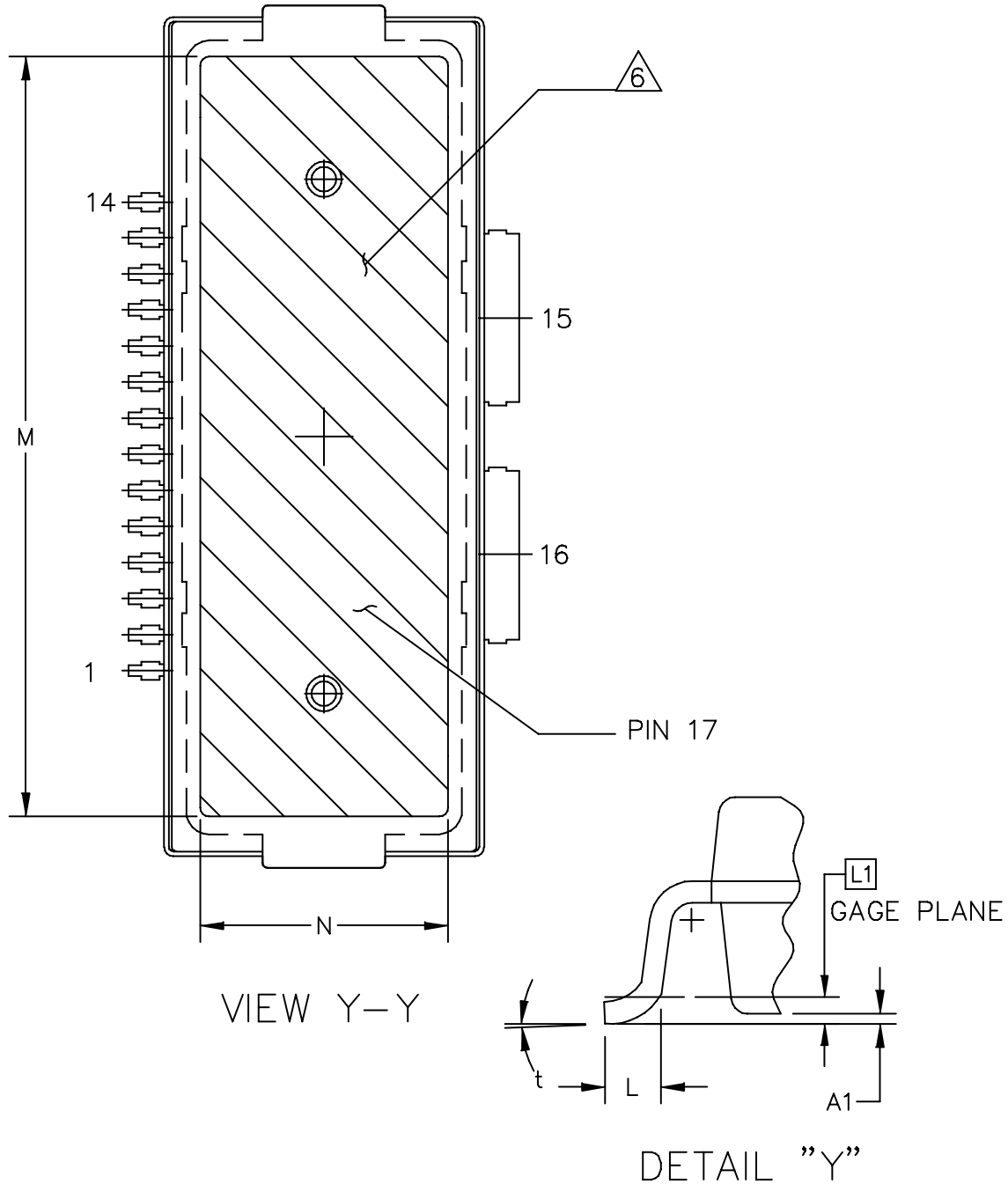
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.122	.128	3.10	3.25	M	.800	----	20.32	----
A1	.039	.043	0.96	1.12	N	.270	----	6.86	----
A2	.040	.042	1.02	1.07	b	.184	.190	4.67	4.83
D	.928	.932	23.57	23.67	b1	.010	.016	0.25	0.41
D1	.954	.958	24.23	24.33	c1	.007	.011	0.18	0.28
E	.551	.559	14.00	14.20	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e3	.131 BSC		3.33 BSC	
E3	.132	.140	3.35	3.56					
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
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					CASE NUMBER: 1866-02			02 AUG 2007	
					STANDARD: NON-JEDEC				



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	CASE NUMBER: 1867-02	02 AUG 2007	
	STANDARD: NON-JEDEC		



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	CASE NUMBER: 1867-02	02 AUG 2007	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.122	.128	3.10	3.25	b	.184	.190	4.67	4.83
A1	.001	.004	0.02	0.10	b1	.010	.016	0.25	0.41
A2	.125	.131	3.18	3.33	c1	.007	.011	0.18	0.28
D	.928	.932	23.57	23.67	e	.020 BSC		0.51 BSC	
D1	.954	.958	24.23	24.33	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.131 BSC		3.33 BSC	
E1	.353	.357	8.97	9.07	t	2°	8°	2°	8°
E2	.346	.350	8.79	8.89	aaa	.004		0.10	
E3	.132	.140	3.35	3.56					
L	.018	.024	0.46	0.61					
L1	.01 BSC		0.25 BSC						
M	.800	----	20.32	----					
N	.270	----	6.86	----					
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TITLE: TO-270 WIDE BODY LONG, 16 LEAD, GULL WING PLASTIC					DOCUMENT NO: 98ASA10740D			REV: A	
					CASE NUMBER: 1867-02			02 AUG 2007	
					STANDARD: NON-JEDEC				



## PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2009	<ul style="list-style-type: none"> <li>• Initial Release of Data Sheet</li> </ul>

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