

SN74S225

16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY WITH 3-STATE OUTPUTS

SDLS207B – SEPTEMBER 1976 – REVISED APRIL 1998

- Independent Asynchronous Inputs and Outputs
- 16 Words by 5 Bits
- DC to 10-MHz Data Rate
- 3-State Outputs
- Packaged in Standard Plastic 300-mil DIPs

description

This 80-bit active-element memory is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words by 5 bits. A memory system using the SN74S225 easily can be expanded in multiples of 48 words or of 10 bits as shown in Figure 3. The 3-state outputs controlled by a single output-enable (\overline{OE}) input make bus connection and multiplexing easy.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from dc to 10 MHz in a bit-parallel format, word by word.

Reading or writing is done independently, utilizing separate asynchronous data clocks. Data can be written into the array on the low-to-high transition of either load-clock (CLKA, CLKB) input. Data can be read out of the array on the low-to-high transition of the unload-clock (UNCK IN) input (normally high). Writing data into the FIFO can be accomplished in one of two ways:

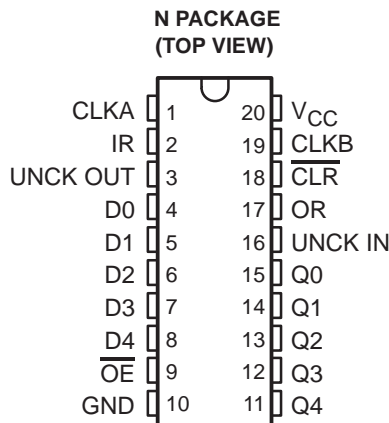
- In applications not requiring a gated clock control, best results are achieved by applying the clock input to one of the clocks while tying the other clock input high.
- In applications needing a gated clock, the load clock (gate control) must be high for the FIFO to load on the next clock pulse.

CLKA and CLKB can be used interchangeably for either clock gate control or clock input.

Status of the SN74S225 is provided by three outputs. The input-ready (IR) output monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload-clock (UNCK OUT) output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready (OR), is high when the first word location contains valid data and UNCK IN is high. When UNCK IN goes low, OR will go low and stay low until new valid data is in the first word position. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are 3-state, with a common control input (\overline{OE}). When \overline{OE} is low, the data outputs are enabled to function as totem-pole outputs. A high logic level forces each data output to a high-impedance state while all other inputs and outputs remain active. The clear (\overline{CLR}) input invalidates all data stored in the memory array by clearing the control logic and setting OR to a low logic level on the high-to-low transition of a low-active pulse.

The SN74S225 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

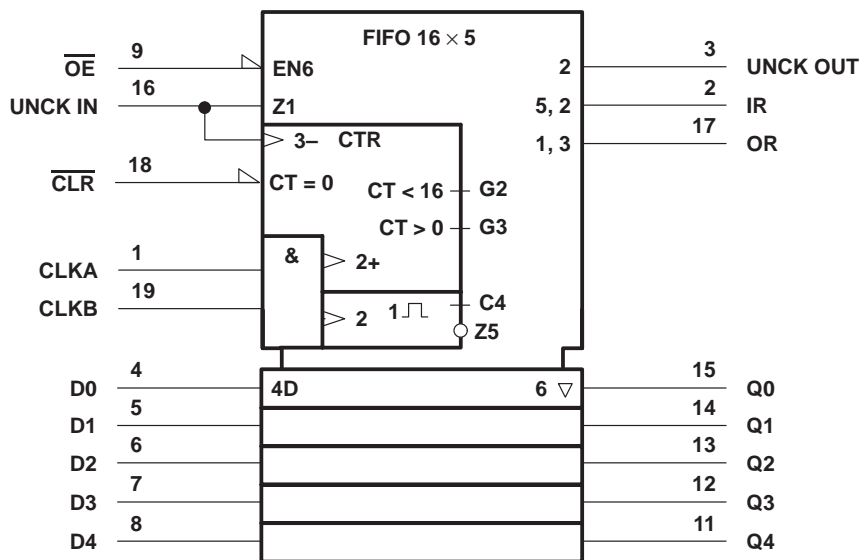
Copyright © 1998, Texas Instruments Incorporated

SN74S225

16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY WITH 3-STATE OUTPUTS

SDLS207B – SEPTEMBER 1976 – REVISED APRIL 1998

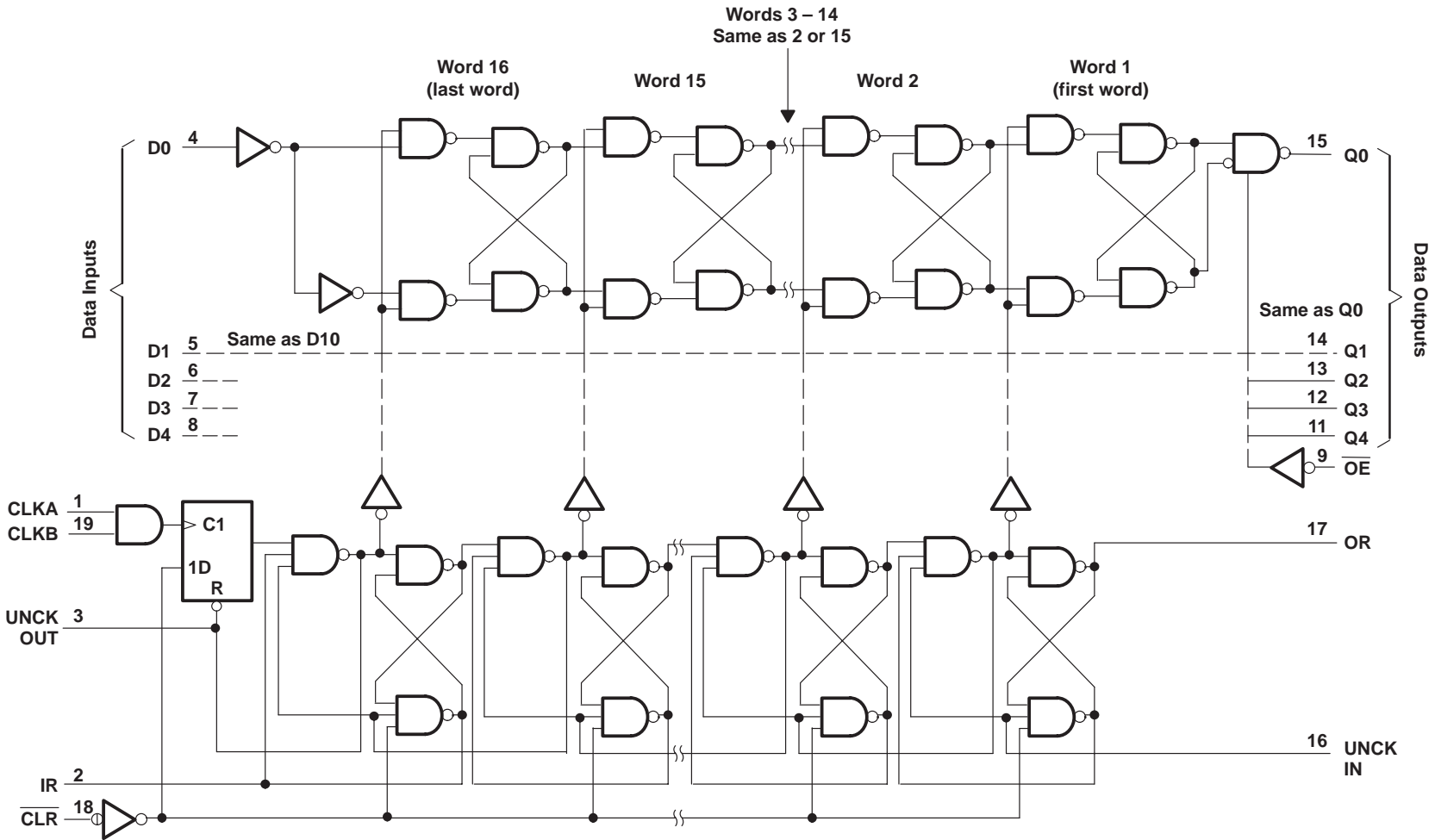
logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

SN74S225
16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY
WITH 3-STATE OUTPUTS
 SDL5207B – SEPTEMBER 1976 – REVISED APRIL 1998

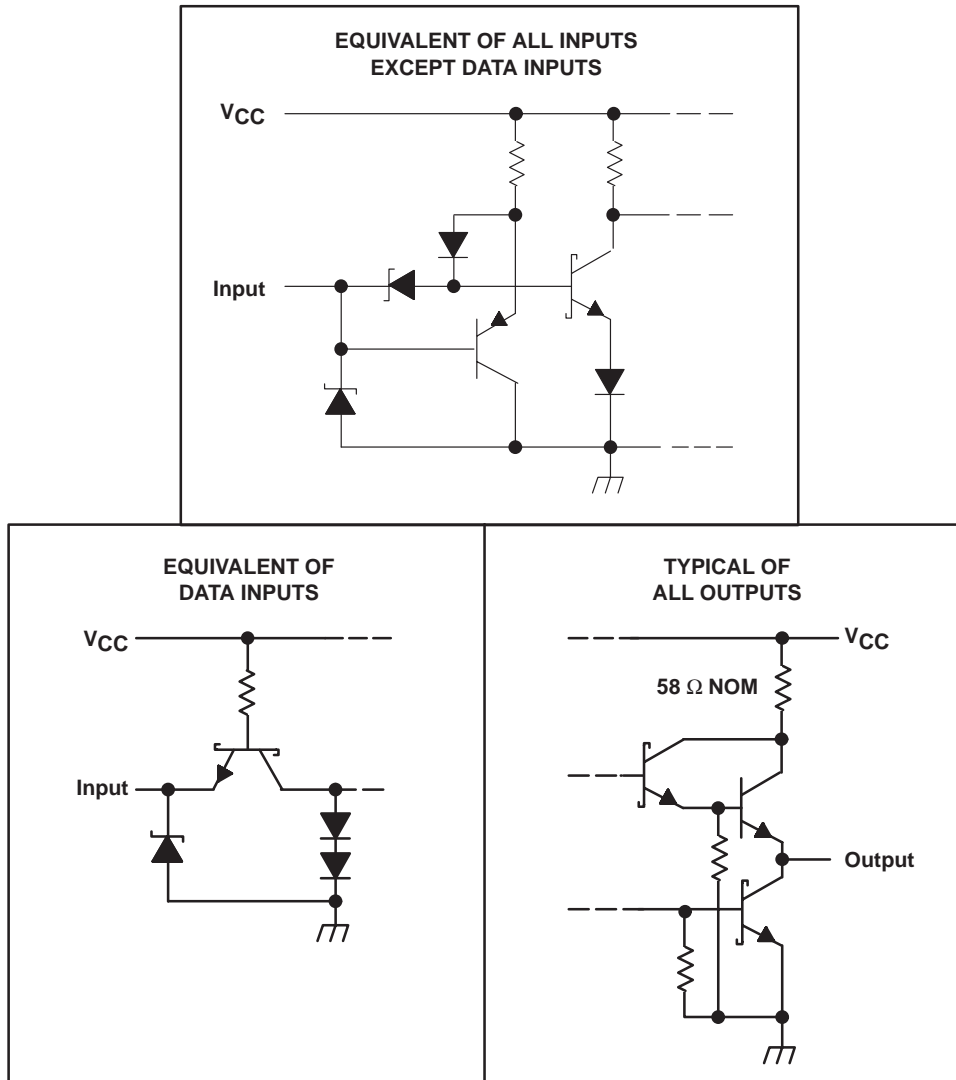
functional block diagram



SN74S225
16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY
WITH 3-STATE OUTPUTS

SDLS207B – SEPTEMBER 1976 – REVISED APRIL 1998

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	-0.5 V to 7 V
Input voltage range, V_I	-0.5 V to 5.5 V
Off-state output voltage range	-0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 2)	67°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



SN74S225

16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY WITH 3-STATE OUTPUTS

SDLS207B – SEPTEMBER 1976 – REVISED APRIL 1998

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{OH}	High-level output current	Q outputs		-6.5	mA
		All other outputs		-3.2	
I _{OL}	Low-level output current	Q outputs		16	mA
		All other outputs		8	
T _A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.75 V,	I _I = -18 mA			-1.2	V
V _{OH}	Q outputs	V _{CC} = 4.75 V,	I _{OL} = -6.5 mA	2.4	2.9		V
	All others	V _{CC} = 4.75 V,	I _{OL} = -3.2 mA	2.4	2.9		
V _{OL}	Q outputs	V _{CC} = 4.75 V,	I _{OL} = 16 mA	0.35	0.5		V
	All others	V _{CC} = 4.75 V,	I _{OL} = 8 mA	0.35	0.5		
I _{OZH}		V _{CC} = 5.25 V,	V _O = 2.4 V			50	μA
I _{OZL}		V _{CC} = 5.25 V,	V _O = 0.5 V			-50	μA
I _I		V _{CC} = 5.25 V,	V _I = 5.5 V			1	mA
I _{IH}	Data	V _{CC} = 5.25 V,	V _I = 2.7 V			40	μA
	All others					25	
I _{IL}	Data	V _{CC} = 5.25 V,	V _I = 0.5 V			-1	mA
	All others					-0.25	
I _{OS} ‡		V _{CC} = 5.25 V,	V _O = 0	-30		-100	mA
I _{CC} §		V _{CC} = 5.25 V			80	120	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Duration of the short circuit should not exceed one second.

§ I_{CC} is measured with all inputs grounded and the outputs open.

timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 1)

		MIN	NOM	MAX	UNIT
f _{clock}	Clock frequency			10	MHz
t _w	Pulse duration	CLKA or CLKB high	25		ns
		UNCK IN low	7		
		CLR low	40		
t _{su}	Setup time before CLKA↑ or CLKB↑	Data (see Note 3)	-20		ns
		CLR inactive	25		
t _h	Hold time after CLKA↑ or CLKB↑	70			ns

NOTE 3: Data must be set up within 20 ns after the load-clock positive transition.

SN74S225

16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY WITH 3-STATE OUTPUTS

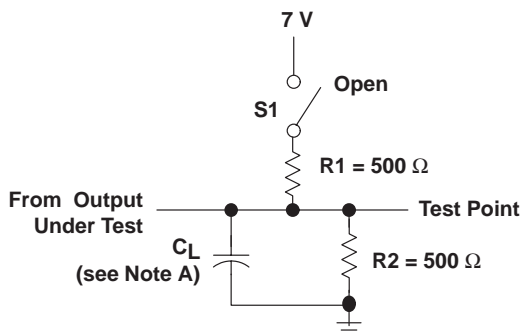
SDLS207B – SEPTEMBER 1976 – REVISED APRIL 1998

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f _{max}	CLKA		C _L = 30 pF	10	20		MHz
	CLKB			10	20		
	UNCK IN			10	20		
t _w	UNCK OUT		C _L = 30 pF	7	14		ns
t _{dis}	OE	Any Q	C _L = 5 pF		10	25	ns
t _{en}	OE	Any Q	C _L = 30 pF		25	40	ns
t _{PLH}	UNCK IN	Any Q	C _L = 30 pF		50	75	ns
t _{PHL}					50	75	
t _{PLH}	CLKA or CLKB	OR	C _L = 30 pF		190	300	ns
t _{PLH}	UNCK IN	OR	C _L = 30 pF		40	60	ns
t _{PHL}					30	45	
t _{PHL}	CLR	OR	C _L = 30 pF		35	60	ns
	CLKA or CLKB	UNCK OUT			25	45	
	UNCK IN				270	400	
	CLKA or CLKB	IR			55	75	
t _{PLH}	UNCK IN	IR	C _L = 30 pF		255	400	ns
	CLR				16	35	
	OR↑			Any Q		10	

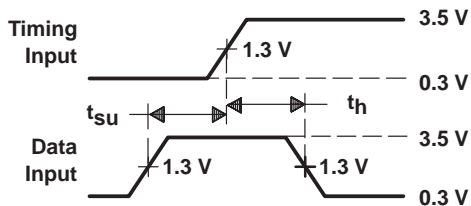
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

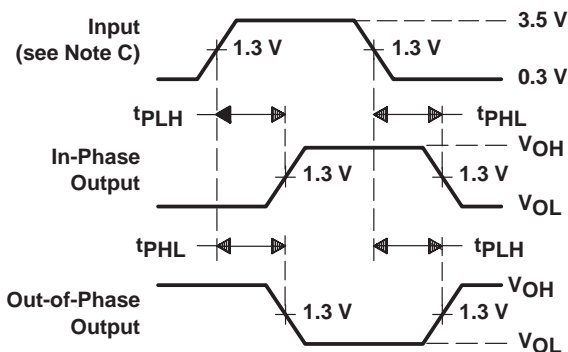


LOAD CIRCUIT FOR 3-STATE OUTPUTS

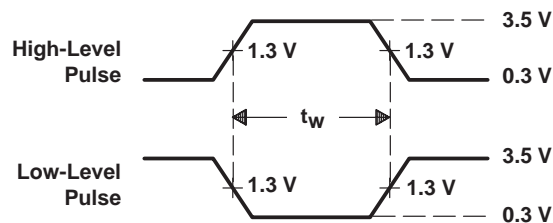
PARAMETER	S1	
t_{en}	tpZH	Open
	tpZL	Closed
t_{dis}	tPHZ	Open
	tPLZ	Closed
t_{pd}	tPLH	Open
	tPHL	Open



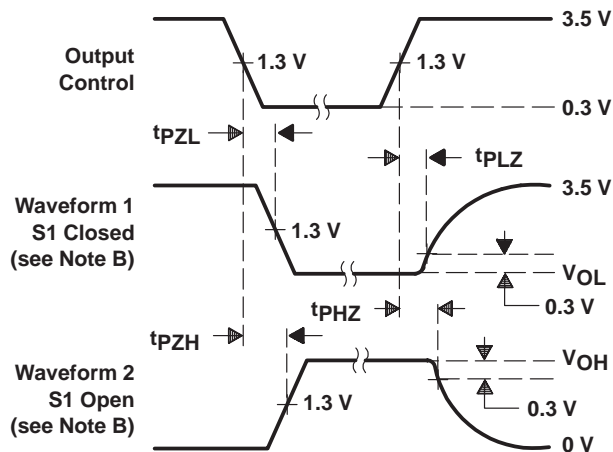
**VOLTAGE WAVEFORMS
SET UP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN74S225
16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY
WITH 3-STATE OUTPUTS

SDLS207B – SEPTEMBER 1976 – REVISED APRIL 1998

APPLICATION INFORMATION

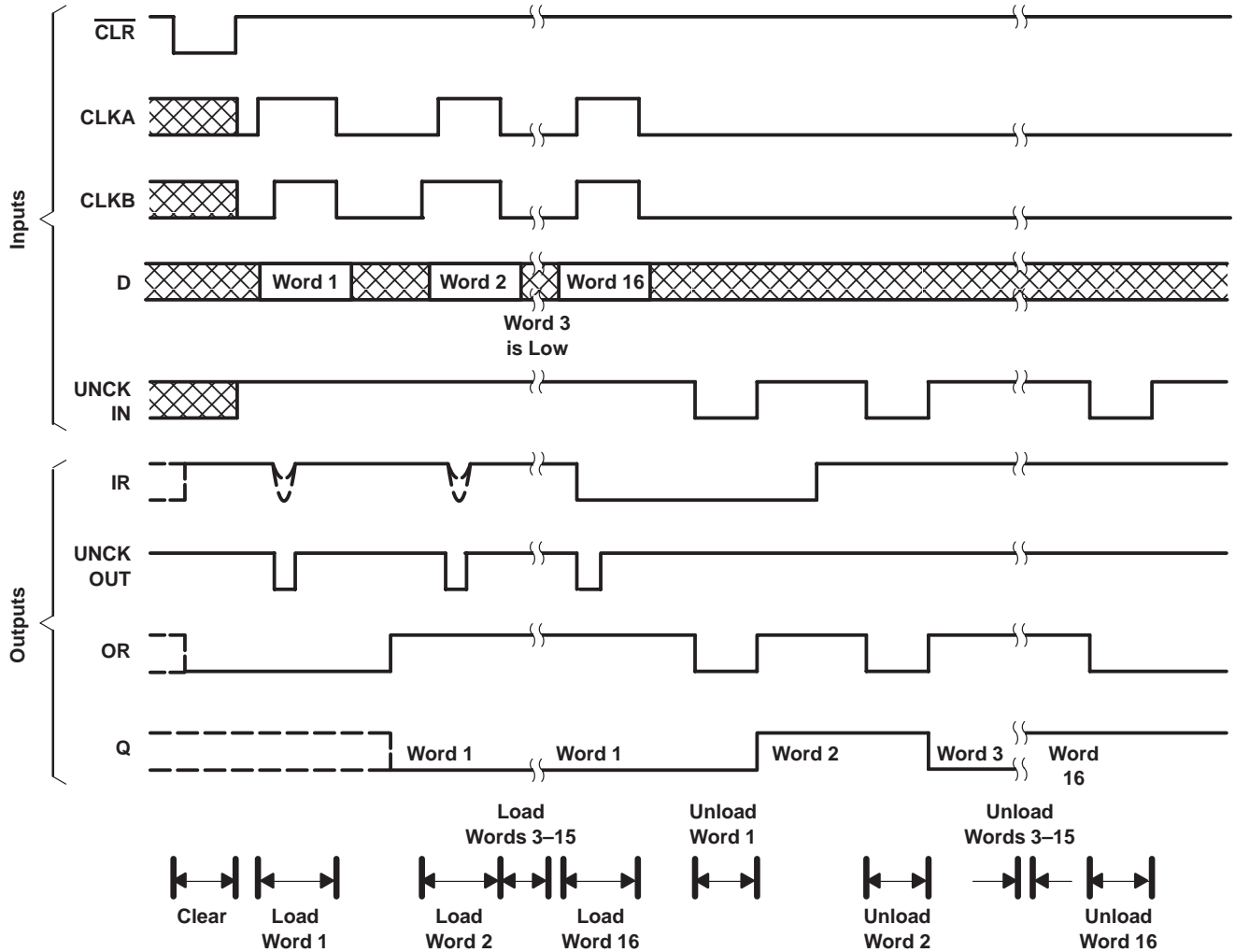


Figure 2. Typical Waveforms for a 16-Word FIFO

SN74S225
**16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY
 WITH 3-STATE OUTPUTS**

SDLS207B – SEPTEMBER 1976 – REVISED APRIL 1998

APPLICATION INFORMATION

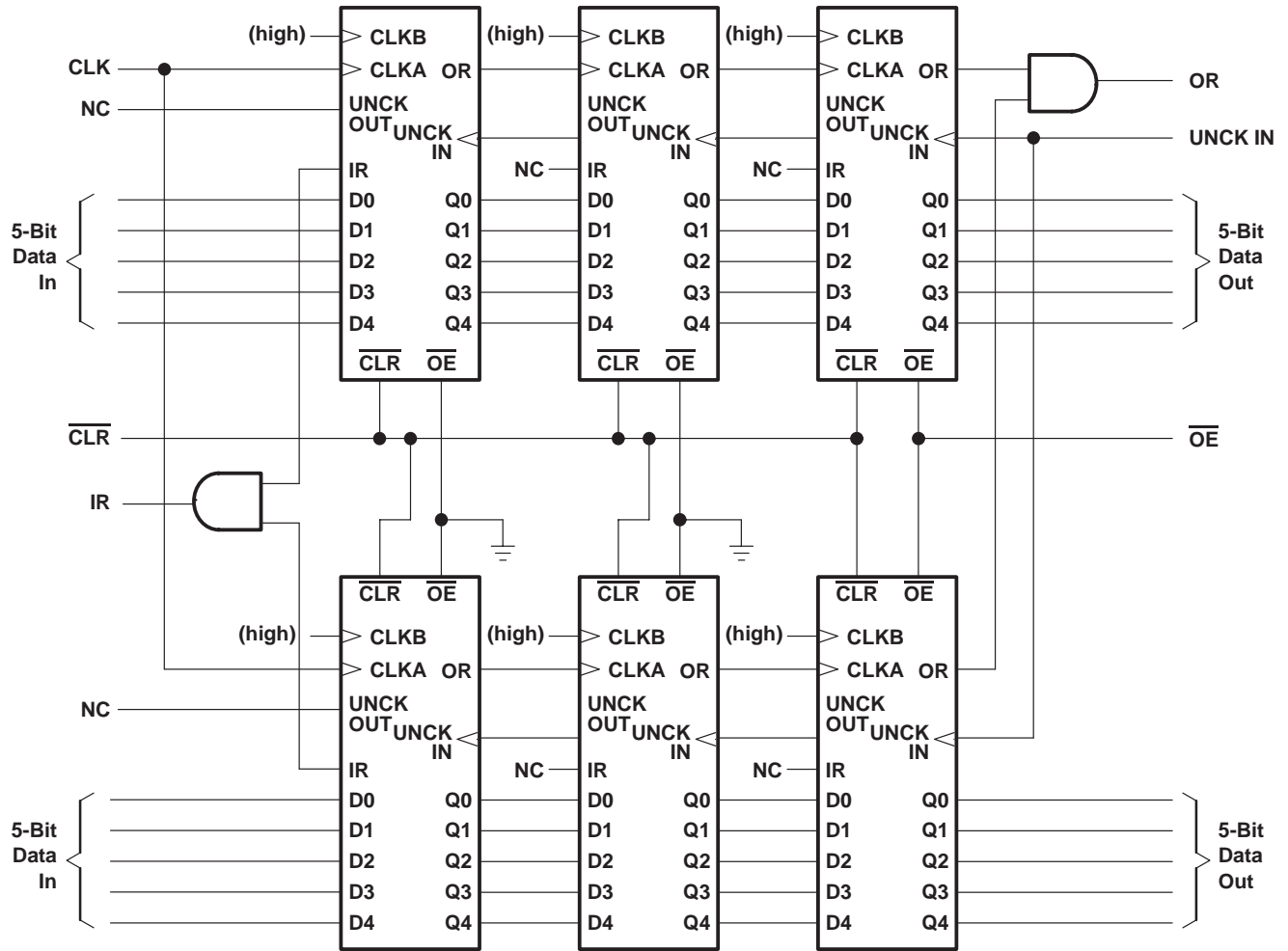


Figure 3. Word-Width Expansion: 48 × 10 Bits

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74S225N	NRND	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S225N	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74S225N	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - △ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - △ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated