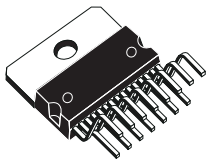
L5959

Multifunction voltage regulator for car radio

Features

- Four outputs
  - 8.5V @ 200mA (V8P5)
  - 8/10V @ 1000mA selectable 10V or 8V (V810)
  - 3.3V @ 100mA permanent (VSTBY)
  - 3.3V @ 800mA (VREGSW)
- Two protected high side driver (HSD1, HSD2)
- Reset function
- Battery voltage (under/over) warning output
- Load dump protection
- Independent thermal shutdown on all regulators and HSDs
- Overcurrent limitation
- Storage CAP output (STCAP)
- Small CAP required by stability of regulators
- All pins ESD protected



Multiwatt15

Description

The L5959 contains a four voltage regulator and two protected HSDs. HSDs are protected against loss of ground and loss of battery.

The IC includes a monitoring circuit for detection.

The IC features a very low quiescent current in stand-by and independent thermal shutdown.

Table 1. Device summary

Order code	Package	Packing
L5959	Multiwatt15	Tube

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1 Block diagram

Figure 1. Block diagram

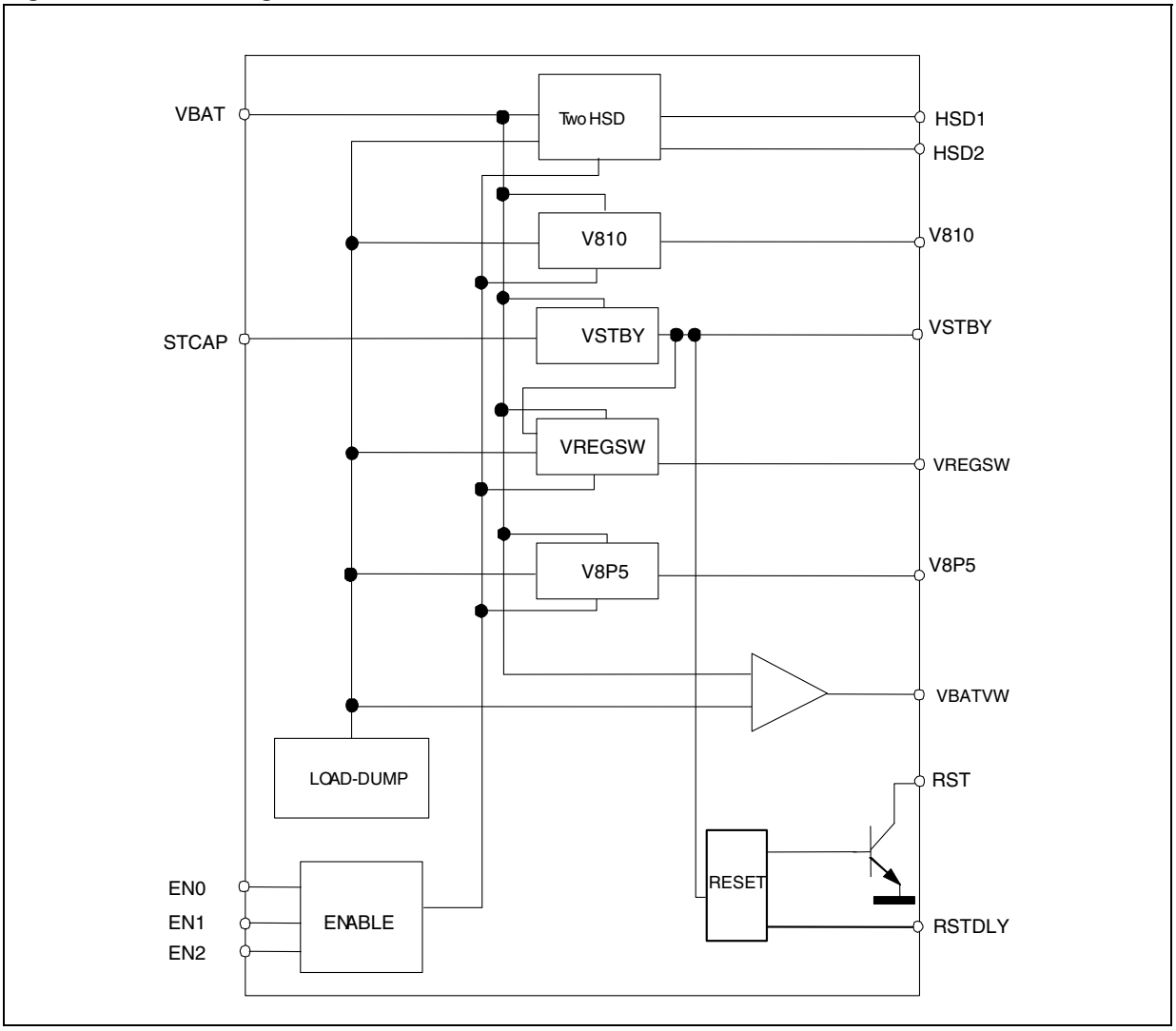


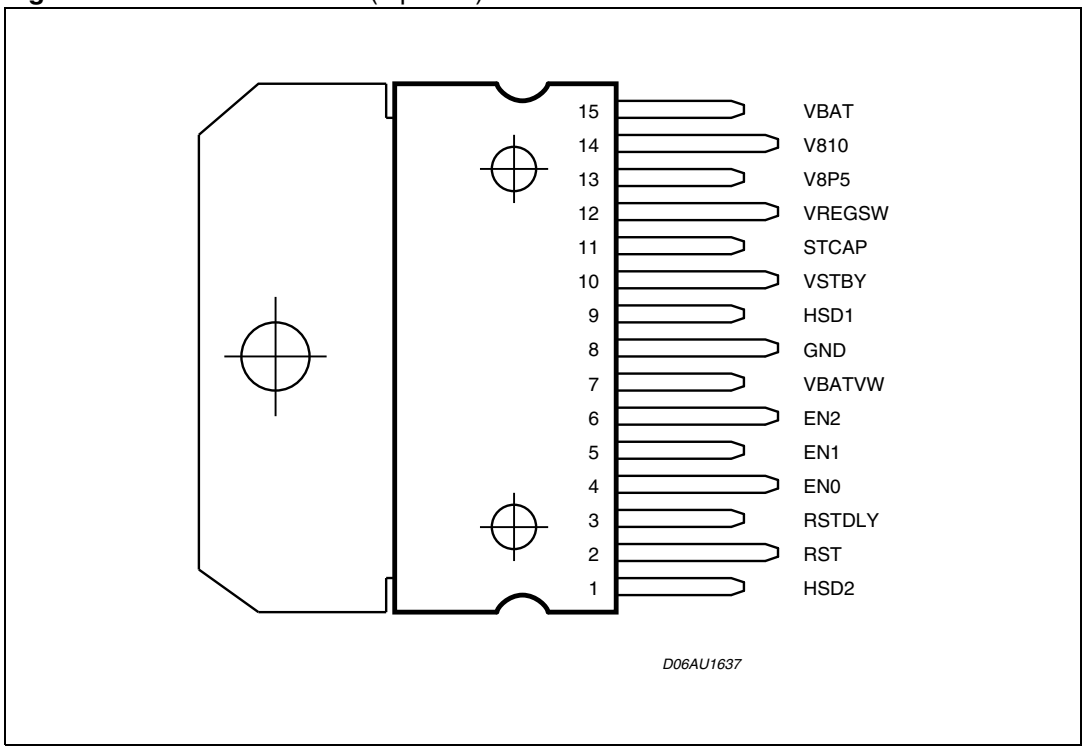
Table 2. Enable logic

EN2	EN1	EN0	VREGSW	V8P5	HSD1	V810 (8V)	V810 (10V)	HSD2
0	0	0	Off	Off	Off	Off	Off	Off
0	0	1	On	On	On	Off	On	On
0	1	0	On	Off	Off	Off	Off	Off
0	1	1	On	On	On	Off	Off	On
1	0	0	On	On	On	Off	Off	Off
1	0	1	On	On	On	Off	On	Off
1	1	0	On	On	On	On	Off	Off
1	1	1	On	On	On	On	Off	On

2 Pins description

2.1 Pins connection

Figure 2. Pins connection (top view)



3 Electrical specification

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{BATDC}	DC operating supply voltage	30	V
V_{BATTR}	Transient supply voltage	50	V
I_O	Output current	internally limited	
R_{ESR}	Output capacitor series eq. resistance (MAX.)	0.5	Ω
T_{op}	Operating temperature range	-40 to 105	°C
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Junction temperature	-55 to 150	°C
P_d	Power dissipation T_{case} = 85°C	43	W

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Multiwatt	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction to case max.	1.8	°C/W

3.3 Electrical characteristics

Table 5. Electrical characteristics

(V_S = 14.4V; T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT SUPPLIES						
V_{bat}	Input supply	Operating	9		18	V
V_{STCAP}	Input supply voltage 2	Operating	6		18	V
V_{bat}	Battery voltage	Reverse polarity		non operating		
V_{STCAP}	Input supply voltage 2	Reverse polarity		non operating		
I_q	Total quiescent current	EN0 = EN1 = EN2 = 0 V; VBAT = 14 V; I_{VSTBY} = 100 µA		55	75	µA
V_{OV}	VBAT Over-voltage shutdown	Verify all outputs except VSTBY disabled and VBATVW* asserted low (VBAT Rising)	24	27	30	V
V_{HYSOV}	Hysteresis of over-voltage shutdown		200	750	1500	mV

Table 5. Electrical characteristics (continued)

(V_S = 14.4V; T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{UV}	VBAT Under-voltage warning	Verify VBATVW* asserted low (VBAT Falling)	7	7.4	7.8	V
V_{HYSUV}	Hysteresis of under-voltage warning		70	300	500	mV
VSTBY						
V_o(VSTBY)	Output voltage of VSTBY		3.14	3.3	3.46	V
ΔV	Line regulation	V_{BAT} = 6 to 18V; I = 100mA	-10	0	+10	mV
ΔV_i	Load regulation	I_{VSTBY} = 0.5 to 100 mA	-40	-5	+10	mV
V_{over}	Over shoot	I_{VSTBY} = 100 to 0.5 mA, Co=1µF		2.5	6	%
PSRR	Supply voltage ripple rejection	I_{VSTBY} = 50 mA; f_o = 20 to 1 kHz; VBAT = 14 V_{dc}, 1.0 $V_{ac(pp)}$	50	70		dB
		I_{VSTBY} = 50 mA; f_o = 20 to 20 kHz; VBAT = 14 V_{dc}, 1.0 $V_{ac(pp)}$	45	55		dB
V_N	Output noise	Weighted filter f_o = 20 Hz to 20 kHz I_{VSTBY} = 5 mA		85	200	µV
V_{drop}	Drop out voltage	I_{VSTBY} = 100mA(1)			2.6	V
	Drop out voltage	I_{VSTBY} = 5 mA			2.3	V
I_m	Current limit	Rshort = 0Ω	150	200	300	mA
TS_{EN}	VSTBY thermal shutdown	I_{VSTBY} = 500 µA; Increase Ta until VSTBY disabled	150		190	°C
VREGSW						
V_o (VREGSW)	Output voltage 3.3V		3.14	3.3	3.46	V
V_{TRK}	VREGSW output tracking voltage on VSTBY	I_{VSTBY} = 50 mA I_{VREGSW} = 0.5 to 800 mA Measure VSTBY – VREGSW	-40		40	mV
		I_{VSTBY} = 0.5 mA to 100 mA I_{VREGSW} = 0.5 to 800 mA Measure VSTBY – VREGSW	-50		50	mV
ΔV	Line regulation	Vin1 = 9 to 18V; I = 800mA	-40	10	40	mV
ΔV_i	Load regulation	I_{VREGSW} = 1 to 800mA	-50	-15	10	mV

Table 5. Electrical characteristics (continued)

(V_S = 14.4V; T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PSRR	Supply voltage ripple rejection	I_{VREGSW} = 400 mA; f_o = 20 to 1 kHz; VBAT = 14 V_{dc}, 1.0 $V_{ac(pp)}$	50	70		dB
		I_{VREGSW} = 400 mA; f_o = 20 to 20 kHz; VBAT = 14 V_{dc}, 1.0 $V_{ac(pp)}$	45	55		dB
V_N	Output noise	Weighted filter f_o = 20 Hz to 20 kHz I_{VREGSW} = 5 mA		85	200	µV
V_{drop}	Drop out voltage	I_{VREGSW} = 800 mA			2.6	V
V_{drop}	Drop out voltage	I_{VREGSW} = 5 mA			2.3	V
I_m	Current limit	Rshort = 0Ω	1	1.5	2.5	A
TS_{EN}	VREGSW thermal shutdown	I_{VREGSW} = 500 µA; Increase Ta until VREGSW disabled	150		190	°C
t_{don}	Turn-on delay;	Ivregsw= 5mA	10	45	110	µs
t_{doff}	Turn-off delay,	I_{VREGSW} = 700 mA		45	110	µs
V8P5 (VBAT=9.5V to 18 V)						
V_o (V8P5)	Output voltage 8.5V		8.3	8.5	8.7	V
ΔV	Line regulation	VBAT = 9.5 to 18V; I = 200mA	-50	3.0	50	mV
ΔVi	Load regulation	IV8P5 = 1 to 200mA	-30	3	20	mV
PSRR	Supply voltage ripple rejection	I_{V8P5} = 100 mA; f_o = 20 to 1 kHz; VBAT = 14 V_{dc}, 1.0 $V_{ac(pp)}$	50	60		dB
		I_{V8P5} = 100 mA; f_o = 20 to 20 kHz; VBAT = 14 V_{dc}, 1.0 $V_{ac(pp)}$	35	40		dB
V_N	Output noise	Weighted filter f_o = 20 Hz to 20 kHz I_{V8P5} = 5 mA		190	450	µV
V_{drop}	Drop out voltage	IV8P5 = 200mA		0.45	0.9	V
I_m	Current limit	Rshort = 0Ω	275	450	700	mA
TS_{EN}	V8P5 thermal shutdown	I_{V8P5} = 500 µA; Increase Ta until V8P5 disabled	150		190	°C
t_{don}	Turn-on delay;	I_{V8P5} = 5mA	10	45	110	µs
t_{doff}	Turn-off delay,	I_{V8P5} = 200 mA		45	110	µs
V810 (8V) (V_{BAT} = 9.2V to 18 V)						
$V_{o\ (V810)}$	Output voltage 8.0V		7.6	8.0	8.4	V
ΔV	Line regulation	VBAT = 9.2 to 18V; I = 1000mA	-50	3	50	mV

Table 5. Electrical characteristics (continued)

(V_S = 14.4V; T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ΔVi	Load regulation	I_{V810} = 0.5 to 1000 mA	-100	-20	10	mV
PSRR	Supply voltage ripple rejection	I_{V810} = 500 mA; f_o = 20 to 1 kHz; VBAT = 14 V_{dc}, 1.0 $V_{ac(pp)}$	50	55		dB
		I_{V810} = 500 mA; f_o = 20 to 20 kHz; VBAT = 14 V_{dc}, 1.0 $V_{ac(pp)}$	30	35		dB
V_N	Output noise	Weighted filter f_o = 20 Hz to 20 kHz I_{V810} = 5 mA		175	450	µV
Vdrop	Drop out voltage	IV810(8V) = 1000mA (1)		0.45	0.9	V
I_m	Current limit	Rshort = 0Ω	1.5	2.3	3.5	A
TS_{EN}	V810(8v) thermal shutdown	$I_{V810(8V)}$ = 500 µA; Increase Ta until V810(8V) disabled	150		190	°C
t_{don}	Turn-on delay;	$I_{V810(8V)}$ = 5mA	10	45	110	µs
t_{doff}	Turn-off delay,	$I_{V810(8V)}$ = 1000 mA		45	110	µs
V810 (10V) (V_{BAT}=11.2V to 18 V)						
V_o (V810)	Output Voltage 10.0V		9.5	10.0	10.5	V
ΔV	Line regulation	VBAT = 11.2 to 18V; I = 1000mA	-50	2.5	50	mV
ΔVi	Load regulation	I_{V810} = 0.5 to 1000 mA	-100	-25	10	mV
PSRR	Supply voltage ripple rejection	I_{V810} = 500 mA; f_o = 20 to 1 kHz; VBAT = 14 V_{dc}, 1.0 $V_{ac(pp)}$	50	55		dB
		I_{V810} = 500 mA; f_o = 20 to 20 kHz; VBAT = 14 V_{dc}, 1.0 $V_{ac(pp)}$	30	35		dB
V_N	Output noise	Weighted filter f_o = 20 Hz to 20 kHz I_{V810} = 5 mA		175	450	µV
Vdrop	Drop out voltage	IV810(10V) = 1000mA (1)		0.4	0.9	V
I_m	Current limit	R_{short} = 0Ω	1.5	2.3	3.5	A
TS_{EN}	V810(10V) thermal shutdown	$I_{V810(8V)}$ = 500 µA; Increase Ta until V810(10V) disabled	150		190	°C
t_{don}	Turn-on delay;	$I_{V810(8V)}$ = 5mA	10	45	110	µs
t_{doff}	Turn-off delay,	$I_{V810(8V)}$ = 1000 mA		45	110	µs
HIGH SIDE DRIVER1						
VdropSW	Drop voltage HDS1	Idc = 100mA		0.25	0.6	V
		Idc = 200mA, t=5S		0.50	1.2	V

Table 5. Electrical characteristics (continued)

(V_S = 14.4V; T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{STG}	HSD1 short to ground current	VHSD1=0V	240	300	400	mA
I_{STB}	HSD1 short to V_{BAT} current	VHSD1=VBAT		2	10	mA
$\Delta I_{Q(VBAT)}$	HSD1 bias current change	I_{HSD1} = 0 to 100 mA; Measure change in VBAT current		0.15	10	mA
TS_{EN}	HSD1 thermal shutdown	I_{HSD1} = 500 µA; Increase Ta until HSD1 disabled	150		190	°C
t_{don}	Turn-on delay;	I_{HSD1}= 10mA	10	50	110	µs
t_{doff}	Turn-off delay,	I_{HSD1}= 100 mA		70	110	µs
t_r	Rise time	10% to 90%, I_{HSD1} = 10mA		35	75	µs
HIGH SIDE DRIVER2						
VdropSW	Drop voltage HDS2	Idc = 300mA		0.2	0.6	V
		Idc =450mA, t=5S		0.3	1.2	V
I_{STG}	HSD2 short to ground current	VHSD2=0V	0.55	0.75	1	A
I_{STB}	HSD2 short to V_{BAT} current	VHSD2=VBAT		3.5	10	mA
$\Delta I_{Q(VBAT)}$	HSD2 bias current change	I_{HSD2} = 0 to 300 mA; Measure change in VBAT current		0.15	10	mA
TS_{EN}	HSD2 thermal shutdown	IHSD2 = 500 µA; Increase Ta until HSD2 disabled	150		190	°C
t_{don}	Turn-on delay;	I_{HSD2}= 10mA	10	45	110	µs
t_{doff}	Turn-off delay,	I_{HSD2}= 300 mA		70	110	µs
t_r	Rise time	10% to 90%, I_{HSD2} = 10mA		30	75	µs
RST (open collector output)						
V_{TH}	VSTBY reset threshold	Force VSTBY low until RST* asserted	0.93 * VSTBY	0.95 * VSTBY	0.97 * VSTBY	V
V_{HYS}	Hysteresis of reset on rising VSTBY		10	50	200	mV
t_{rRST}	Rise time	10% to 90%, R_{RST}= 47 kΩ, C_{RST} = 50 pF		20	30	µs
t_{fRST}	Fall time	90% to 10%,R_{RST}= 47 kΩ, C_{RST} = 50 pF		300	1000	ns
V_{IH}_RSTDLY	RSTDLY input voltage threshold	Verify RST is de asserted	2.5	2.75	3.5	V
I_{SRC}	RSTDLY current	RSTDLY = 0 VDC	6	8.5	12	µA

Table 5. Electrical characteristics (continued)

(V_S = 14.4V; T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{por}	RST POR delay time	C_{RSTDLY} = 0.1 µF	20	30	50	ms
T_{glitch}	Glitch rejection filter time		5	12.5	20	µs
ENABLE INPUT (VREGSW, V8P5, V810, HSD1, HSD2)						
V_{IH}	Threshold recognized as high level				2.0	V
V_{IL}	Threshold recognized as low level		0.8			V
V_{HYSEN}	Hysteresis of enable		0.15	0.35		V
I_{LKGEN}	Enable input pull-down current	V_{EN} = $V_{IL(mIN)}$ to VSTBY	10	30	50	µA

1. Drop condition means that the supply voltage drop down to 100 mV from the regulated output and the regulator is sourcing its maximal load.

2. Stability Request is design info, not tested.

4 Timing diagrams

Figure 3. Timing diagram of regulators and HSD

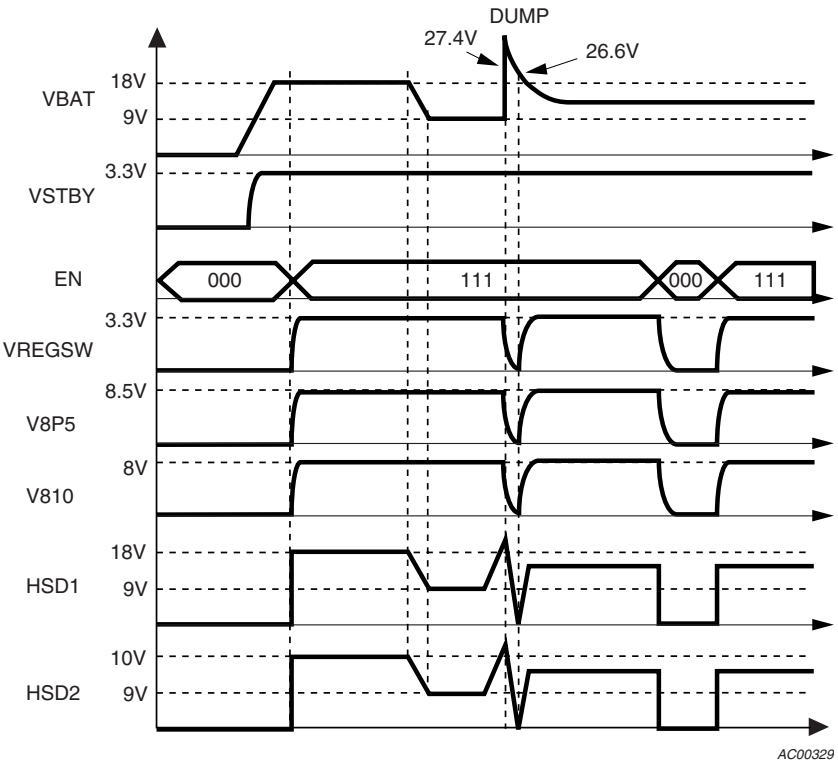


Figure 4. STCAP and RST diagram

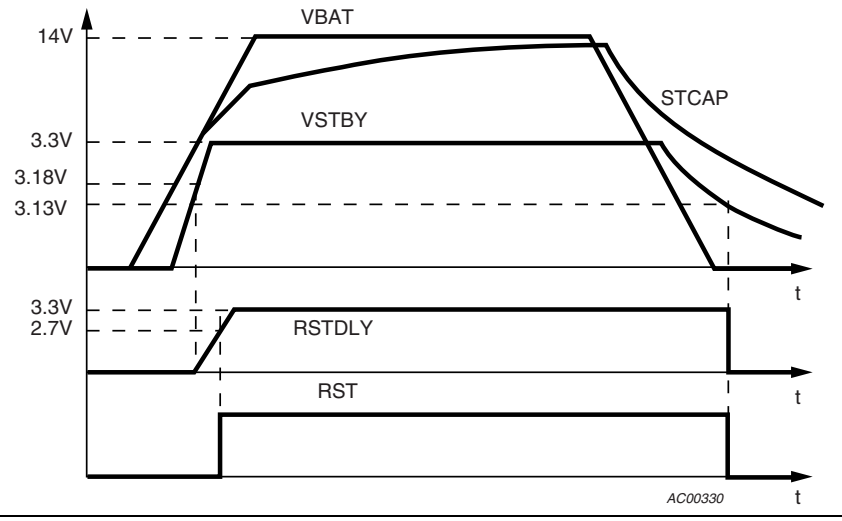


Figure 5. VBATVW (over/under voltage warning)

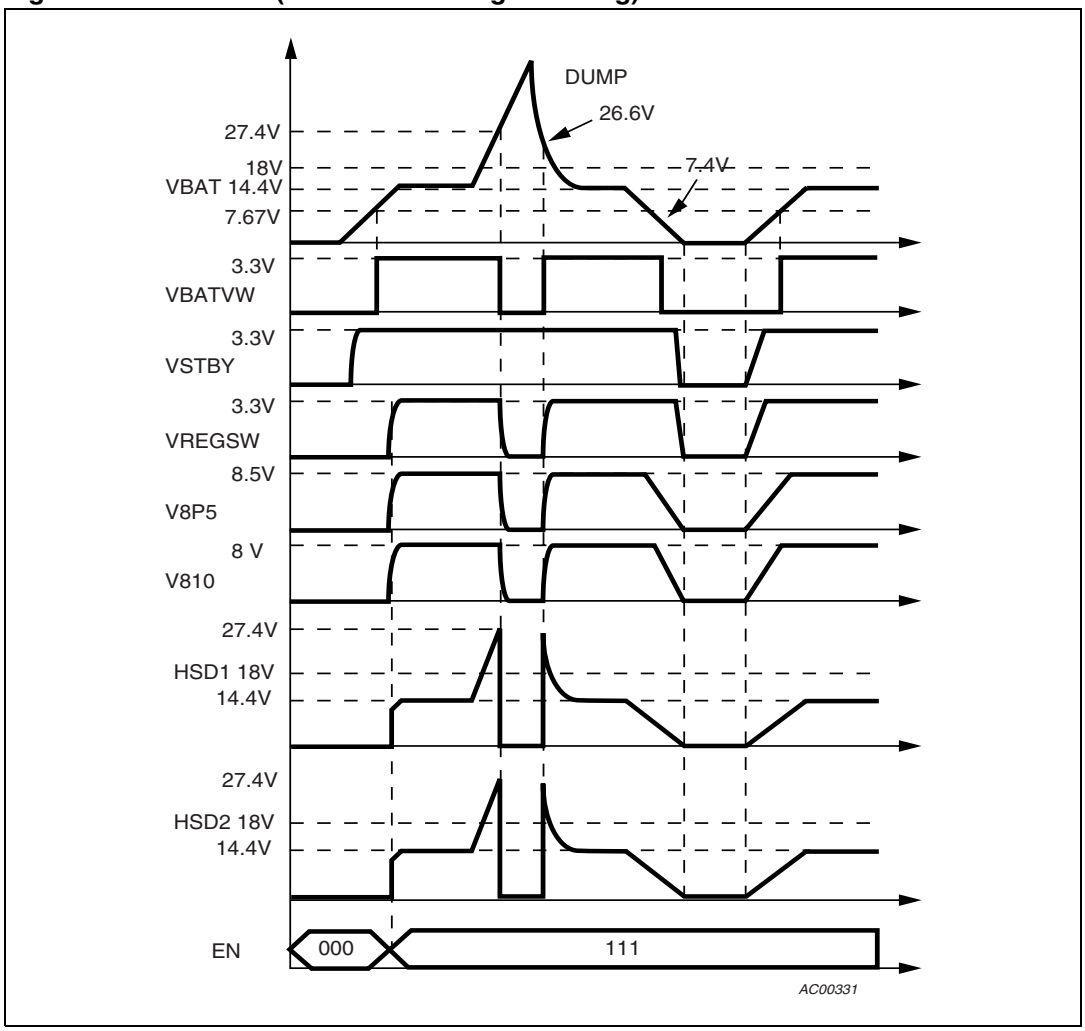


Figure 6. Independent thermal shutdown

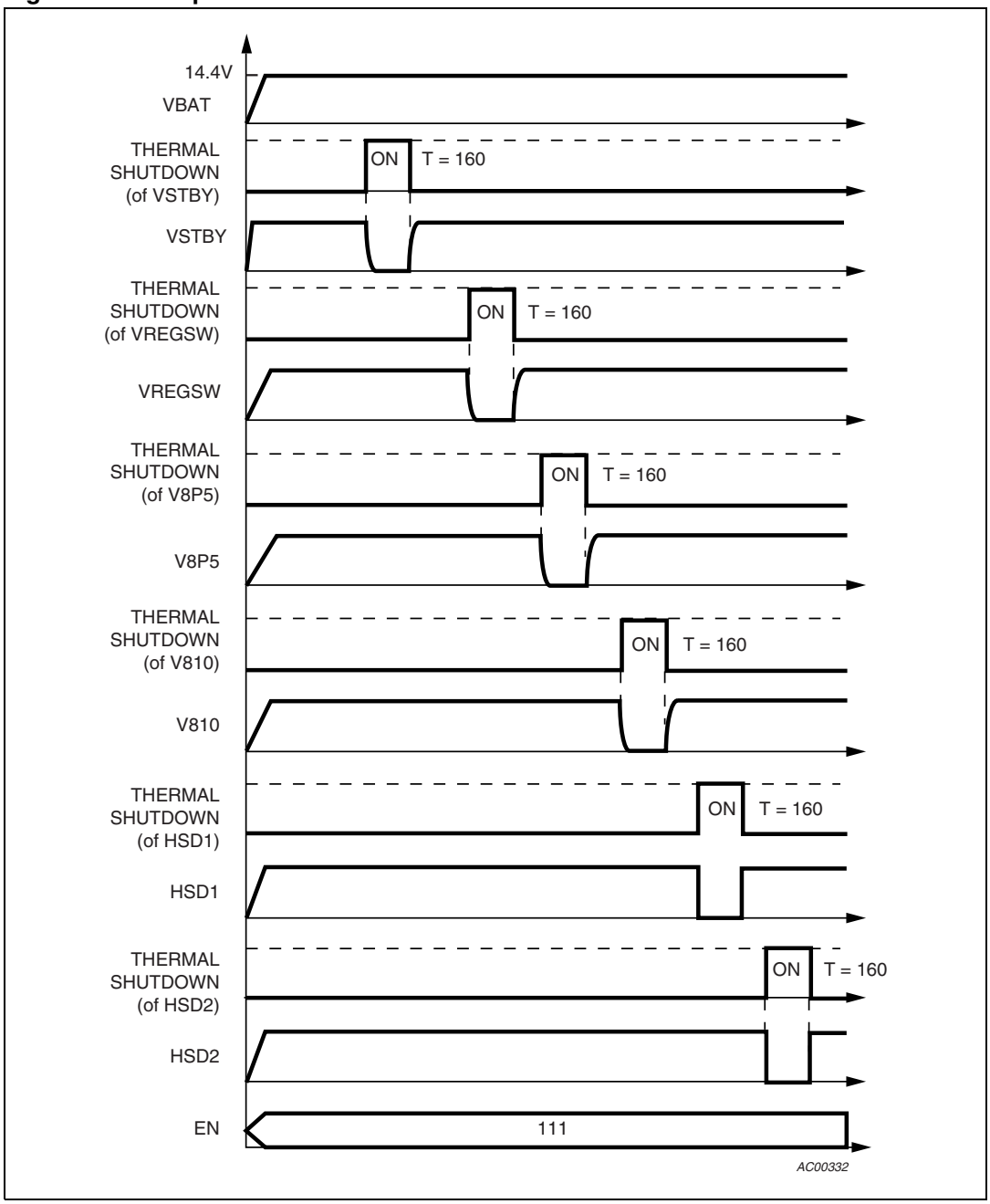


Figure 7. RST glitch rejection

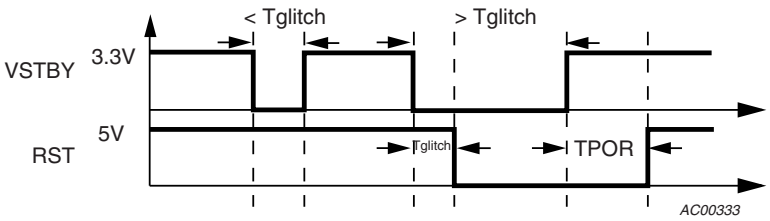
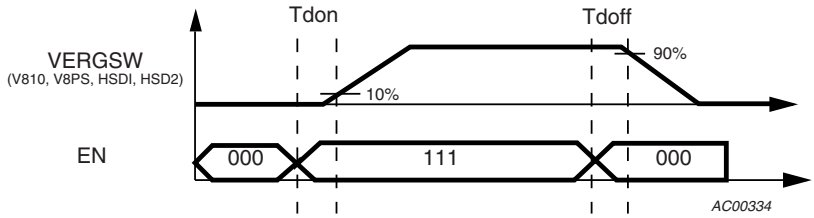


Figure 8. Enable on/off delay



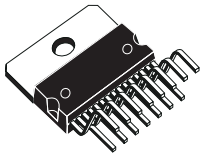
5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

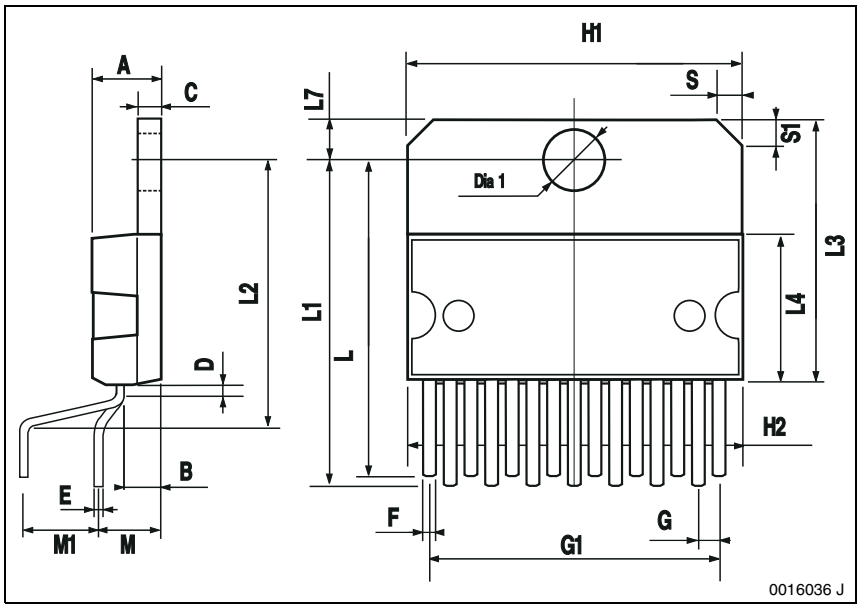
Figure 9. Multiwatt15 (vertical) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A5						0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.87	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.73	5.08	5.43	0.186	0.200	0.214
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



Multiwatt15 (Vertical)



6 Revision history

Table 6. Document revision history

Date	Revision	Changes
26-Jun-2006	1	Initial release.
28-Aug-2007	2	Minor changes, improved quality of the drawings.
17-Sep-2013	3	Updated Disclaimer.