60V Synchronous 4-Switch Buck-Boost LED Driver Controller

FEATURES

- **4-Switch Single Inductor Architecture Allows V_{IN} Above, Below or Equal to V_{OUT}**
- **Synchronous Switching: Up to 98% Efficiency**
- **Proprietary Peak-Buck Peak-Boost Current Mode**
- **Wide V_{IN} Range: 4V to 60V**
- **Wide V_{OUT} Range: 0V to 60V**
- **±4% LED Current Accuracy**
- No Top MOSFET Refresh Noise in Buck or Boost Mode
- Adjustable Frequency: 150kHz to 650kHz
- Flicker-Free Spread Spectrum for Low EMI
- Open and Short LED Protection with Fault Reporting
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive Head Lamps/Running Lamps
- High Frequency LED Lighting

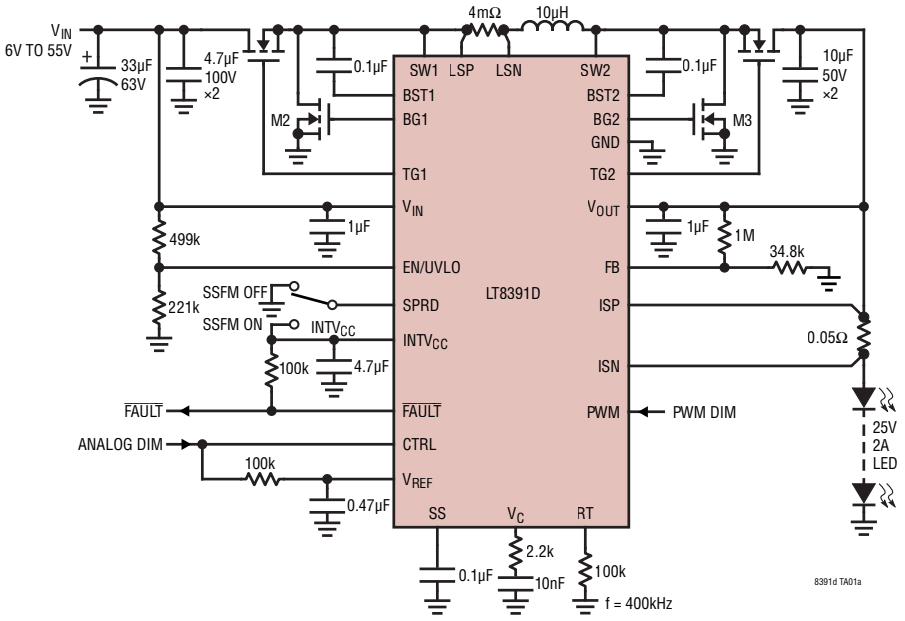
DESCRIPTION

The LT®8391D is a synchronous 4-switch buck-boost LED controller that regulates LED current from an input voltage above, below, or equal to the output voltage. The proprietary peak-buck peak-boost current mode control scheme allows adjustable 150kHz to 650kHz fixed frequency operation, or internal ±15% triangle spread spectrum operation for low EMI. With 4V to 60V input, 0V to 60V output, and seamless low noise transitions between operation regions, the LT8391D is ideal for LED driver applications in automotive, industrial, and battery-powered systems.

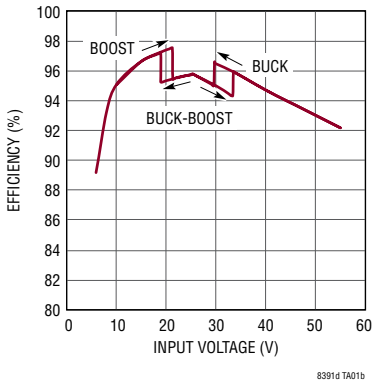
The LT8391D provides LED current PWM dimming with an option low-side NMOS switch. The CTRL pin provides flexible 20:1 analog dimming with ±4% LED current accuracy at 100mV full scale. Fault protection is provided to detect an open or short LED condition, during which the LT8391D retries, latches off, or keeps running.

TYPICAL APPLICATION

98% Efficient 50W (25V, 2A) Buck-Boost LED Driver



Efficiency vs V_{IN}

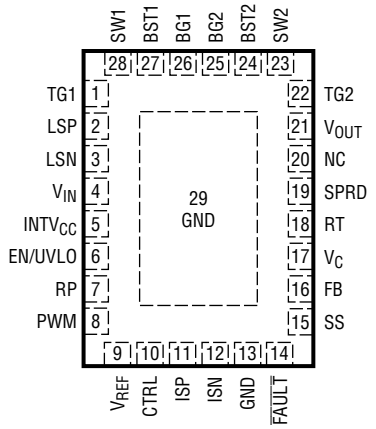


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO, V_{OUT}, ISP, ISN ..... –0.3V to 60V
(ISP–ISN)..... –1V to 1V
BST1, BST2..... –0.3V to 66V
SW1, SW2, LSP, LSN ..... –5V to 60V
$INTV_{CC}$, (BST1–SW1), (BST2–SW2) ..... –0.3V to 6V
(BST1–LSP), (BST1–LSN) ..... –0.3V to 6V
RP, RT, SS, V_C, V_{REF}..... –0.3V to 4V
FB, PWM, SPRD, CTRL, $\overline{FAULT}$ ..... –0.3V to 6V
BG1, BG2, TG1, TG2 ..... (Note 2)
Operating Junction Temperature Range (Notes 3, 4)
LT8391DJ ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFDM PACKAGE
28-LEAD (4mm × 5mm) PLASTIC SIDE WETTABLE QFN
θ_{JA} = 34°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
AUTOMOTIVE PRODUCTS*				
LT8391DJUFDM#WPBF	LT8391DJUFDM#WTRPBF	8391D	28-Lead (4mm × 5mm) Plastic Side Solderable QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

*Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2). V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{IN} Operating Voltage Range		●	4		60	V
	V_{IN} Quiescent Current	$V_{EN/UVLO}$ = 0.3V Not Switching			1 2.1	2 2.8	µA mA
	V_{OUT} Voltage Range		●	0		60	V
Linear Regulators							
	$INTV_{CC}$ Regulation Voltage	I_{INTVCC} = 20mA		4.85	5.0	5.15	V
	$INTV_{CC}$ Current Limit	V_{INTVCC} = 4.5V		80	120	160	mA
	$INTV_{CC}$ Undervoltage Lockout Threshold	Falling		3.44	3.54	3.64	V
	$INTV_{CC}$ Undervoltage Lockout Hysteresis				0.24		V
	V_{REF} Regulation Voltage	I_{VREF} = 100µA	●	1.96	2.00	2.04	V
Control Inputs/Outputs							
	EN/UVLO Shutdown Threshold		●	0.3	0.6	1.0	V
	EN/UVLO Enable Threshold	Falling	●	1.196	1.220	1.244	V
	EN/UVLO Enable Hysteresis				13		mV
	EN/UVLO Hysteresis Current	$V_{EN/UVLO}$ = 1.1V $V_{EN/UVLO}$ = 1.3V		2.1 –0.1	2.5 0	2.9 0.1	µA µA
PWM Dimming							
	PWM Dimming Threshold Voltage		●	0.4		1.5	V
Error Amplifier							
	Full Scale LED Current Regulation $V_{(ISP-ISN)}$	V_{CTRL} = 2V, V_{ISP} = 12V V_{CTRL} = 2V, V_{ISP} = 0V	● ●	96 96	100 100	104 104	mV mV
	ISP/ISN Input Common Mode Range		●	0		50	V
	LED Current Regulation Amplifier g_m				2000		µS
	FB Regulation Voltage	V_C = 1.2V	●	0.98	1.00	1.02	V
	FB Voltage Regulation Amplifier g_m				660		µS
Current Comparator							
	Maximum Current Sense Threshold $V_{(LSP-LSN)}$	Buck, V_{FB} = 0.8V Boost, V_{FB} = 0.8V	● ●	34 38	48 48	62 58	mV mV
Fault							
	FB Overvoltage Threshold (V_{FB})	Rising		1.03	1.05	1.07	V
	FB Overvoltage Hysteresis			15	25	35	mV
	FB Open LED Threshold (V_{FB})	Rising, $V_{(ISP-ISN)}$ = 0V		0.93	0.95	0.97	V
	FB Open LED Hysteresis	$V_{(ISP-ISN)}$ = 0V		35	50	65	mV
	FB Short LED Threshold (V_{FB})	Falling		0.04	0.05	0.06	V
	FB Short LED Hysteresis	Hysteresis		35	50	65	mV
	$\overline{FAULT}$ Pull-Down Resistance				100	200	Ω
	SS Hard Pull-Down Resistance	$V_{EN/UVLO}$ = 1.1V			100	200	Ω
	SS Pull-Up Current	V_{FB} = 0.8V, V_{SS} = 0V		10	12.5	15	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2). V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	SS Pull-Down Current	V_{FB} = 1.0V, V_{SS} = 2V		1	1.25	1.5	µA
	SS Fault Latch-Off Threshold	Falling			1.7		V
	SS Fault Reset Threshold				0.2		V
Oscillator							
	Switching Frequency	V_{SPRD} = 0V, R_T = 226k V_{SPRD} = 0V, R_T = 100k	● ●	190 380	200 400	210 420	kHz kHz
NMOS Drivers							
	TG1, TG2 Gate Driver On-Resistance Gate Pull-Up Gate Pull-Down	$V_{(BST-SW)}$ = 5V			 2.6 1.4		 Ω Ω
	BG1, BG2 Gate Driver On-Resistance Gate Pull-Up Gate Pull-Down	V_{INTVCC} = 5V			 3.2 1.2		 Ω Ω
	TG Off to BG On Delay	C_L = 3.3nF			60		ns
	BG Off to TG On Delay	C_L = 3.3nF			60		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

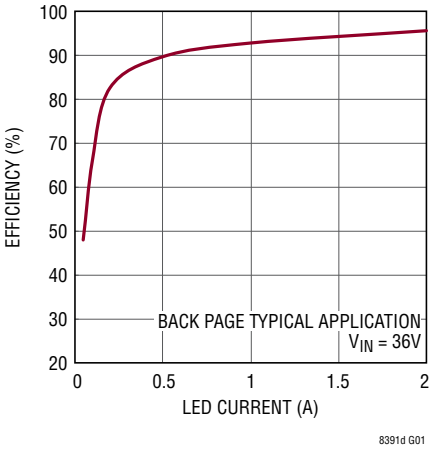
Note 2: Do not apply a positive or negative voltage source to these pins, otherwise permanent damage may occur.

Note 3: The LT8391DJ is guaranteed over the –40°C to 150°C operating junction temperature range.

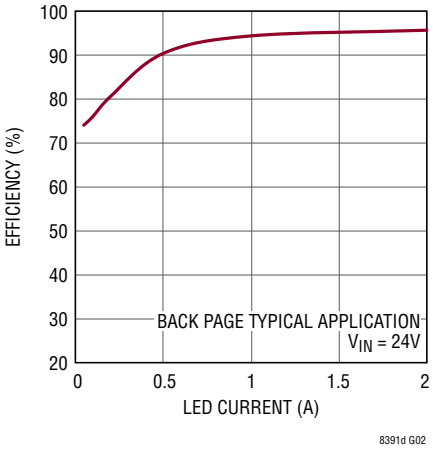
Note 4: The LT8391D includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

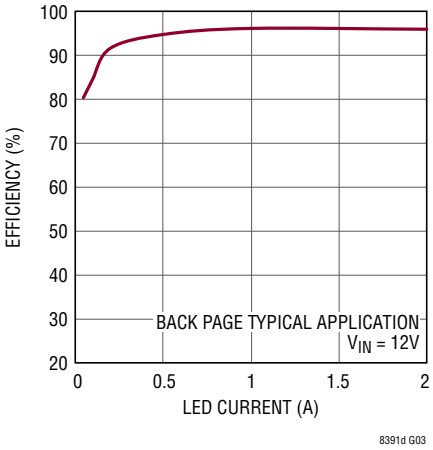
Efficiency vs LED Current (Buck Region)



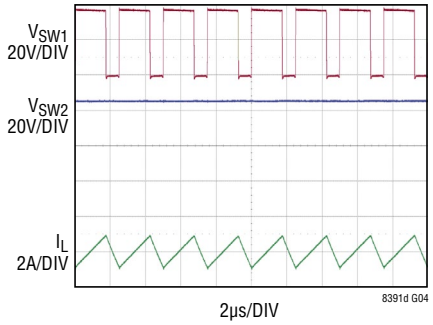
Efficiency vs LED Current (Buck-Boost Region)



Efficiency vs LED Current (Boost Region)

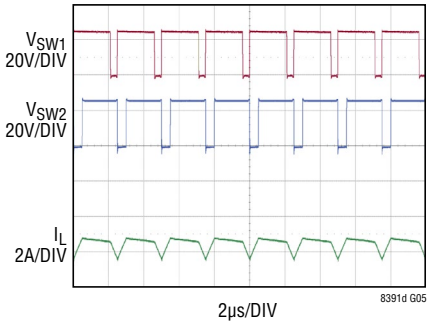


Switching Waveforms (Buck Region)



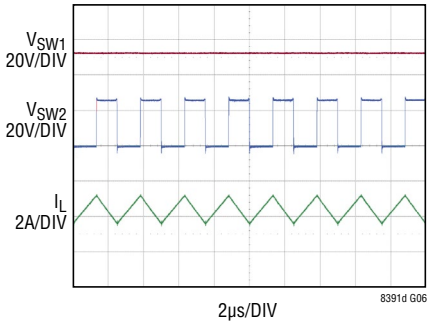
BACK PAGE TYPICAL APPLICATION
V_{IN} = 36V, I_{LED} = 2A

Switching Waveforms (Buck-Boost Region)



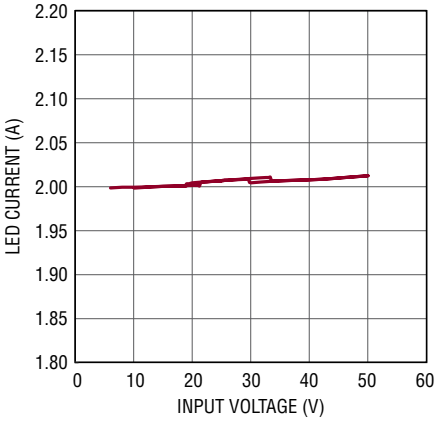
BACK PAGE TYPICAL APPLICATION
V_{IN} = 24V, I_{LED} = 2A

Switching Waveforms (Boost Region)

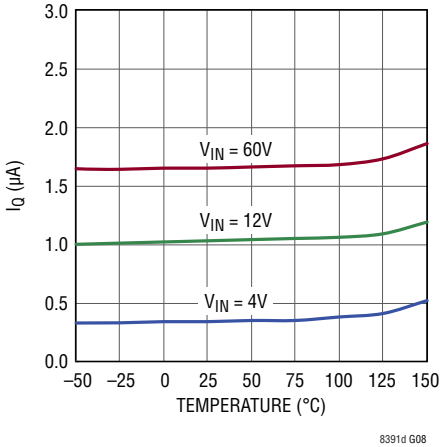


BACK PAGE TYPICAL APPLICATION
V_{IN} = 12V, I_{LED} = 2A

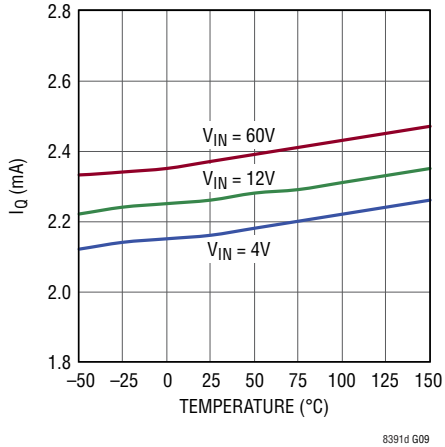
LED Current vs V_{IN}



V_{IN} Shutdown Current

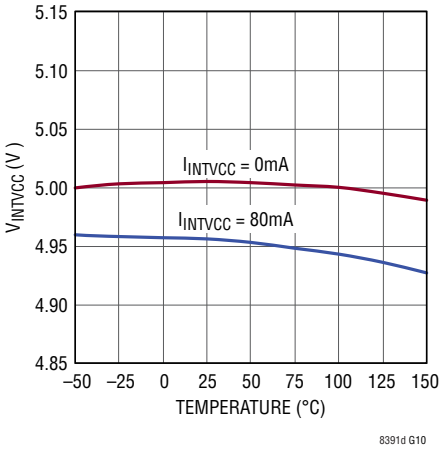


V_{IN} Quiescent Current

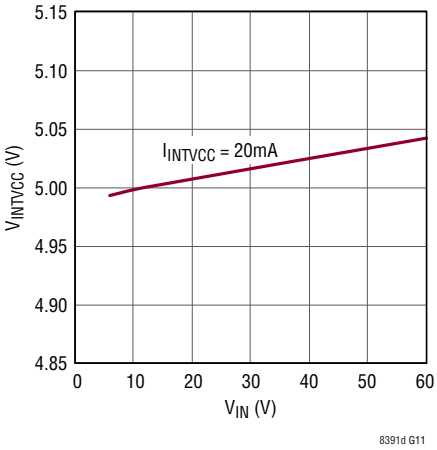


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

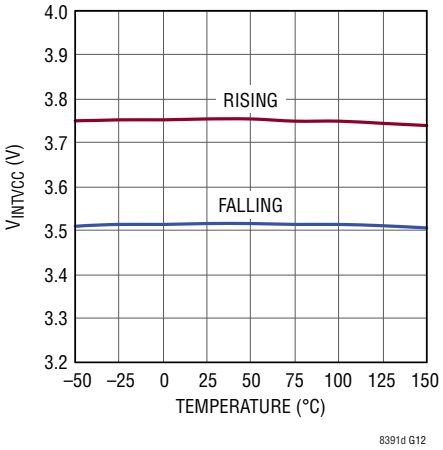
$INTV_{CC}$ Voltage vs Temperature



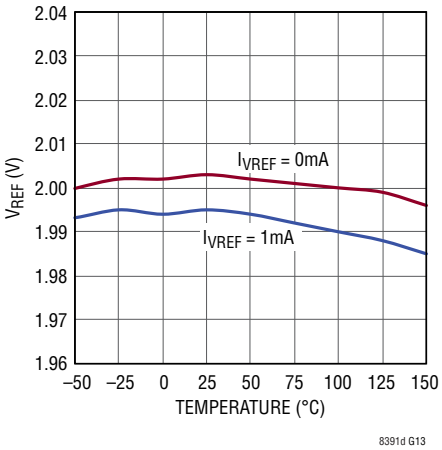
$INTV_{CC}$ Voltage vs V_{IN}



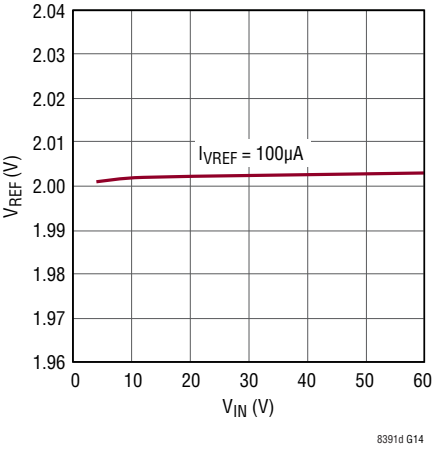
$INTV_{CC}$ UVLO Threshold



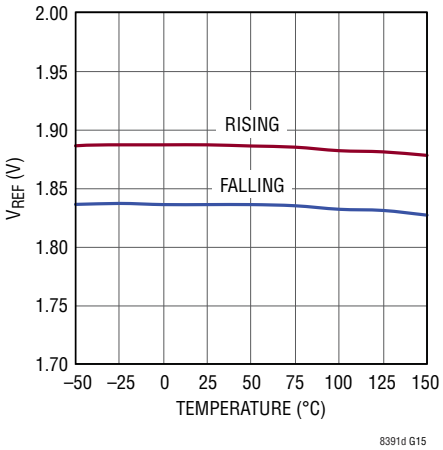
V_{REF} Voltage vs Temperature



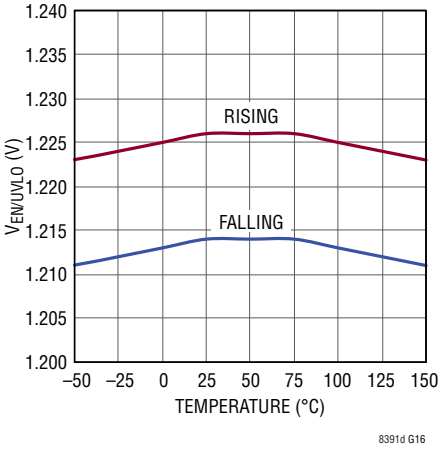
V_{REF} Voltage vs V_{IN}



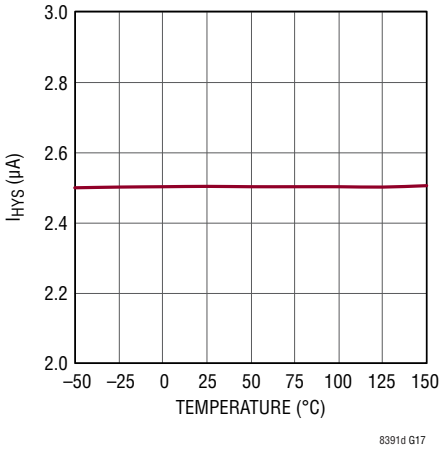
V_{REF} UVLO Threshold



EN/UVLO Enable Threshold

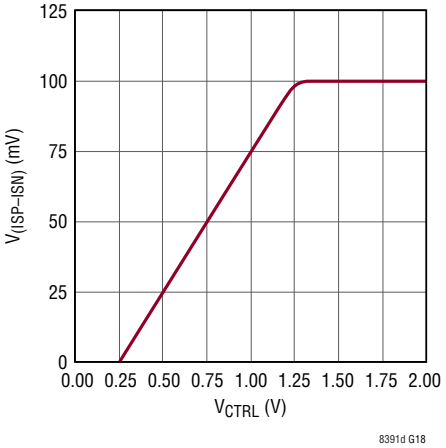


EN/UVLO Hysteresis Current

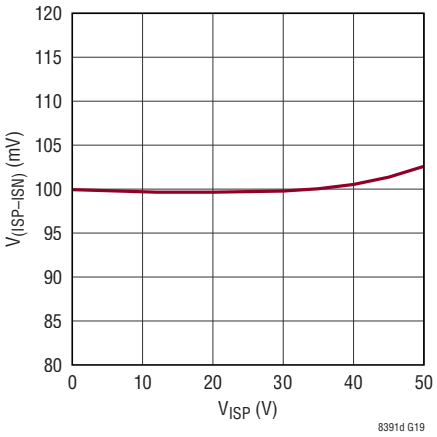


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

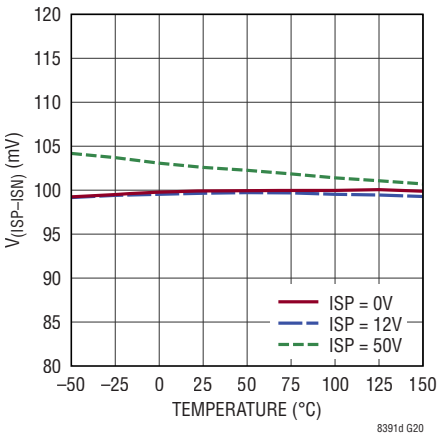
$V_{(ISP-ISN)}$ Regulation vs V_{CTRL}



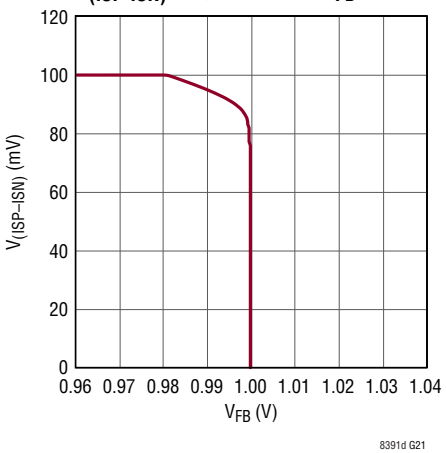
$V_{(ISP-ISN)}$ Regulation vs V_{ISP}



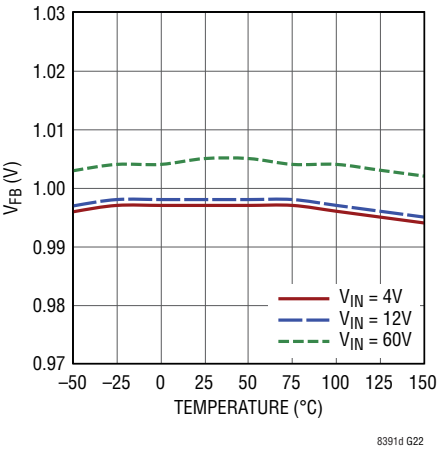
$V_{(ISP-ISN)}$ Regulation vs Temperature



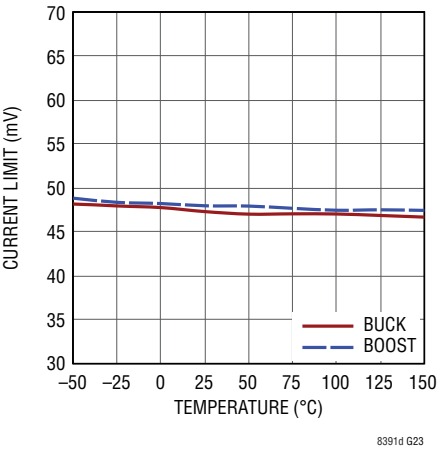
$V_{(ISP-ISN)}$ Regulation vs V_{FB}



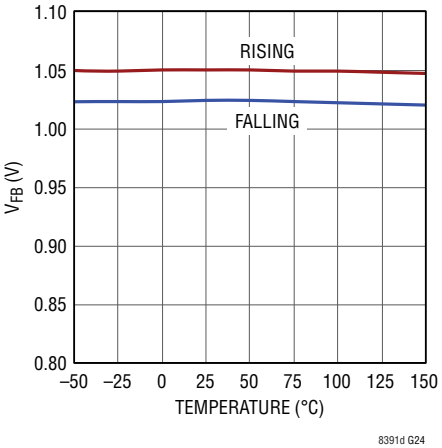
FB Regulation vs Temperature



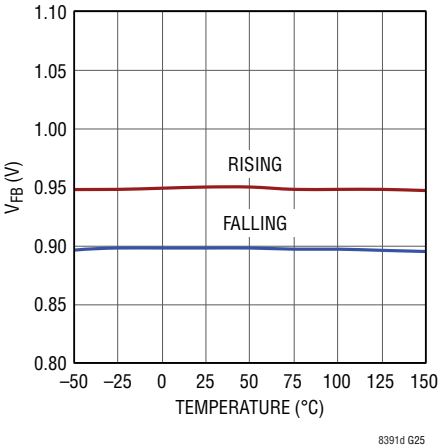
Maximum Current Sense vs Temperature



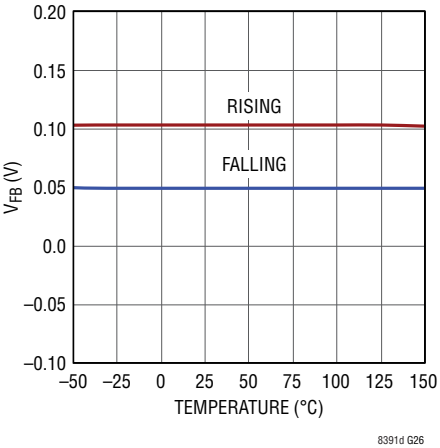
FB Overvoltage Threshold



FB Open LED Threshold

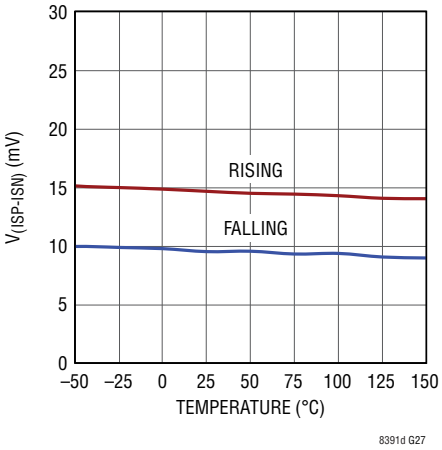


FB Short LED Threshold

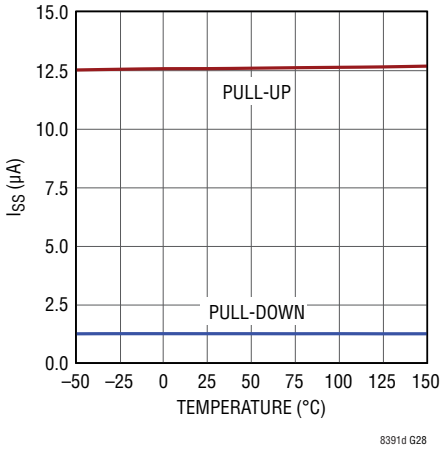


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

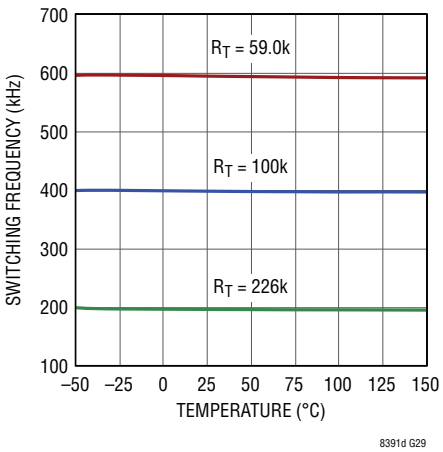
ISP/ISN Open LED Threshold



SS Current vs Temperature



Oscillator Frequency vs Temperature



PIN FUNCTIONS

TG1 (Pin 1): Buck Side Top Gate Drive. Drives the gate of buck side top N-channel MOSFET with a voltage swing from SW1 to BST1.

LSP (Pin 2): Positive Terminal of the Buck Side Inductor Current Sense Resistor (R_{SENSE}). Ensure accurate current sense with Kelvin connection.

LSN (Pin 3): Negative Terminal of the Buck Side Inductor Current Sense Resistor (R_{SENSE}). Ensure accurate current sense with Kelvin connection.

V_{IN} (Pin 4): Input Supply. The V_{IN} pin must be tied to the power input to determine the buck, buck-boost, or boost operation regions. Locally bypass this pin to ground with a minimum 1µF ceramic capacitor.

$INTV_{CC}$ (Pin 5): Internal 5V Linear Regulator Output. The $INTV_{CC}$ linear regulator is supplied from the V_{IN} pin, and powers the internal control circuitry and gate drivers. Locally bypass this pin to ground with a minimum 4.7µF ceramic capacitor.

EN/UVLO (Pin 6): Enable and Undervoltage Lockout. Force the pin below 0.3V to shut down the part and reduce V_{IN} quiescent current below 2µA. Force the pin above 1.233V for normal operation. The accurate 1.220V falling threshold can be used to program an undervoltage lockout (UVLO) threshold with a resistor divider from V_{IN} to ground. An accurate 2.5µA pull-down current allows the programming of V_{IN} UVLO hysteresis. If neither function is used, tie this pin directly to V_{IN}.

RP (Pin 7): Factory Test Pin. Tie this pin to ground for normal operation.

PWM (Pin 8): PWM Dimming Input. For PWM dimming, drive this pin with a digital pulse from 0V to a voltage higher than 1.5V to control PWM dimming of the LED string. If PWM dimming is not used, tie this pin to $INTV_{CC}$. Forcing the pin low turns off TG1 and TG2, turns on BG1 and BG2, disconnects the V_C pin from all internal loads.

V_{REF} (Pin 9): Voltage Reference Output. The V_{REF} pin provides an accurate 2V reference capable of supplying 1mA current. Locally bypass this pin to ground with a 0.47µF ceramic capacitor.

CTRL (Pin 10): Control Input for LED Current Sense Threshold. The CTRL pin is used to program the LED regulation current:

$$I_{LED} = \frac{Min(V_{CTRL} - 0.25V, 1V)}{10 \bullet R_{LED}}$$

The V_{CTRL} can be set by an external voltage reference or a resistor divider from V_{REF} to ground. For $0.25V \le V_{CTRL} \le 1.15V$, the current sense threshold linearly goes up from 0mV to 90mV. For $V_{CTRL} \ge 1.35V$, the current sense threshold is constant at 100mV full scale value. For $1.15V \le V_{CTRL} \le 1.35V$, the current sense threshold smoothly transitions from the linear function of V_{CTRL} to the 100mV constant value. Tie CTRL to V_{REF} for the 100mV full scale threshold.

ISP (Pin 11): Positive Terminal of the LED Current Sense Resistor (R_{LED}). Ensure accurate current sense with Kelvin connection.

ISN (Pin 12): Negative Terminal of the LED Current Sense Resistor (R_{LED}). Ensure accurate current sense with Kelvin connection.

GND (Pin 13, Exposed Pad): Ground. Solder the exposed pad directly to the ground plane.

$\overline{FAULT}$ (Pin 14): LED Fault Open Drain Output. The $\overline{FAULT}$ pin is pulled low when any of the following conditions happens:

1. Open LED ($V_{FB} > 0.95V$
2. Short LED ($V_{FB} < 0.05V$)

To function, the pin requires an external pull-up resistor. The $\overline{FAULT}$ status is updated only during PWM high state and latched during PWM low state.

SS (Pin 15): Soft-Start Timer Setting. The SS pin is used to set soft-start timer by connecting a capacitor to ground. An internal 12.5µA pull-up current charging the external SS capacitor gradually ramps up FB regulation voltage. A 0.1µF capacitor is recommended on this pin. Any UVLO or thermal shutdown immediately pulls SS pin to ground and stops switching. Using a single resistor from SS to V_{REF},

PIN FUNCTIONS

the LT8391D can be set in three different fault protection modes during open or short LED fault conditions: hiccup (no resistor), latchoff (499k), and keep-running (100k). See more details in the Application Information section.

FB (Pin 16): Voltage Loop Feedback Input. The FB pin is used for constant-voltage regulation and LED fault protection. The internal error amplifier with its output V_C regulates V_{FB} to 1.00V through the DC/DC converter. During open LED (V_{FB} > 0.95V or short LED (V_{FB} < 0.05V) fault conditions, the part pulls the $\overline{FAULT}$ pin low and gets into one fault mode per customer setting. During an overvoltage (V_{FB} > 1.05V) condition, the part turns off all TG1, BG1, TG2, BG2.

V_C (Pin 17): Error Amplifier Output to Set Inductor Current Comparator Threshold. The V_C pin is used to compensate the control loop with an external RC network. During PWM low state, the V_C pin is disconnected from all internal loads to store its voltage information for the highest PWM dimming performance.

RT (Pin 18): Switching Frequency Setting. Connect a resistor from this pin to ground to set the internal oscillator frequency from 150kHz to 650kHz.

SPRD (Pin 19): Spread Spectrum. Ground this pin for switching at internal oscillator frequency. Tie to $INTV_{CC}$ for ±15% triangle spread spectrum around internal oscillator frequency.

NC (Pin 20): No Internal Connection Pin.

V_{OUT} (Pin 21): Output Supply. The V_{OUT} pin must be tied to the power output to determine the buck, buck-boost, or boost operation regions. The V_{OUT} pin also serves as positive rail for the PWMTG drive. Locally bypass this pin to ground with a minimum 1µF ceramic capacitor.

TG2 (Pin 22): Boost Side Top Gate Drive. Drives the gate of boost side top N-Channel MOSFET with a voltage swing from SW2 to BST2.

SW2 (Pin 23): Boost Side Switch Node. The SW2 pin swings from a Schottky diode voltage drop below ground to V_{OUT}.

BST2 (Pin 24): Boost Side Bootstrap Floating Driver Supply. The BST2 pin has an integrated bootstrap Schottky diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW2 pin. The BST2 pin swings from a diode voltage drop below $INTV_{CC}$ to (V_{OUT} + $INTV_{CC}$).

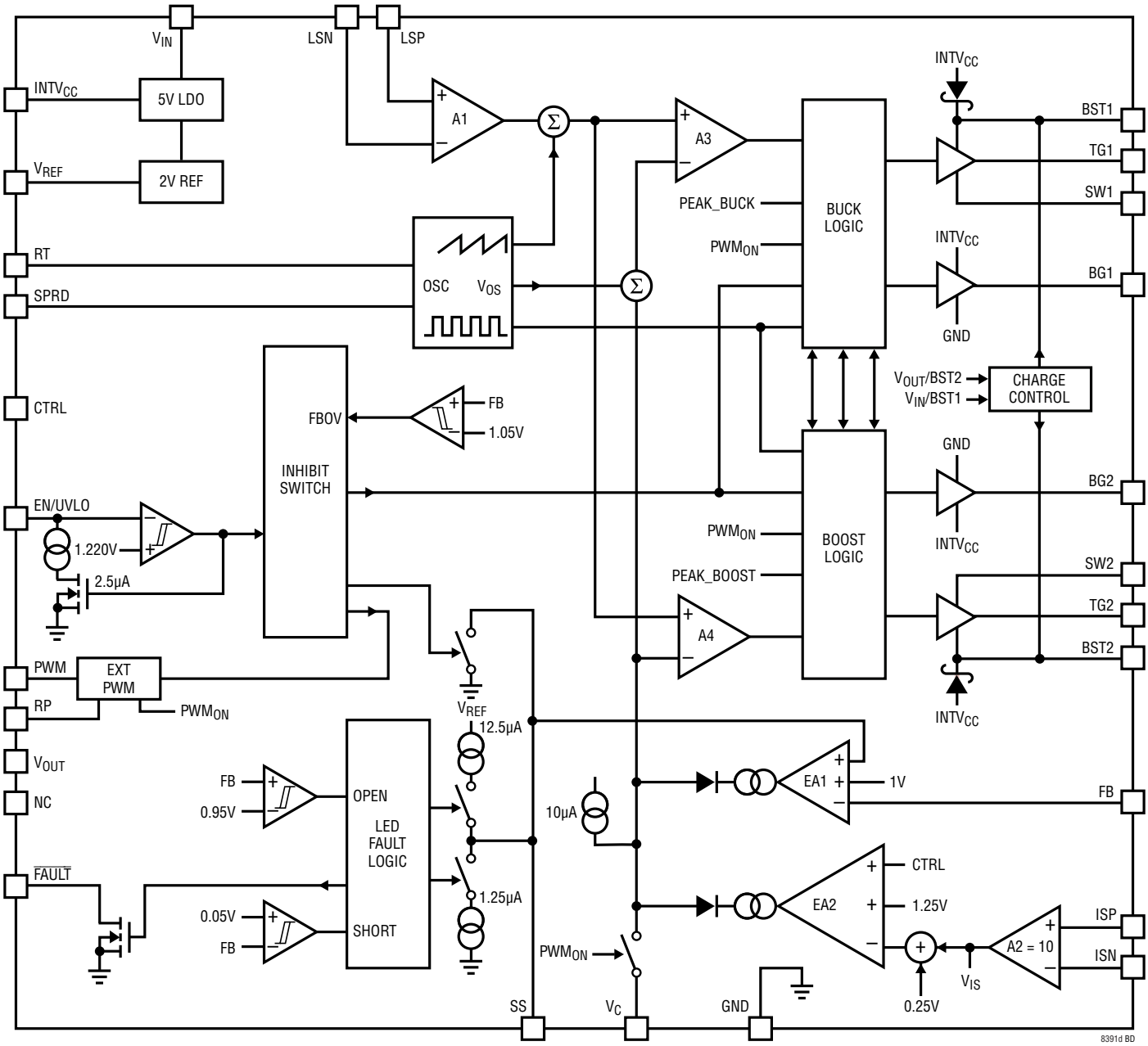
BG2 (Pin 25): Boost Side Bottom Gate Drive. Drives the gate of boost side bottom N-Channel MOSFET with a voltage swing from ground to $INTV_{CC}$.

BG1 (Pin 26): Buck Side Bottom Gate Drive. Drives the gate of buck side bottom N-channel MOSFET with a voltage swing from ground to $INTV_{CC}$.

BST1 (Pin 27): Buck Side Bootstrap Floating Driver Supply. The BST1 pin has an integrated bootstrap Schottky diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW1 pin. The BST1 pin swings from a diode voltage drop below $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

SW1 (Pin 28): Buck Side Switch Node. The SW1 pin swings from a Schottky diode voltage drop below ground up to V_{IN}.

BLOCK DIAGRAM



OPERATION

The LT8391D is a current mode LED controller that can regulate LED current from input voltage above, below, or equal to the LED string voltage. The ADI proprietary peak-buck peak-boost current mode control scheme uses a single inductor current sense resistor and provides smooth transition between buck region, buck-boost region, and boost region. Its operation is best understood by referring to the Block Diagram.

Power Switch Control

Figure 1 shows a simplified diagram of how the four power switches A, B, C, and D are connected to the inductor L, the current sense resistor R_{SENSE}, power input V_{IN}, power output V_{OUT}, and ground. The current sense resistor R_{SENSE} connected to the LSP and LSN pins provides inductor current information for both peak current mode control and reverse current detection in buck region, buck-boost region, and boost region. Figure 2 shows the current mode control as a function of V_{IN}/V_{OUT} ratio and Figure 3 shows the operation region as a function of V_{IN}/V_{OUT} ratio. The power switches are properly controlled to smoothly transition between modes and regions. Hysteresis is added to prevent chattering between modes and regions.

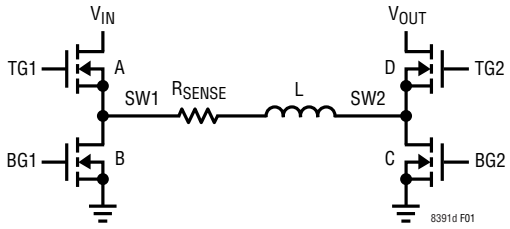


Figure 1. Simplified Diagram of the Power Switches

There are total four states: (1) peak-buck current mode control in buck region, (2) peak-buck current mode control in buck-boost region, (3) peak-boost current mode control in buck-boost region, and (4) peak-boost current mode control in boost region. The following sections give detailed description for each state with waveforms, in which the shoot-through protection dead time between switches A and B, between switches C and D are ignored for simplification.

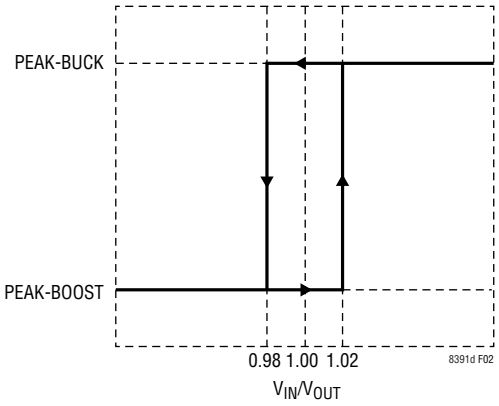


Figure 2. Current Mode vs V_{IN}/V_{OUT} Ratio

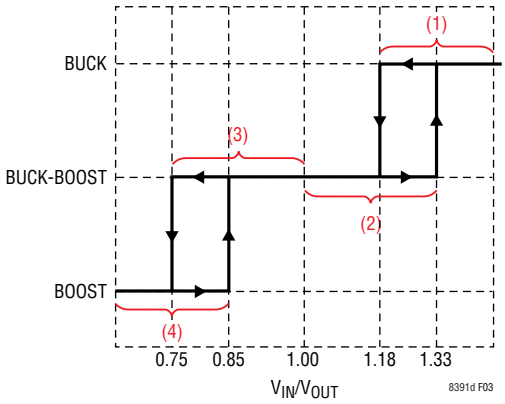


Figure 3. Operation Region vs V_{IN}/V_{OUT} Ratio

Peak-Buck in Buck Region (V_{IN} >> V_{OUT})

When V_{IN} is much higher than V_{OUT}, the LT8391D uses peak-buck current mode control in buck region (Figure 4). Switch C is always off and switch D is always on. At the beginning of every cycle, switch A is turned on and the inductor current ramps up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A3 during (A+D) phase, switch A is turned off and switch B is turned on for the rest of the cycle. Switches A and B will alternate, behaving like a typical synchronous buck regulator.

OPERATION

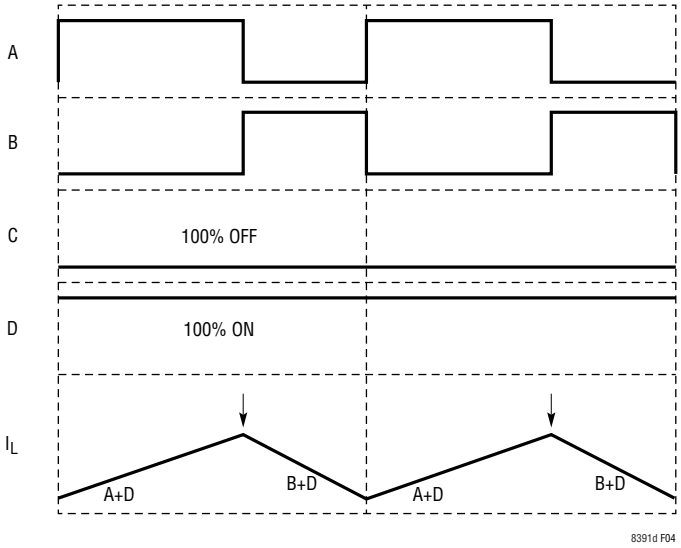


Figure 4. Peak-Buck in Buck Region (V_{IN} >> V_{OUT})

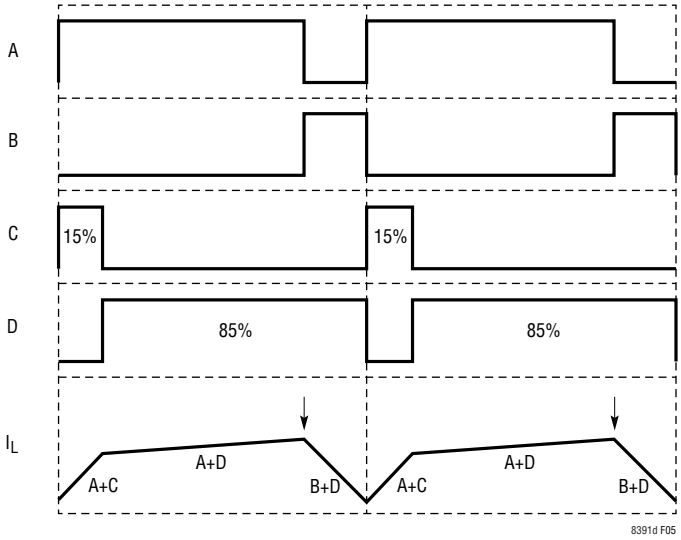


Figure 5. Peak-Buck in Buck-Boost Region (V_{IN} ~> V_{OUT})

Peak-Buck in Buck-Boost Region (V_{IN} ~> V_{OUT})

When V_{IN} is slightly higher than V_{OUT}, the LT8391D uses peak-buck current mode control in buck-boost region (Figure 5). Switch C is always turned on for the beginning 15% cycle and switch D is always turned on for the remaining 85% cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. After 15% cycle, switch C is turned off and switch D is turned on, and the inductor keeps ramping up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A3 during (A+D) phase, switch A is turned off and switch B is turned on for the rest of the cycle.

Peak-Boost in Buck-Boost Region (V_{IN} <~ V_{OUT})

When V_{IN} is slightly lower than V_{OUT}, the LT8391D uses peak-boost current mode control in buck-boost region (Figure 6). Switch A is always turned on for the beginning 85% cycle and switch B is always turned on for the remaining 15% cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A4 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of the cycle. After 85% cycle, switch A is turned off and switch B is turned on for the rest of the cycle.

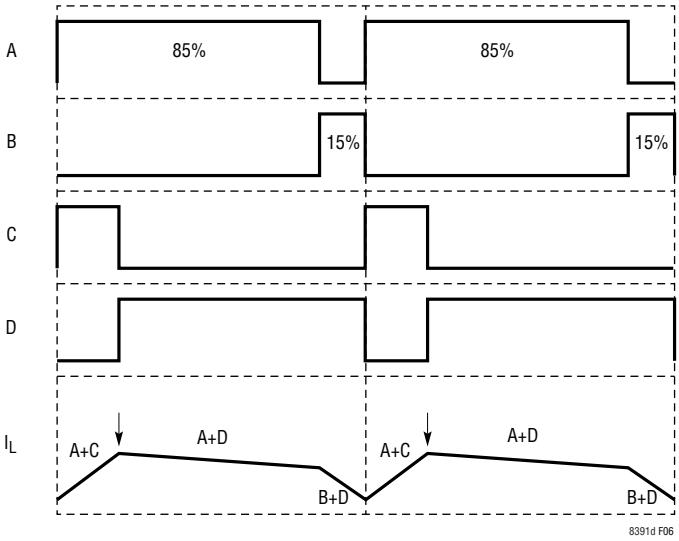


Figure 6. Peak-Boost in Buck-Boost Region (V_{IN} <~ V_{OUT})

Peak-Boost in Boost Region (V_{IN} << V_{OUT})

When V_{IN} is much lower than V_{OUT}, the LT8391D uses peak-boost current mode control in boost region (Figure 7). Switch A is always on and switch B is always off. At the beginning of every cycle, switch C is turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A4 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of the cycle. Switches C and D will alternate, behaving like a typical synchronous boost regulator.

OPERATION

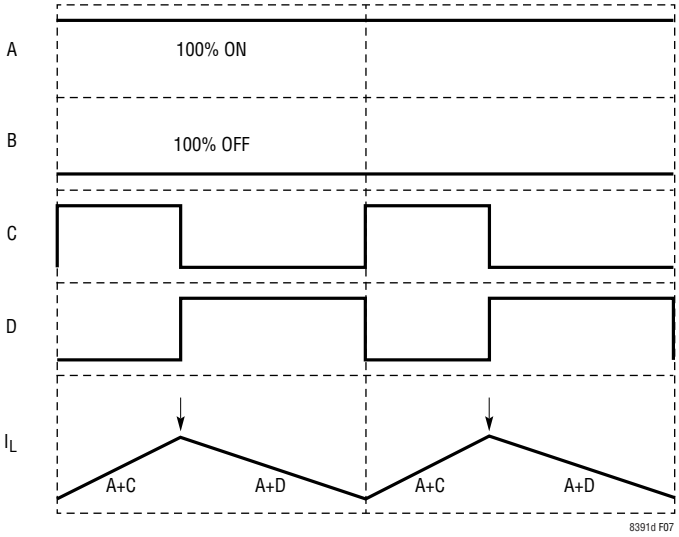


Figure 7. Peak-Boost in Boost Region (V_{IN} << V_{OUT})

Main Control Loop

The LT8391D is a fixed frequency current mode controller. The inductor current is sensed through the inductor sense resistor between the LSP and LSN pins. The current sense voltage is gained up by amplifier A1 and added to a slope compensation ramp signal from the internal oscillator. The summing signal is then fed into the positive terminals of the buck current comparator A3 and boost current comparator A4. The negative terminals of A3 and A4 are controlled by the voltage on the V_C pin, which is the diode-OR of error amplifiers EA1 and EA2.

Depending on the state of the peak-buck peak-boost current mode control, either the buck logic or the boost logic is controlling the four power switches so that either the FB voltage is regulated to 1V or the current sense voltage between the ISP and ISN pins is regulated by the CTRL pin during normal operation. The gains of EA1 and EA2 have been balanced to ensure smooth transition between constant-voltage and constant-current operation with the same compensation network.

Light Load Current Operation

At light load, the LT8391D runs in discontinuous conduction mode.

In the buck region, switch B is turned off whenever the buck reverse current threshold is triggered during (B+D) phase. In the boost region, switch D is turned off whenever the boost reverse current threshold is triggered during (A+D) phase. In the buck-boost region, switch D is turned off whenever the boost reverse current threshold is triggered during (A+D) phase, and both switches B and D are turned off whenever the buck reverse current threshold is triggered during (B+D) phase.

Internal Charge Path

Each of the two top MOSFET drivers is biased from its floating bootstrap capacitor, which is normally recharged by $INTV_{CC}$ through both the external and internal bootstrap diodes when the top MOSFET is turned off. When the LT8391D operates exclusively in the buck or boost regions, one of the top MOSFETs is constantly on. An internal charge path, from V_{OUT} and BST2 to BST1 or from V_{IN} and BST1 to BST2, charges the bootstrap capacitor to 4.6V so that the top MOSFET can be kept on.

Shutdown and Power-On-Reset

The LT8391D enters shutdown mode and drains less than 2µA quiescent current when the EN/UVLO pin is below its shutdown threshold (0.3V minimum). Once the EN/UVLO pin is above its shutdown threshold (1V maximum), the LT8391D wakes up startup circuitry, generates bandgap reference, and powers up the internal $INTV_{CC}$ LDO. The $INTV_{CC}$ LDO supplies the internal control circuitry and gate drivers. Now the LT8391D enters undervoltage lockout (UVLO) mode with a hysteresis current (2.5µA typical) pulled into the EN/UVLO pin. When the $INTV_{CC}$ pin is charged above its rising UVLO threshold (3.78V typical), the EN/UVLO pin passes its rising enable threshold (1.233V typical), and the junction temperature is less than its thermal shutdown (165°C typical), the LT8391D enters enable mode, in which the EN/UVLO hysteresis current is turned off and the voltage reference V_{REF} is being charged up from ground. From the time of entering enable mode to the time of V_{REF} passing its rising UVLO threshold (1.89V typical), the LT8391D is going through a power-on-reset (POR), waking up the entire internal control circuitry and settling to the right initial conditions. After the POR, the LT8391D is ready and waiting for the signals on the PWM pin to start switching.

OPERATION

Start-Up and Fault Protection

Figure 8 shows the start-up and fault sequence for the LT8391D. During the POR state, the SS pin is hard pulled down with a 100Ω to ground. In a pre-biased condition, the SS pin has to be pulled below 0.2V to enter the INIT state, where the LT8391D wait 10µs so that the SS pin can be fully discharged to ground. After the 10µs, the LT8391D enters the UP/PRE state when the PWM_{ON} signal goes high.

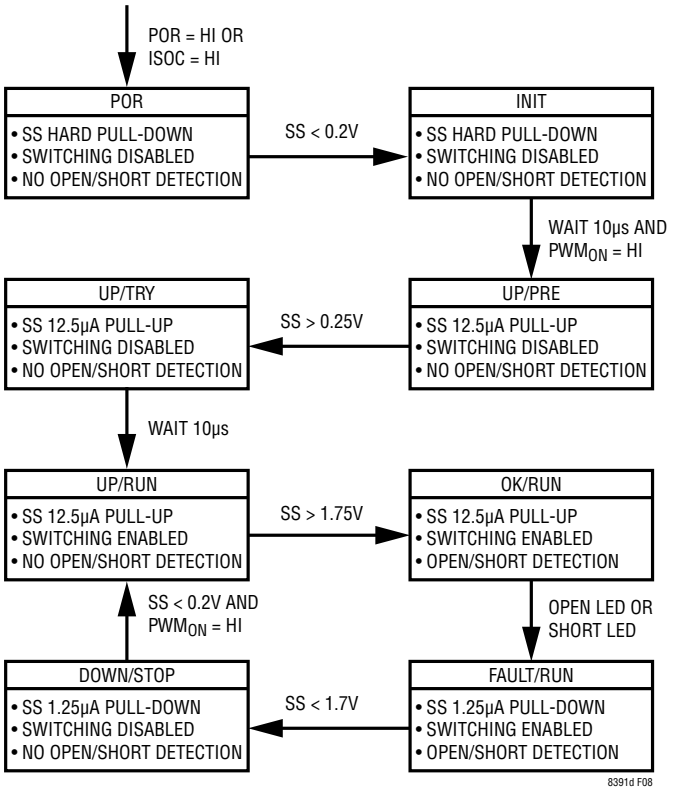


Figure 8. Start-Up and Fault Sequence

During the UP/PRE state, the SS pin is charged up by a 12.5µA pull-up current while the switching is disabled. Once the SS pin is charged above 0.25V, the LT8391D enters the UP/TRY state, where the switching is still disabled. After 10µs in the UP/TRY state, the LT8391D enters the UP/RUN state.

During the UP/RUN state, the switching is enabled and the start-up of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the SS pin voltage is less than 1V, the LT8391D regulates the FB pin voltage to the SS pin voltage instead of the 1V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to GND. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage V_{OUT} rises smoothly to its final LED string voltage.

Once the SS pin is charged above 1.75V, the LT8391D enters the OK/RUN state, where the LED fault (both open LED and short LED) detection is activated. The open LED means that V_{FB} > 0.95V, and the short LED means that V_{FB} < 0.05V. Both the open LED and short LED faults are combined to the $\overline{FAULT}$ pin. When either fault happens, the LT8391D enters the FAULT/RUN state, where a 1.25µA pull-down current slowly discharges the SS pin with the other conditions the same as the OK/RUN state. Once the SS pin is discharged below 1.7V, the LT8391D enters the DOWN/STOP state, where the switching is disabled and the LED fault detection is deactivated with the previous fault latched. Once the SS pin is discharged below 0.2V and the PWM_{ON} signal is still high, the LT8391D goes back to the UP/RUN state.

In an open or short LED condition, the LT8391D can be set to hiccup, latch-off, or keep-running fault protection mode with a resistor between the SS and V_{REF} pins. Without any resistor, the LT8391D will hiccup with SS pin between 0.2V and 1.75V and go around the UP/RUN, OK/RUN, FAULT/RUN, and DOWN/STOP states until the fault condition is cleared. With a 499k resistor, the LT8391D will latch off until the EN/UVLO is toggled. With a 100k resistor, the LT8391D will keep running regardless of the fault.

APPLICATIONS INFORMATION

The front page shows a typical LT8391D application circuit. This Applications Information section serves as a guideline of selecting external components for typical applications. The examples and equations in this section assume continuous conduction mode unless otherwise specified.

Switching Frequency Selection

The LT8391D uses a constant frequency control scheme between 150kHz and 650kHz. Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. For low power applications, consider operating at higher frequencies to minimize the total solution size.

In addition, the specific application also plays an important role in switching frequency selection. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band.

Switching Frequency Setting

The switching frequency of the LT8391D can be set by the internal oscillator. With the SPRD pin pulled to ground, the switching frequency is set by a resistor from the RT pin to ground. Table 1 shows R_T resistor values for common switching frequencies.

Table 1. Switching Frequency vs R_T Value (1% Resistor)

f_{OSC} (kHz)	R_T (k)
150	309
200	226
300	140
400	100
500	75
600	59
650	51.1

Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the LT8391D implements a triangle spread spectrum frequency modulation scheme. With the SPRD pin tied to $INTV_{CC}$, the LT8391D starts to spread its switching frequency ±15% around the internal oscillator frequency. Figure 9 and Figure 10 show the noise spectrum comparison of the front page application between spread spectrum enabled and disabled.

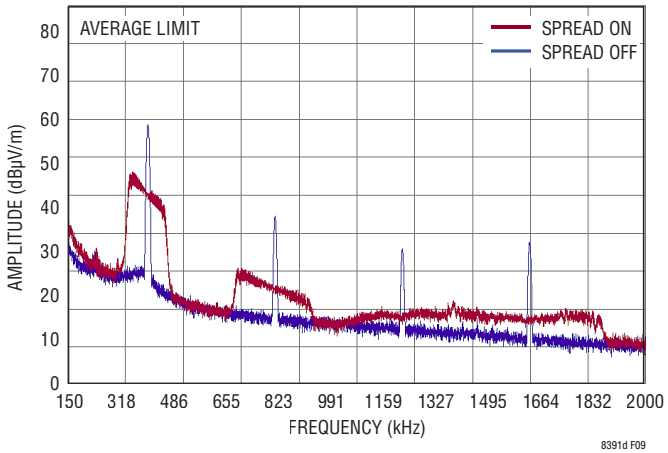


Figure 9. CISPR25 Average Conducted EMI

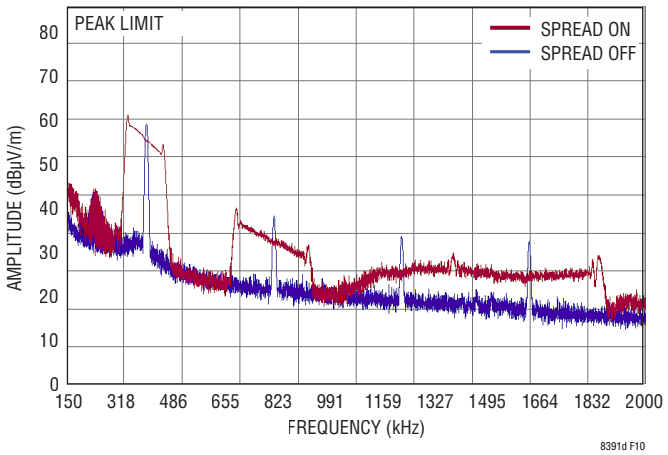


Figure 10. CISPR25 Peak Conducted EMI

Inductor Selection

The switching frequency and inductor selection are interrelated in that higher switching frequencies allow the use of smaller inductor and capacitor values. The inductor

APPLICATIONS INFORMATION

value has a direct effect on ripple current. The highest current ripple $\Delta I_L\%$ happens in the buck region at $V_{IN(MAX)}$, and the lowest current ripple $\Delta I_L\%$ happens in the boost region at $V_{IN(MIN)}$. For any given ripple allowance set by customers, the minimum inductance can be calculated as:

$$L_{BUCK} > \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{f \bullet I_{LED(MAX)} \bullet \Delta I_L\% \bullet V_{IN(MAX)}}$$

$$L_{BOOST} > \frac{V_{IN(MIN)}^{2} \bullet (V_{OUT} - V_{IN(MAX)})}{f \bullet I_{LED(MAX)} \bullet \Delta I_L\% \bullet V_{OUT}^{2}}$$

where:

f is switching frequency

$\Delta I_L\%$ is allowable inductor current ripple

$V_{IN(MIN)}$ is minimum input voltage

$V_{IN(MAX)}$ is maximum input voltage

V_{OUT} is output voltage

$I_{LED(MAX)}$ is maximum LED current

Slope compensation provides stability in constant frequency current mode control by preventing subharmonic oscillations at certain duty cycles. The minimum inductance required for stability can be calculated as:

$$L > \frac{10 \bullet V_{OUT} \bullet R_{SENSE}}{f}$$

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

R_{SENSE} Selection and Maximum Output Current

R_{SENSE} is chosen based on the required output current. The duty cycle independent maximum current sense thresholds (50mV in peak-buck and 50mV in peak-boost) set the maximum inductor peak current in buck region, buck-boost region, and boost region.

In boost region, the lowest maximum average load current happens at $V_{IN(MIN)}$ and can be calculated as:

$$I_{OUT(MAX\_BOOST)} = \left(\frac{50mV}{R_{SENSE}} - \frac{\Delta I_{L(BOOST)}}{2} \right) \bullet \frac{V_{IN(MIN)}}{V_{OUT}}$$

where $\Delta I_{L(BOOST)}$ is peak-to-peak inductor ripple current in boost region and can be calculated as:

$$\Delta I_{L(BOOST)} = \frac{V_{IN(MIN)} \bullet (V_{OUT} - V_{IN(MIN)})}{f \bullet L \bullet V_{OUT}}$$

In buck region, the lowest maximum average load current happens at $V_{IN(MAX)}$ and can be calculated as:

$$I_{OUT(MAX\_BUCK)} = \left(\frac{50mV}{R_{SENSE}} - \frac{\Delta I_{L(BUCK)}}{2} \right)$$

where $\Delta I_{L(BUCK)}$ is peak-to-peak inductor ripple current in buck region and can be calculated as:

$$\Delta I_{L(BUCK)} = \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{f \bullet L \bullet V_{IN(MAX)}}$$

The maximum current sense R_{SENSE} in boost region is:

$$R_{SENSE(BOOST)} = \frac{2 \bullet 50mV \bullet V_{IN(MIN)}}{2 \bullet I_{LED(MAX)} \bullet V_{OUT} + \Delta I_{L(BOOST)} \bullet V_{IN(MIN)}}$$

The maximum current sense R_{SENSE} in buck region is

$$R_{SENSE(BUCK)} = \frac{2 \bullet 50mV}{2 \bullet I_{LED(MAX)} + \Delta I_{L(BUCK)}}$$

The final R_{SENSE} value should be lower than the calculated R_{SENSE} in both buck and boost regions. A 20% to 30% margin is usually recommended.

Power MOSFET Selection

The LT8391D requires four external N-channel power MOSFETs, two for the top switches (switches A and D shown in Figure 1) and two for the bottom switches (switches B and C shown in Figure 1). Important parameters for the power MOSFETs are the breakdown

APPLICATIONS INFORMATION

voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

Since the gate drive voltage is set by the 5V $INTV_{CC}$ supply, logic-level threshold MOSFETs must be used in LT8391D applications. Switching four MOSFETs at certain frequency, the gate charge current from $INTV_{CC}$ can be estimated as:

$$I_{INTVCC} = f \bullet (Q_{gA} + Q_{gB} + Q_{gC} + Q_{gD})$$

where:

f is the switching frequency

Q_{gA}, Q_{gB}, Q_{gC}, Q_{gD} are the total gate charges of MOSFETs A, B, C, D at 5V V_{GS}

Make sure the total required $INTV_{CC}$ current not exceeding the $INTV_{CC}$ current limit in the data sheet.

The LT8391D uses the V_{IN}/V_{OUT} ratio to transition between modes and regions. Bigger IR drop in the power path caused by improper MOSFET and inductor selection may prevent the LT8391D from smooth transition. Make sure that low $R_{DS(ON)}$ MOSFETs and low DCR inductor are used to satisfy:

$$I_{LED(MAX)} \le \frac{0.025 \bullet V_{OUT}}{R_{A,B}+R_{C,D}+R_{SENSE}+R_L}$$

where:

$R_{A,B}$ is the maximum $R_{DS(ON)}$ of MOSFETs A or B at 25°C

$R_{C,D}$ is the maximum $R_{DS(ON)}$ of MOSFETs C or D at 25°C

R_L is the maximum DCR resistor of inductor at 25°C

The $R_{DS(ON)}$ and DCR increase at higher junction temperatures and the process variation have been included in the calculation above.

In order to select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A(BOOST)} = \left(\frac{I_{LED(MAX)} \bullet V_{OUT}}{V_{IN}}\right)^2 \bullet \rho_T \bullet R_{DS(ON)}$$

where ρ_T is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically 0.4%/°C as shown in Figure 11. For a maximum junction temperature of 125°C, using a value of ρ_T = 1.5 is reasonable.

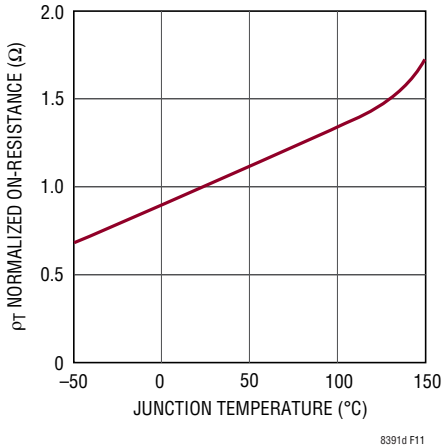


Figure 11. Normalized $R_{DS(ON)}$ vs Temperature

Switch B operates in buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B(BUCK)} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{LED(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

Switch C operates in boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C(BUCK)} = \frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}^2} \bullet I_{LED(MAX)}^2 \bullet \rho_T$$

$$\bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{LED(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

where C_{RSS} is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

APPLICATIONS INFORMATION

For switch D, the maximum power dissipation happens in boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D(BOOST)} = \frac{V_{OUT}}{V_{IN}} \bullet I_{LED(MAX)}^{2} \bullet \rho_T \bullet R_{DS(ON)}$$

For the same output voltage and current, typically switch A has the highest power dissipation in buck region at $V_{IN(MAX)}$ and switch C has the highest power dissipation in boost region at $V_{IN(MIN)}$.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

The junction-to-ambient thermal resistance $R_{TH(JA)}$ includes the junction-to-case thermal resistance $R_{TH(JC)}$ and the case-to-ambient thermal resistance $R_{TH(CA)}$. This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Optional Schottky Diode (D_B, D_D) Selection

The optional Schottky diodes D_B (in parallel with switch B) and D_D (in parallel with switch D) conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches B and D from turning on and storing charge during the dead time. In particular, D_B significantly reduces reverse recovery current between switch B turn-off and switch A turn-on, and D_D significantly reduces reverse recovery current between switch D turn-off and switch C turn-on. They improve converter efficiency and reduce switch voltage stress. In order for the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

C_{IN} and C_{OUT} Selection

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low equivalent series resistance (ESR). Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching spikes. Ceramic capacitors, of at least 1µF, should also be placed from V_{IN} to GND and V_{OUT} to GND as close to the LT8391D pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitance C_{IN}

Discontinuous input current is highest in buck region due to the switch A toggling on and off. Make sure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. In buck region, the input RMS current is given by:

$$I_{RMS} \approx I_{LED(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{LED(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

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Output Capacitance C_{OUT}

Discontinuous current shifts from the input to the output in the boost region. Make sure that the C_{OUT} capacitor network is capable of reducing the output voltage ripple. The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The maximum steady state ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{CAP(BOOST)} = \frac{I_{LED} \bullet (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \bullet V_{OUT} \bullet f}$$

$$\Delta V_{CAP(BOOST)} = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{8 \bullet L \bullet f^2 \bullet C_{OUT}}$$

The maximum steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR(BOOST)} = \frac{V_{OUT} \bullet I_{LED(MAX)}}{V_{IN(MIN)}} \bullet ESR$$

$$\Delta V_{ESR(BUCK)} = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{L \bullet f} \bullet ESR$$

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. The $INTV_{CC}$ powers internal circuitry and gate drivers in the LT8391D. The $INTV_{CC}$ regulator can supply a peak current of 145mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good local bypass is necessary to supply the high transient current required by MOSFET gate drivers.

Higher input voltage applications with large MOSFETs being driven at higher switching frequencies may cause the maximum junction temperature rating for the LT8391D to be exceeded. The system supply current is normally dominated by the gate charge current. Additional external loading of the $INTV_{CC}$ also needs to be taken into account for the power dissipation calculation. The total LT8391D power dissipation in this case is $V_{IN} \bullet I_{INTVCC}$, and overall efficiency is lowered. The junction temperature can be estimated by using the equation:

$$T_J = T_A + P_D \bullet \theta_{JA}$$

where θ_{JA} (in °C/W) is the package thermal resistance.

To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum V_{IN}.

Top Gate MOSFET Driver Supply (C_{BST1}, C_{BST2})

The top MOSFET drivers, TG1 and TG2, are driven between their respective SW and BST pin voltages. The boost voltages are biased from floating bootstrap capacitors C_{BST1} and C_{BST2}, which are normally recharged through both the external and internal bootstrap diodes when the respective top MOSFET is turned off. Both capacitors are charged to the same voltage as the $INTV_{CC}$ voltage. The bootstrap capacitors C_{BST1} and C_{BST2}, need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

Programming V_{IN} UVLO

A resistor divider from V_{IN} to the EN/UVLO pin implements V_{IN} undervoltage lockout (UVLO). The EN/UVLO enable falling threshold is set at 1.220V with 13mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage on the pin is below 1.220V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are:

$$V_{IN(UVLO+)} = 1.233V \bullet \frac{R1+R2}{R2} + 2.5\mu A \bullet R1$$

$$V_{IN(UVLO-)} = 1.220V \bullet \frac{R1+R2}{R2}$$

Figure 12 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the LT8391D in shutdown with quiescent current less than 2µA.

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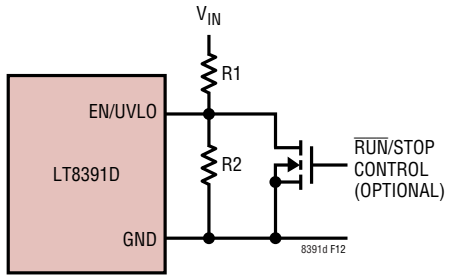

Figure 12. V_{IN} Undervoltage Lockout (UVLO)

Programming LED Current

The LED current is programmed by placing an appropriate value current sense resistor, R_{LED}, in series with the LED string. The voltage drop across R_{LED} is (Kelvin) sensed by the ISP and ISN pins. The CTRL pin should be tied to a voltage higher than 1.35V to get the full-scale 100mV (typical) threshold across the sense resistor. The CTRL pin can be used to dim the LED current to zero, although relative accuracy decreases with the decreasing sense threshold. When the CTRL pin voltage is less than 1.15V, the LED current is:

$$I_{LED} = \frac{V_{CTRL} - 250mV}{10 \bullet R_{LED}}$$

When V_{CTRL} is between 1.15V and 1.35V, the LED current varies with the V_{CTRL}, but departs from the equation above by an increasing amount as V_{CTRL} increases. Ultimately, when $V_{CTRL} > 1.35V$, the LED current no longer varies. The typical $V_{(ISP-ISN)}$ threshold vs V_{CTRL} is listed in Table 2.

Table 2. $V_{(ISP-ISN)}$ Threshold vs V_{CTRL}

V_{CTRL} (V)	$V_{(ISP-ISN)}$ (mV)
1.15	90
1.20	94.5
1.25	98
1.30	99.5
1.35	100

When V_{CTRL} is higher than 1.35V, the LED current is regulated to:

$$I_{LED} = \frac{100mV}{R_{LED}}$$

The CTRL pin should not be left open (tie to V_{REF} if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the LED load, or with a resistor divider to V_{IN} to reduce output power and switching current when V_{IN} is low. The presence of a time varying differential voltage ripple signal across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by higher LED load current, lower switching frequency, or smaller value output filter capacitor. Some level of ripple signal is acceptable, and the compensation capacitor on the V_C pin filters the signal so the average difference between ISP and ISN is regulated to the user-programmed value. The ripple voltage amplitude (peak-to-peak) in excess of 20mV should not cause mis-operation, but may lead to noticeable offset between the average value and the user-programmed value.

Dimming Control

There are two methods to control the LED current for dimming using the LT8391D. One method uses the CTRL pin to adjust the current regulated in the LEDs. A second method uses the PWM pin to modulate the LED current between zero and full current to achieve a precisely programmed average current.

Compared to the analog dimming method, the PWM dimming method offers much higher dimming ratio without any color shift. To make PWM dimming more accurate, the switch demand current is stored on the V_C node when the PWM signal is low. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time, a low side NMOS PWM switch should be used in the LED current path to prevent the output capacitor from discharging during the PWM signal low phase.

The choice of switching frequency, inductor value, and loop compensation affects the minimum PWM on time, below which the LT8391D loses the LED current regulation. For the same application, the LT8391D achieves the highest PWM dimming ratio in buck region, the medium PWM dimming ratio in buck-boost region, and the lowest PWM dimming ratio in boost region.

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In either fixed frequency operation set by R_T resistor or spread spectrum frequency operation, the internal oscillator is synchronized to the PWM signal rising edge, thereby providing flicker-free PWM dimming performance.

Programming Output Voltage and Thresholds

The LT8391D has a voltage feedback pin FB that can be used to program a constant-voltage output. The output voltage can be set by selecting the values of R3 and R4 (Figure 13) according to the following equation:

$$V_{OUT} = 1.00V \bullet \frac{R3 + R4}{R4}$$

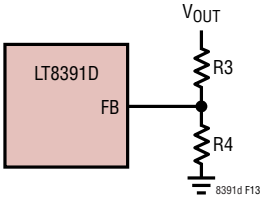

Figure 13. Feedback Resistor Connection

In addition, the FB pin also sets output overvoltage threshold, open LED threshold, and short LED threshold. For an LED driver application with small output capacitors, the output voltage usually overshoots a lot during an open LED event. Although the 1.00V FB regulation loop tries to regulate the output, the loop is usually too slow to prevent the output from overshooting. Once the FB pin hits its overvoltage threshold 1.05V, the LT8391D stops switching by turning off TG1, BG1, TG2, and BG2. The output overvoltage threshold can be set as:

$$V_{OUT(OVP)} = 1.05V \bullet \frac{R3 + R4}{R4}$$

Make sure the expected V_{FB} during normal operation stays between the short LED rising threshold 0.1V and the open LED falling threshold 0.9V:

$$0.1V \le V_{LED} \bullet \frac{R4}{R3 + R4} \le 0.9V$$

These equations set the maximum LED string voltage with full open LED protection.

$\overline{\text{FAULT}}$ Pin

The LT8391D provides an open-drain status pin, $\overline{\text{FAULT}}$, which is pulled low during either open LED or short LED conditions. The open LED condition happens when the FB pin is above 0.95V. The short LED condition happens when the FB pin is below 0.05V. The $\overline{\text{FAULT}}$ status is updated when the SS pin is above 1.75V and the PWM signal is high.

Soft-Start and Fault Protection

As shown in Figure 8 and explained in the Operation section, the SS pin can be used to program soft-start by connecting an external capacitor from the SS pin to ground. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage rises smoothly and transitions into LED current regulation. The soft-start range is defined to be the voltage range from 0V to the FB voltage in LED current regulation. The soft-start time can be calculated as:

$$t_{SS} = V_{LED} \bullet \frac{R4}{R3 + R4} \bullet \frac{C_{SS}}{12.5\mu A}$$

Make sure the C_{SS} is at least five to ten times larger than the compensation capacitor on the V_C pin. A 22nF ceramic capacitor is a good starting point.

The SS pin is also used as a fault timer. Once an open LED or a short LED fault is detected, a 1.25µA pull-down current source is activated. Using a single resistor from the SS pin to the V_{REF} pin, the LT8391D can be set to three different fault protection modes: hiccup (no resistor), latch-off (499k), and keep-running (100k).

With a 100k resistor in keep-running mode, the LT8391D continues switching normally, either regulating the programmed V_{OUT} during open LED fault or regulating the current during short LED fault. With a 499k resistor in latch-off mode, the LT8391D stops switching until the EN/UVLO pin is pulled low and high to restart. With no resistor in hiccup mode, the LT8391D enters low duty cycle auto-retry operation. The 1.25µA pull-down current discharges the SS pin to 0.2V and then 12.5µA pull-up

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current charges the SS pin up. If the fault condition has not been removed when the SS pin reaches 1.75V, the 1.25µA pull-down current turns on again, initiating a new hiccup cycle. This will continue until the fault is removed.

Loop Compensation

The LT8391D uses an internal transconductance error amplifier, the output of which, V_C, compensates the control loop. The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability.

The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor on the V_C pin are set to optimize control loop response and stability. For a typical LED application, a 10nF compensation capacitor on the V_C pin is adequate, and a series resistor should always be used to increase the slew rate on the V_C pin to maintain tighter regulation of LED current during fast transients on the input supply of the converter.

Efficiency Considerations

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most of the losses in LT8391D circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
2. Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors.
3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents.
4. C_{IN} and C_{OUT} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck region. The output capacitor has the difficult job of filtering the large RMS output current in boost region. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
5. Other losses. Schottky diode D_B and D_D are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads. Switch A causes reverse recovery current loss in buck region, and switch C causes reverse recovery current loss in boost region.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in the input current, then there is no change in efficiency.

PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

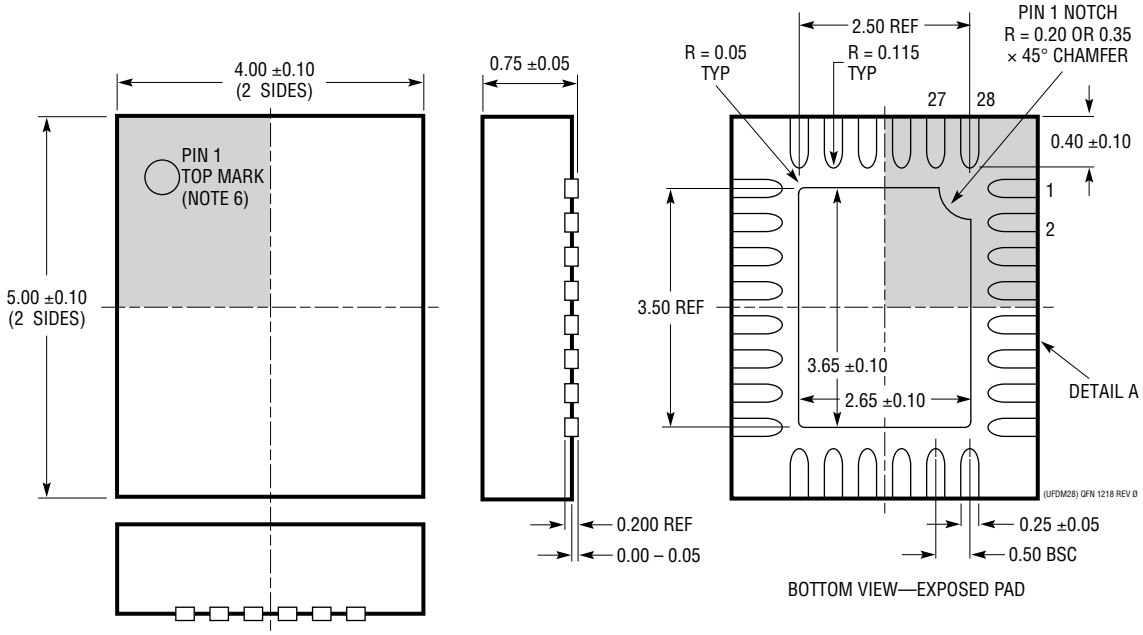
- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, switch A, switch B and D_B in one compact area. Place C_{OUT}, switch C, switch D and D_D in one compact area.
- Use immediate vias to connect the components to the ground plane. Use several large vias for each power component.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.

APPLICATIONS INFORMATION

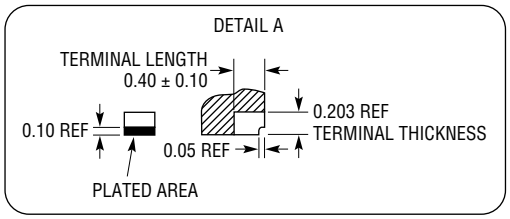
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or GND).
- Separate the signal and power grounds. All small-signal components should return to the exposed GND pad from the bottom, which is then tied to the power GND close to the sources of switch B and switch C.
- Place switch A and switch C as close to the controller as possible, keeping the power GND, BG and SW traces short.
- Keep the high d_V/d_T SW1, SW2, BST1, BST2, TG1 and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B, D_B and the C_{IN} capacitor should have short leads and PCB trace lengths. The path formed by switch C, switch D, D_D and the C_{OUT} capacitor also should have short leads and PCB trace lengths.
- The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.
- Connect the top driver bootstrap capacitor C_{BST1} closely to the BST1 and SW1 pins. Connect the top driver bootstrap capacitor C_{BST2} closely to the BST2 and SW2 pins.
- Connect the input capacitors C_{IN} and output capacitors C_{OUT} closely to the power MOSFETs. These capacitors carry the MOSFET AC current.
- Route LSP and LSN traces together with minimum PCB trace spacing. Avoid sense lines pass through noisy areas, such as switch nodes. The filter capacitor between LSP and LSN should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{SENSE} resistor. A low ESL sense resistor is recommended.
- Connect the V_C pin compensation network close to the IC, between V_C and the signal ground. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ bypass capacitor, C_{INTVCC}, close to the IC, between the $INTV_{CC}$ and the power ground. This capacitor carries the MOSFET drivers' current peaks.

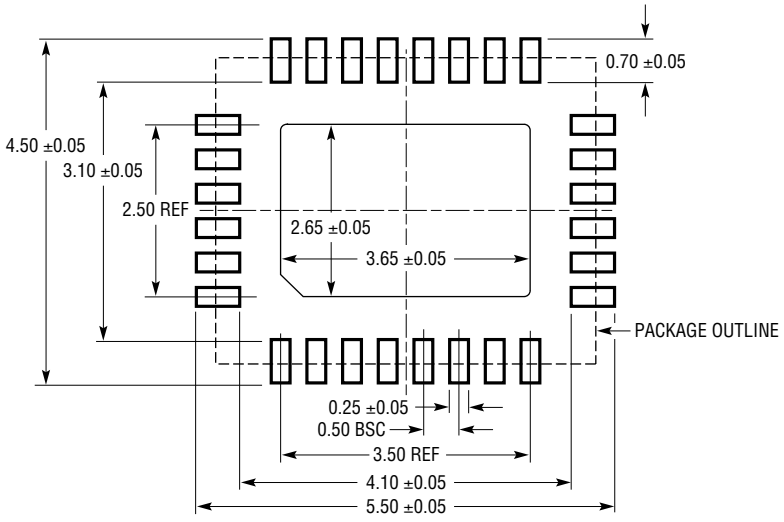
PACKAGE DESCRIPTION

UFDM Package
28-Lead Plastic Side Wettable QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1682 Rev Ø)



NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

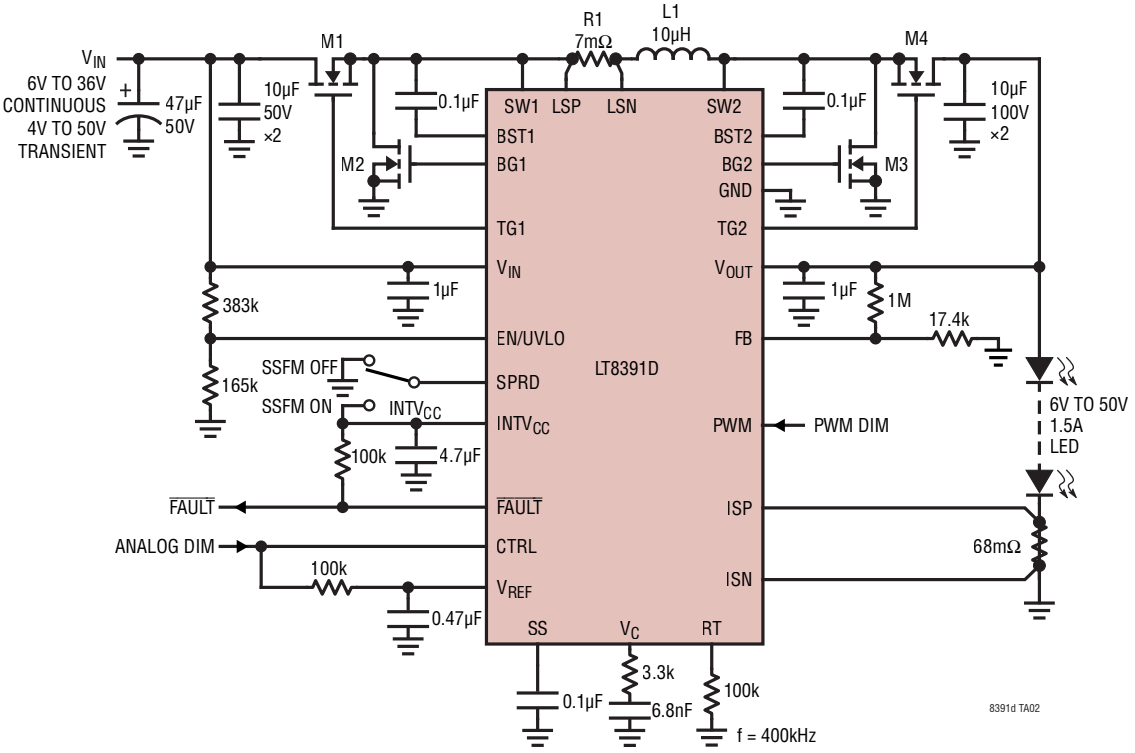




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

TYPICAL APPLICATION

97% Efficient 75W (50V, 1.5A) Buck-Boost LED Driver with Fault Protection



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8391/LT8391A	60V, 2MHz Synchronous 4-Switch Buck-Boost LED Controller with Spread Spectrum	V_{IN}: 4V to 60V, V_{OUT}: 0V to 60V, ±3% Current Accuracy, Internal and External PWM Dimming, TSSOP-28 and 4mm × 5mm QFN-28
LT8390/LT8390A	High Efficiency, 2MHz, Synchronous, 4-Switch Buck-Boost Controller	V_{IN}: 4V to 60V, V_{OUT}: 1V to 60V, I_{SD} = <1µA, TSSOP-28E and 4mm × 5mm QFN-28
LT3791	60V, 700kHz 4-Switch Synchronous Buck-Boost LED Controller	V_{IN}: 4.7V to 60V, V_{OUT}: 0V to 60V, ±6% Current Accuracy, TSSOP-38
LT3922	36V, 2A, 2MHz Synchronous Step Up LED Driver with Internal 128:1 PWM Dimming	V_{IN}: 2.8V to 36V, V_{OUT}: 4V to 34V, I_{SD} = 1µA, Internal 128:1 PWM Dimming, Ext 5000:1, 4mm × 5mm QFN-28
LT3755/LT3755-1/ LT3755-2	40V_{IN}, 75V_{OUT}, 1MHz Non-Synchronous Boost LED Controller	V_{IN}: 4.5V to 40V, V_{OUT}: V_{IN} to 75V, ±4% Current Accuracy, 3mm × 3mm QFN-16 and MSE-16
LT3761	60V_{IN}, 80V_{OUT}, 1MHz Non-Synchronous Boost LED Controller with Internal PWM Generator	V_{IN}: 4.5V to 60V, V_{OUT}: V_{IN} to 80V, ±3% Current Accuracy, External and Internal PWM dimming, MSE-16
LT3795	110V, 1MHz Non-Synchronous Boost LED Controller with Spread Spectrum Frequency Modulation	V_{IN}: 4.5V to 110V, V_{OUT}: V_{IN} to 110V, ±3% Current Accuracy, Internal Spread Spectrum, TSSOP-28