BVA304C

DIGITAL VARIABLE GAIN AMPLIFIER

50MHz - 4000MHz

Device Features

- Integrate DSA to Amp Functionality
- 50-4000MHz Broadband Performance
- 14.8dB Gain @1.9GHz
- 3.1dB Noise Figure at max gain setting @ 1.9GHz
- 19.0dBm P1dB @ 1.9GHz
- 32.2dBm OIP3 @ 1.9GHz
- No matching circuit needed
- Attenuation: 0.5 dB steps up to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- High attenuation accuracy (DSA to Amp)
  ±(0.25 + 3.5% x Atten) @ 1.9 GHz
- Wide Power supply range of +2.7 to +5.5V(DSA)
  Single Fixed +3.3V supply (Amp)
- 1.8V control logic compatible
- Programming modes
  - Direct Parallel
  - Latched Parallel
  - Serial
- Unique power-up state selection
- Lead-free/RoHS2-compliant 24-lead 4mm x 4mm x 0.9mm QFN SMT package

24-lead 4mm x 4mm x 0.9mm QFN

Figure 1. Package Type

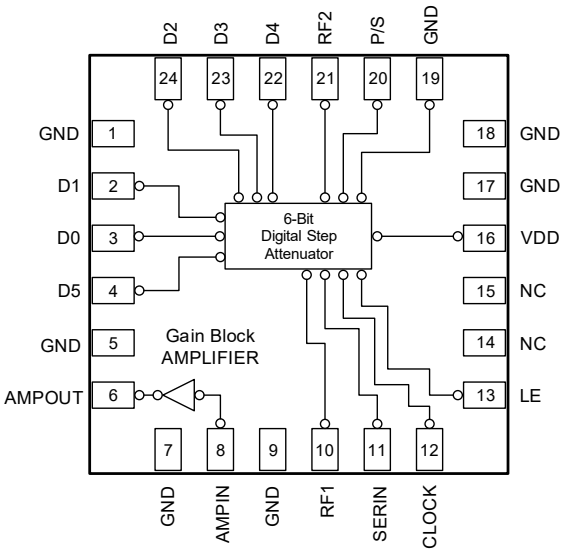


Figure 2. Functional Block Diagram

Product Description

The BVA304C is a digitally controlled variable gain amplifier (DVGA) is featuring high linearity using the voltage 3.3V supply with a broad-band frequency range of 50MHz to 4000MHz.

The BVA304C integrates a high performance digital step attenuator and a high linearity, broadband gain block amplifier using the small package(4mmx4mm QFN package) and operating voltage 3.3V DC. The BVA304C is designed for use in 3G/4G/5G wireless infrastructure and other high performance RF applications.

Both DSA and gain block amplifier in BVA304C are internally matched to 50 Ohms and it is easy to use with no external matching compo-nents required.

The BVA304C always initialize to the maximum attenuation setting on power-up for both Serial and Parallel mode until next programming word is inputted.

The BVA304C is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless applications.

Application

- 3G/4G/5G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

Table 1. Electrical Specifications[1]

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			50		4000	MHz
Gain[2]		Attenuation = 0dB @ 1900MHz		14.8		dB
Attenuation Control range		0.5dB Step		0 - 31.5		dB
Attenuation Step				0.5		dB
Attenuation Accuracy	0.05GHz - 1GHz	Any bit or bit combination			±(0.25 + 2.5% of Attenuation setting)	dB
	1GHz - 2GHz				±(0.25 + 3.5% of Attenuation setting)	
	2GHz - 3GHz				±(0.25 + 4% of Attenuation setting)	
	3GHz - 4GHz				±(0.25 + 4% of Attenuation setting)	
Input Return loss	0.05GHz - 1.7GHz	Attenuation = 0dB		13		dB
	1.7GHz - 4GHz			10		
Output Return loss	0.05GHz - 1.7GHz			18		
	1.7GHz - 4GHz			15		
Output Power for 1dB Compression		Attenuation = 0dB @ 1900MHz		19.0		dBm
Output Third Order Intercept Point[3]		Attenuation = 0dB @ 1900MHz Output power = –3dBm/ tone separated by 1MHz		32.2		dBm
Noise Figure		Attenuation = 0dB @ 1900MHz		3.1		dB
Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Supply voltage		DSA	2.7		5.5	V
		AMP		3.3		V
Supply Current		DSA + AMP	20	26	30	mA
Control Interface		Serial / parallel mode		6		Bit
Control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.6	V
Maximum Spurious level[4]		Measured @ DSA RF1, RF2 ports		< -145		dBm/Hz
Impedance				50		Ω

1. Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+3.3V, measure on Evaluation Board (DSA to AMP)
2. Gain data has PCB & Connectors insertion loss de-embedded
3. OIP3 _ measured with two tones at an output of –3dBm per tone separated by 1MHz.
4. The unwanted spurious can be occurred due to built-in negative voltage generator. Typical generated fundamental frequency is around 6MHz.

Table 2. Typical RF Performance[1]

Parameter	Frequency						Unit
	70[2]	900[3]	1900[4]	2140[4]	2650[4]	3500[4]	MHz
Gain[5]	24.0	19.4	14.8	13.8	12.0	9.0	dB
S11	-17.2	-9.1	-9.6	-9.4	-9.0	-7.8	dB
S22	-12.4	-20.1	-21.0	-24.8	-18.8	-12.3	dB
OIP3[6]	30.0	29.6	32.2	31.7	31.6	30.6	dBm
P1dB	20.3	20.1	19.0	19.0	18.7	18.8	dBm
Noise Figure	2.8	2.9	3.1	3.3	3.5	4.0	dB

1. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+3.3V, 50 Ω system. measure on Evaluation Board. (DSA to AMP)
2. 70MHz measured with application circuit refer to table 13.
3. 900MHz measured with application circuit refer to table 15.
4. 1900MHz,2140MHz,2650MHz, 3500MHz measured with application circuit refer to table 17.
5. Gain data has PCB & Connectors insertion loss de-embedded.
6. OIP3 measured with two tones at an output of –3dBm per tone separated by 1MHz.

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage (VDD)	Amp/DSA			5.0 / 5.5	V
Supply Current	Amp		110		mA
Digital input voltage		-0.3		3.6	V
Maximum input power	Amp/DSA			+24 / +30	dBm
Storage Temperature		-55		150	℃
Junction Temperature			220		℃

Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	Amp + DSA	50		4000	MHz
Supply Voltage	Amp		3.3		V
	DSA	2.7		5.5	V
Operating Temperature	Amp + DSA	-40		105	℃

Specifications are not guaranteed over all recommended operating conditions.

Figure 3. Pin Configuration (Top View)

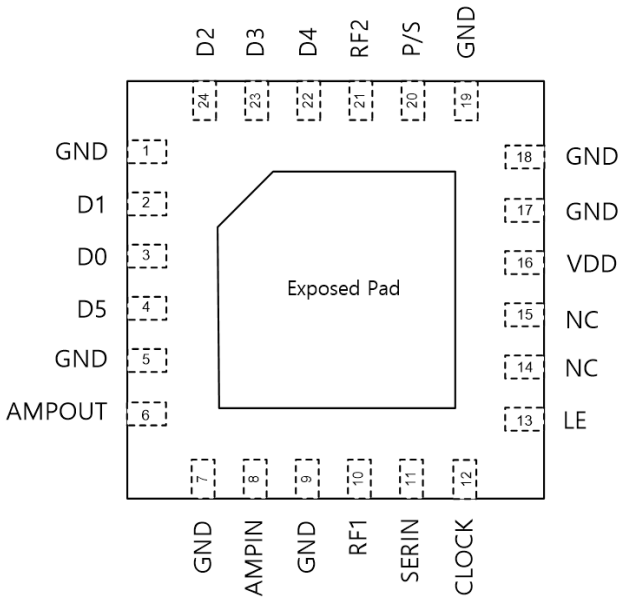


Table 5. Pin Description

Pin	Pin name	Description
1,5,7,9,17,18,19	GND	Ground, These pins must be connected to ground
2	D1	Parallel Control Voltage Inputs, Attenuation control bit 1dB
3	D0	Parallel Control Voltage Inputs, Attenuation control bit 0.5dB
4	D5	Parallel Control Voltage Inputs, Attenuation control bit 16dB
6	AMPOUT	RF Gain block Amplifier output Port. DC block Capacitor is needed.
8	AMPIN	RF Gain block Amplifier input Port. DC block Capacitor is needed.
10	RF1[1]	RF1 port (Digital Step Attenuator RF Input) This pin can also be used as an output because the design is bidirectional. RF1 is DC-coupled and matched to 50 Ω
11	SERIN	Serial interface data input
12	CLOCK	Serial interface clock input
13	LE	Latch Enable input
14,15	NC	Not connected, These pin s are recommended to connect to ground.
16	VDD	DSA Power Supply (nominal 3.3V)
20	P/S	Parallel/Serial Mode Select. For parallel mode operation, set this pin to LOW. For serial mode operation, set this pin to HIGH.
21	RF2[1]	RF2 port (Attenuator RF Output.) This pin can also be used as an input because the design is bidirectional. RF2 is DC-coupled and matched to 50 Ω.
22	D4	Parallel Control Voltage Inputs, Attenuation control bit 8dB
23	D3	Parallel Control Voltage Inputs, Attenuation control bit 4dB
24	D2	Parallel Control Voltage Inputs, Attenuation control bit 2dB
EXPOSE PAD	GND	Exposed pad : The exposed pad must be connected to ground for proper operation

Note: 1. RF1,2 pins 10 and 21 must be at 0V DC. The RF1,2 pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met.

Programming Options

BVA304C can be programmed using either the parallel or serial interface, which is selectable via P/S pin(Pin20).
Serial mode is selected by pulling it to a voltage logic HIGH and parallel mode is selected by setting P/S to logic LOW

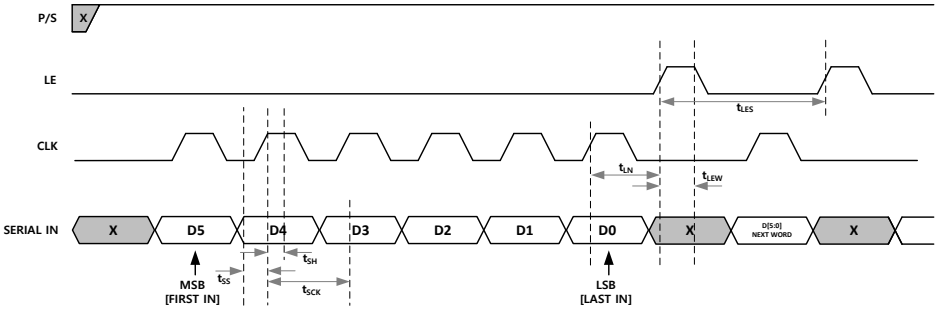
Serial Control Mode

The serial interface is a 6 bit shift register to shift in the data MSB (D5) first. When serial programming is used, all the parallel control input pins (2,3,4,22,23,24) should be grounded.
It is controlled by three CMOS-compatible signals: SERIN, Clock, and Latch Enable (LE).

Table 6. 6-Bit Serial Word Sequence

D5	Attenuation 16dB Control Bit
D4	Attenuation 8dB Control Bit
D3	Attenuation 4dB Control Bit
D2	Attenuation 2dB Control Bit
D1	Attenuation 1dB Control Bit
D0	Attenuation 0.5dB Control Bit

Figure 4. Serial Mode Timing Diagram



The BVA304C has a 3-wire serial peripheral interface (SPI): serial data input (Data), clock (CLK), and latch enable (LE). The serial control interface is activated when P/S is set to HIGH.
In serial mode, the 6-bit Data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled HIGH to latch the new attenuation state into the device. LE must be set to LOW to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept HIGH (see Figure 4 and Table 9).

Table 7. Mode Selection

P/S	Control Mode
LOW	Parallel
HIGH	Serial

Table 8. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{CLK}	Serial data clock frequency			10	MHz
t_{SCK}	Minimum serial period	70			ns
t_{SS}	Serial Data setup time	10			ns
t_{SH}	Serial Data hold time	10			ns
t_{LN}	LE setup time	10			ns
t_{LEW}	Minimum LE pulse width	30			ns
t_{LES}	Minimum LE pulse spacing	600			ns

Table 9. Truth Table for Serial Control Word

Digital Control Input						Attenuation
D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	(dB)
LOW	LOW	LOW	LOW	LOW	LOW	0 (Reference)
LOW	LOW	LOW	LOW	LOW	HIGH	0.5
LOW	LOW	LOW	LOW	HIGH	LOW	1
LOW	LOW	LOW	HIGH	LOW	LOW	2
LOW	LOW	HIGH	LOW	LOW	LOW	4
LOW	HIGH	LOW	LOW	LOW	LOW	8
HIGH	LOW	LOW	LOW	LOW	LOW	16
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	31.5

Parallel Control Mode

The BVA304C has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 10. The parallel control interface is activated when P/S is set to LOW. There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

The LE pin must be kept High. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 2, 3, 4, 22,23, 24]. Use direct parallel mode for the fastest settling time.

Latched Parallel Mode

The LE pin must be kept LOW when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled LOW to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled LOW to latch the change into the device until the next desired attenuation change (see Figure 5 and Table 11).

Power-UP Status

The BVA304C basically is set the maximum attenuation state when the initially powered up for all serial and parallel mode status until the next programming word is inputted.
If the BVA304C powered up in serial mode, all parallel control pins should be set to logic Low.

Figure 5. Latched Parallel Mode Timing Diagram

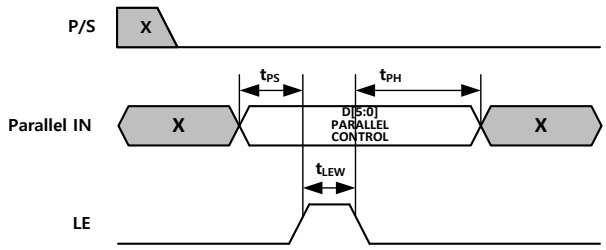


Table 10. Parallel Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_{LEW}	Minimum LE pulse width	10			ns
t_{PH}	Data hold time from LE	10			ns
t_{PS}	Data setup time to LE	10			ns

Table 11. Truth Table for the Parallel Control Word

D0	D1	D2	D3	D4	D5	P/S	LE	Attenuation State
LOW	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	Reference Loss
HIGH	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	0.5dB
LOW	HIGH	LOW	LOW	LOW	LOW	LOW	HIGH	1dB
LOW	LOW	HIGH	LOW	LOW	LOW	LOW	HIGH	2dB
LOW	LOW	LOW	HIGH	LOW	LOW	LOW	HIGH	4dB
LOW	LOW	LOW	LOW	HIGH	LOW	LOW	HIGH	8dB
LOW	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	16dB
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	31.5dB

Typical RF Performance Plot - BVA304C EVK - PCB (Application Circuit:50 ~ 500MHz)

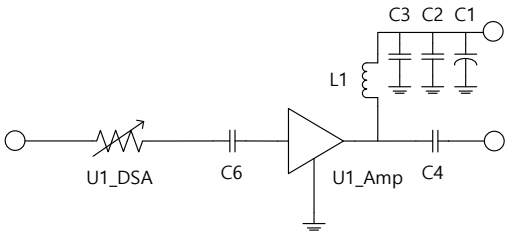
Typical Performance Data @ 25°C and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13

Table 12. Typical RF Performance(50 ~ 500MHz)

parameter	Frequency		Unit
	70	200	MHz
Gain[1]	24.0	23.7	dB
S11	-17.2	-21.2	dB
S22	-12.4	-15.1	dB
OIP3[2]	30.0	29.5	dBm
P1dB	20.3	20.4	dBm
N.F	2.8	2.9	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of -3dBm per tone separated by 1MHz.

Table 13. 50 ~ 500MHz IF Application Circuit



Application Circuit Values	Frequency band	IF Circuit
		50MHz ~ 500MHz
	C6/C4	2.2nF[1]
	L1	330nH[1]

1. This value can be changed little by little according to the frequency bond and bandwidth.

Figure 6. Gain vs. Frequency
over Temperature

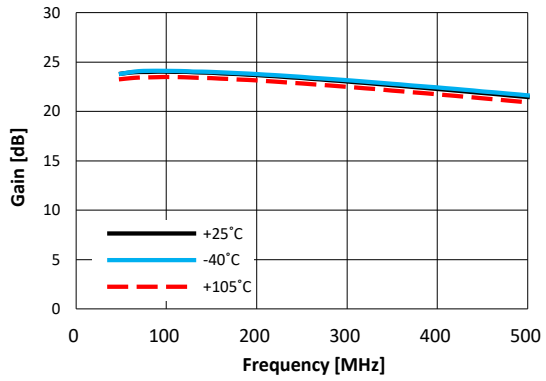


Figure 7. Gain vs. Frequency
over Major Attenuation States

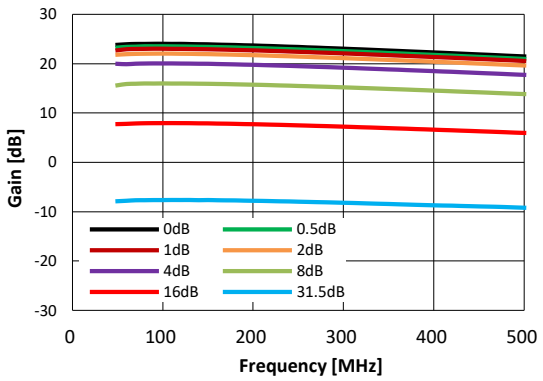


Figure 8. Input Return Loss vs. Frequency
over Major Attenuation States

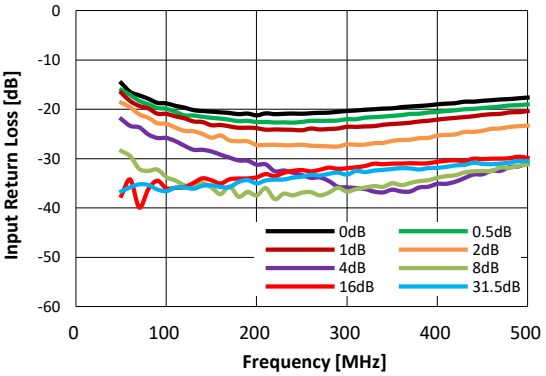
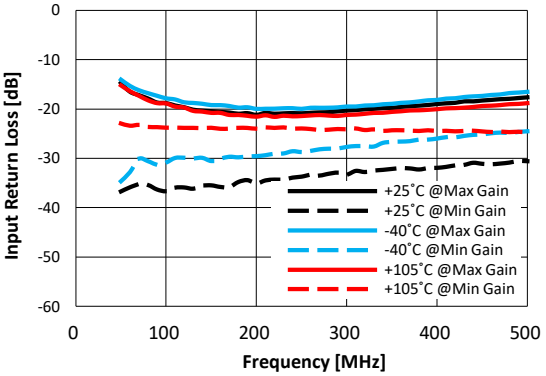


Figure 9. Input Return Loss vs. Frequency
over Temperature (Min/Max Gain State)



Typical RF Performance Plot - BVA304C EVK - PCB (Application Circuit:50 ~ 500MHz)

Typical Performance Data @ 25°C and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13

Figure 10. Output Return Loss vs. Frequency
over Major Attenuation States

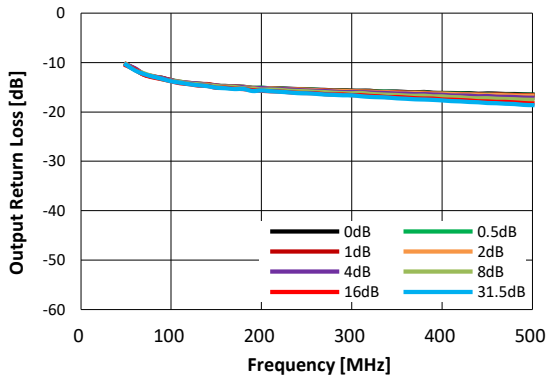


Figure 11. Output Return Loss vs. Frequency
over Temperature (Min/Max Gain State)

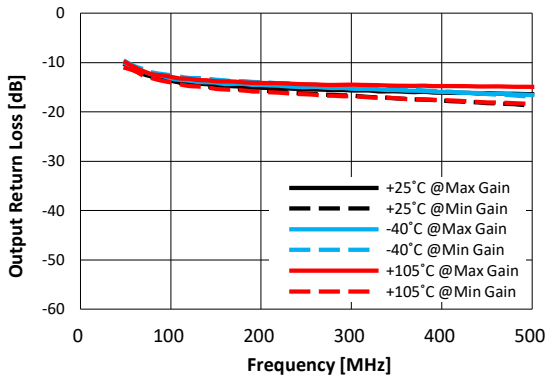


Figure 12. OIP3 vs. Frequency
Over Temperature (Max Gain State)

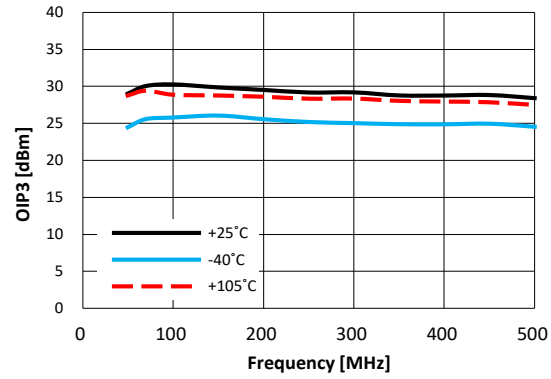


Figure 13. OIP3 vs. Frequency
Over Temperature (15.5dB Attenuation State)

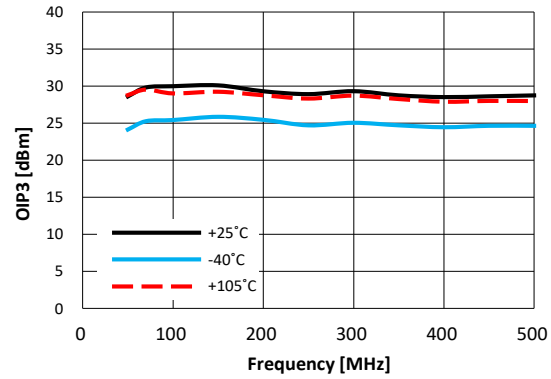


Figure 14. P1dB vs. Frequency
Over Temperature (Max Gain State)

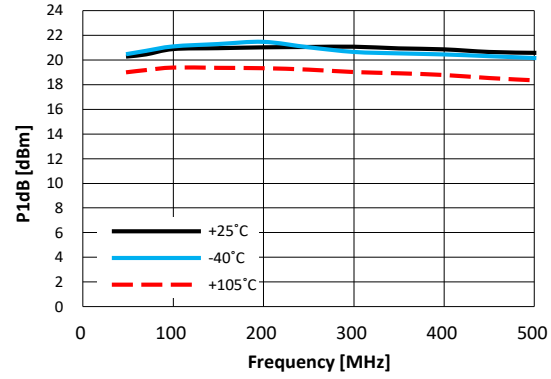
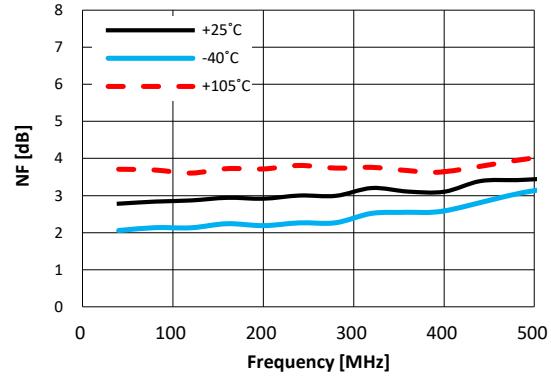


Figure 15. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA304C EVK - PCB (Application Circuit:50 ~ 500MHz)

Typical Performance Data @ 25°C and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13

Figure 16. Attenuation Error vs Frequency
over Major Attenuation Steps

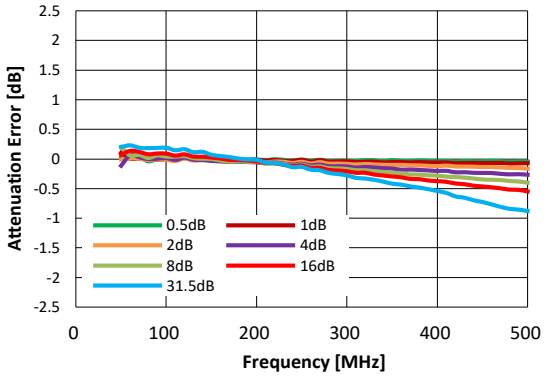


Figure 17. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

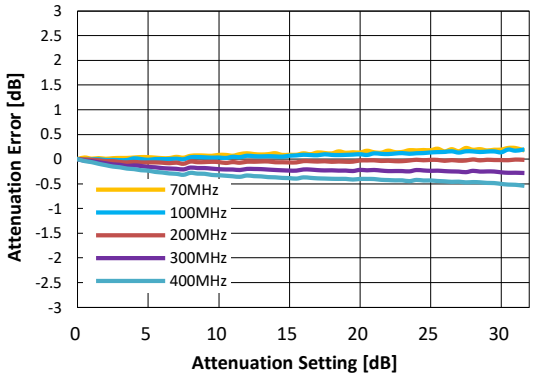


Figure 18. 0.5dB Step Attenuation vs Attenuation Setting
over Major Frequency

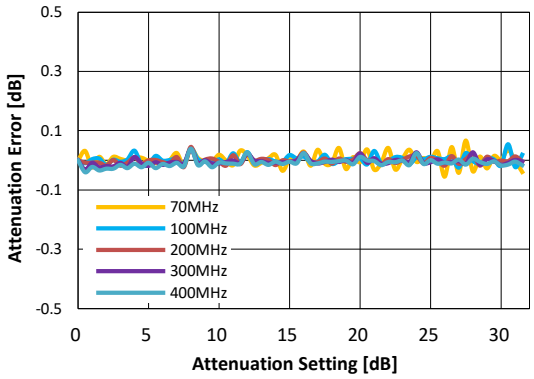


Figure 19. Attenuation Error at 70MHz vs Temperature
Over All Attenuation States

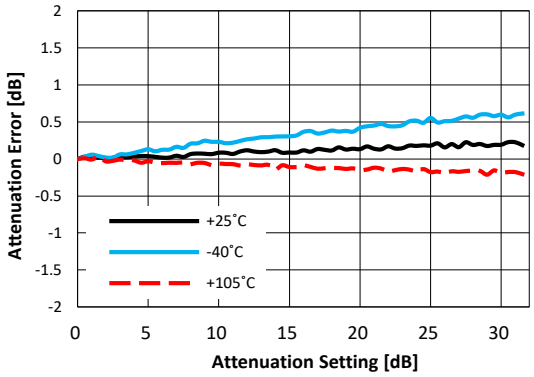
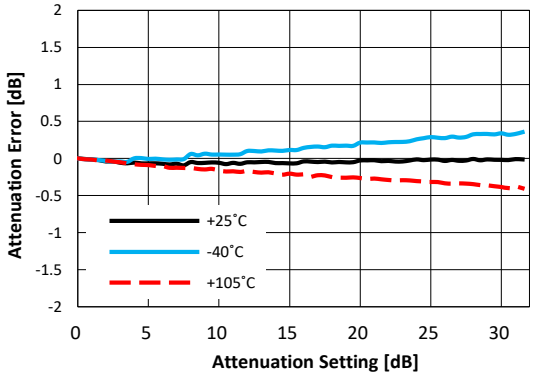


Figure 20. Attenuation Error at 200MHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA304C EVK - PCB (Application Circuit:500 ~ 1700MHz)

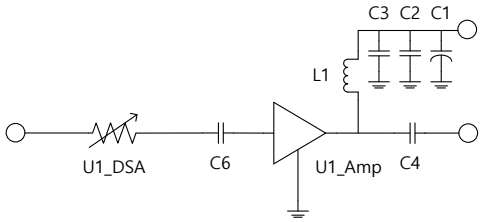
Typical Performance Data @ 25°C and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15

Table 14. Typical RF Performance(500~1700MHz)

parameter	Frequency					Unit
	700	800	900	1000	1100	MHz
Gain[1]	20.6	19.9	19.4	18.9	18.2	dB
S11	-9.0	-9.0	-9.1	-9.3	-9.5	dB
S22	-15.3	-17.9	-20.1	-23.3	-26.4	dB
OIP3[2]	28.1	29.2	29.6	29.5	29.7	dBm
P1dB	20.4	20.2	20.1	19.9	19.7	dBm
N.F	2.9	2.9	2.9	2.9	2.9	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of -3 dBm per tone separated by 1 MHz.

Table 15. 500~1700MHz RF Application Circuit



Application Circuit Values	Frequency band	RF Circuit
		500MHz ~ 1700MHz
	C6/C4	56pF[1]
	L1	22nH[1]

1. This value can be changed little by little according to the frequency bond and bandwidth.

Figure 21. Gain vs. Frequency
over Temperature (Max Gain State)

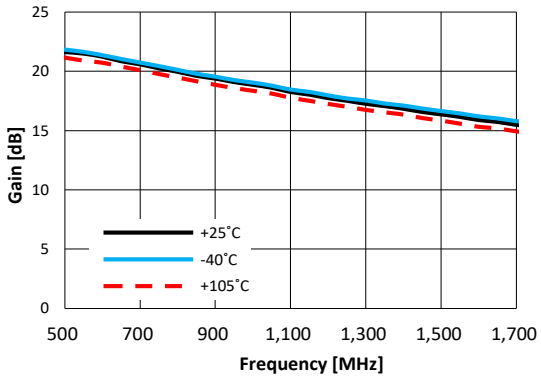


Figure 22. Gain vs. Frequency
over Major Attenuation States

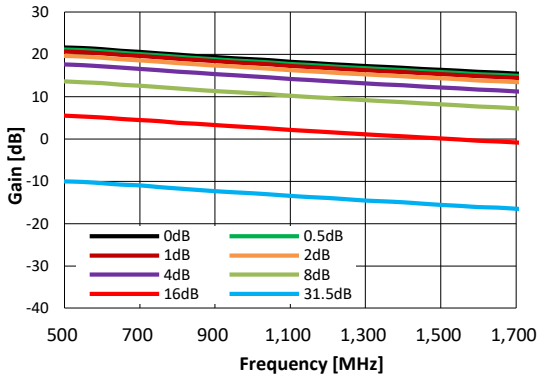


Figure 23. Input Return Loss vs. Frequency
over Major Attenuation States

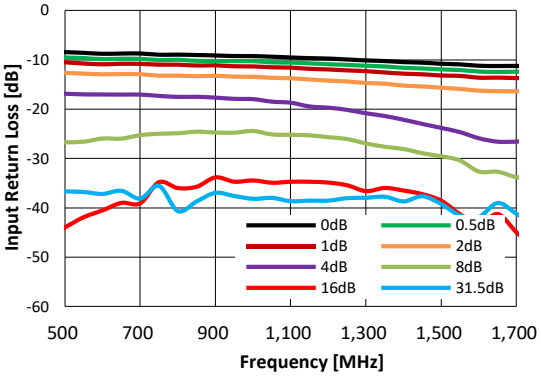
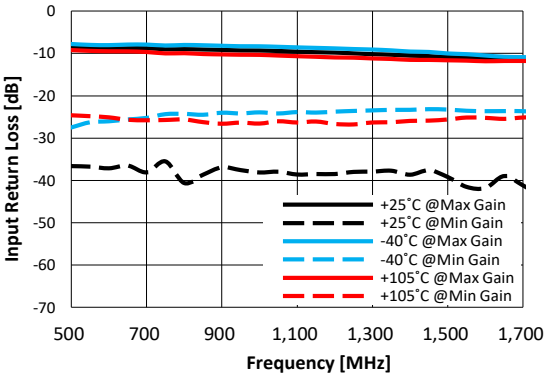


Figure 24. Input Return Loss vs. Frequency
over Temperature (Min[1]/Max Gain State)



1. Min Gain was measured in the state is set with attenuation 31.5dB.

Typical RF Performance Plot - BVA304C EVK - PCB (Application Circuit:500 ~ 1700MHz)

Typical Performance Data @ 25°C and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15

Figure 25. Output Return Loss vs. Frequency
over Major Attenuation States

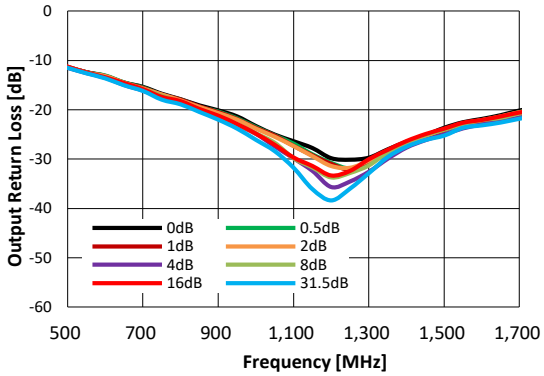


Figure 26. Output Return Loss vs. Frequency
over Temperature (Min/Max Gain State)

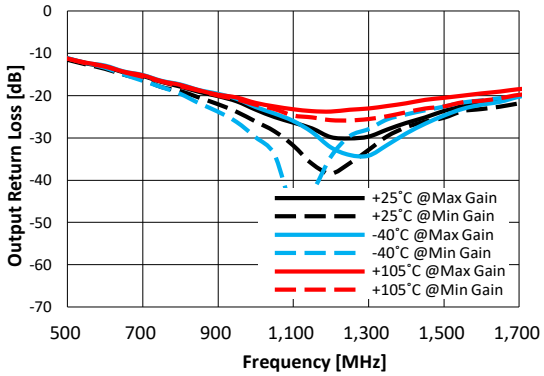


Figure 27. OIP3 vs. Frequency
Over Temperature (Max Gain State)

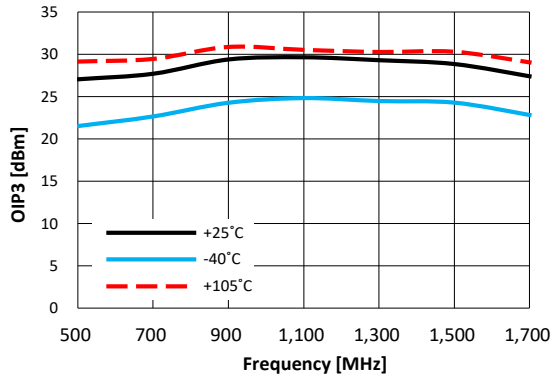


Figure 28. OIP3 vs. Frequency
Over Temperature (15.5dB Attenuation State)

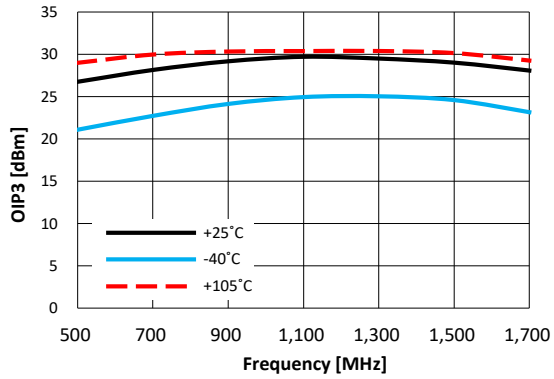


Figure 29. P1dB vs. Frequency
Over Temperature (Max Gain State)

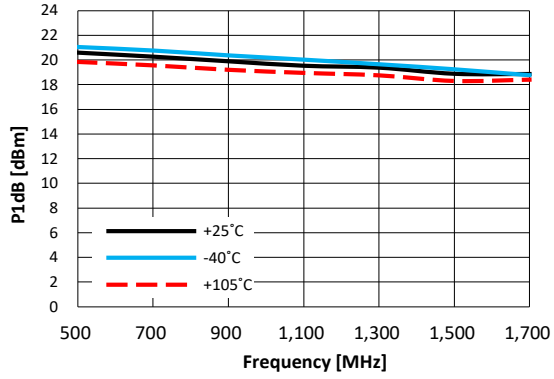
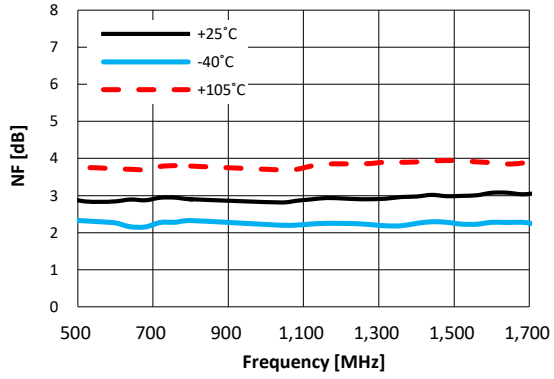


Figure 30. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA304C EVK - PCB (Application Circuit:500 ~ 1700MHz)

Typical Performance Data @ 25°C and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15

Figure 31. Attenuation Error vs Frequency
over Major Attenuation Steps

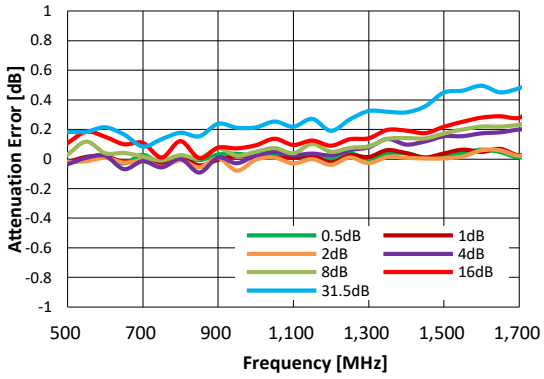


Figure 32. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

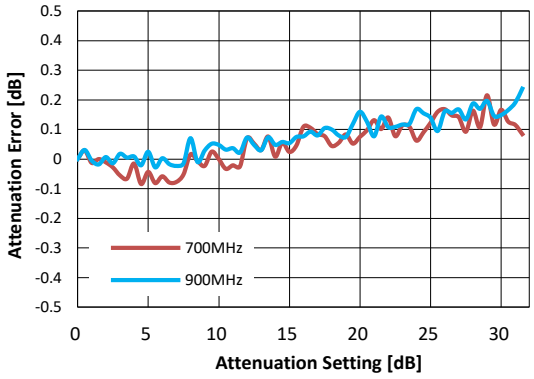


Figure 33. 0.5dB Step Attenuation vs Attenuation Setting
over Major Frequency (Max Gain State)

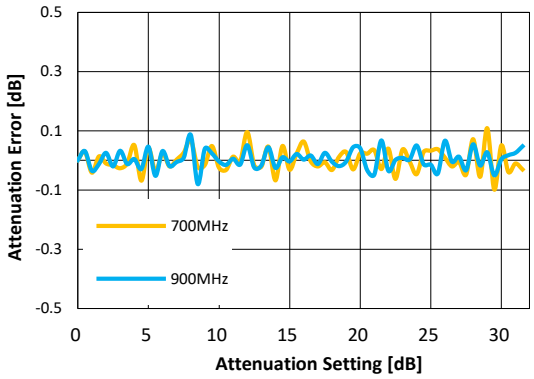
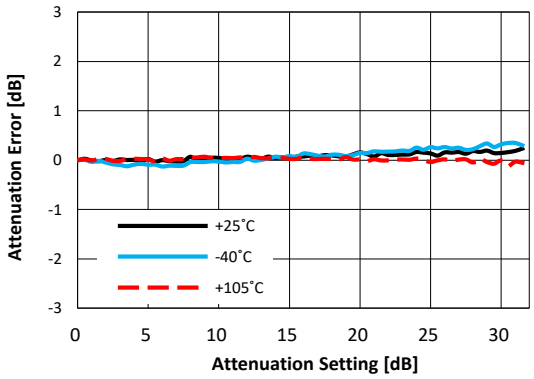


Figure 34. Attenuation Error at 900MHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA304C EVK - PCB (Application Circuit:1700 ~ 4000MHz)

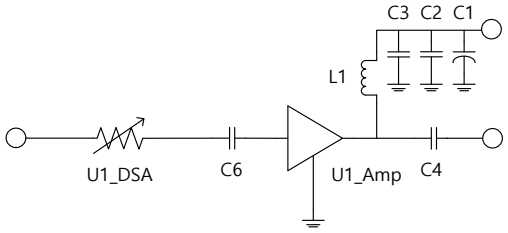
Typical Performance Data @ 25°C and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17

Table 16. Typical RF Performance(1700~4000MHz)

parameter	Frequency					Unit
	1700	1900	2140	2650	3500	MHz
Gain[1]	15.4	14.8	13.8	12.0	9.0	dB
S11	-9.1	-9.6	-9.4	-9.0	-7.8	dB
S22	-16.7	-21.0	-24.8	-18.8	-12.3	dB
OIP3[2]	30.7	32.2	31.7	31.6	30.6	dBm
P1dB	19.2	19.0	19.0	18.7	18.8	dBm
N.F	3.0	3.1	3.3	3.5	4.0	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of -3 dBm per tone separated by 1 MHz.

Table 17. 1700~4000MHz RF Application Circuit



Application Circuit Values	Frequency band	RF Circuit
		1700MHz ~ 4000MHz
	C6/C4	22pF[1]
	L1	6.2nH[1]

1. This value can be changed little by little according to the frequency bond and bandwidth.

Figure 35. Gain vs. Frequency
over Temperature (Max Gain State)

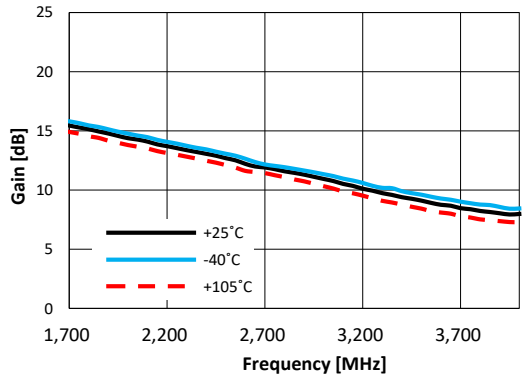


Figure 36. Gain vs. Frequency
over Major Attenuation States

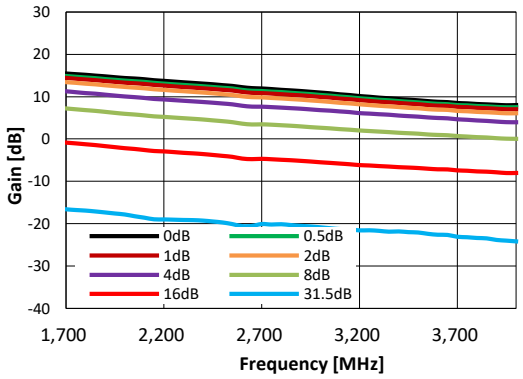


Figure 37. Input Return Loss vs. Frequency
over Major Attenuation States

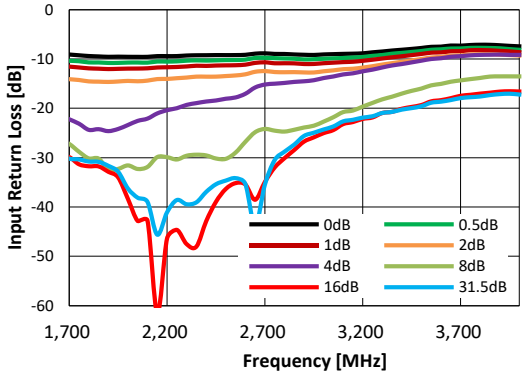
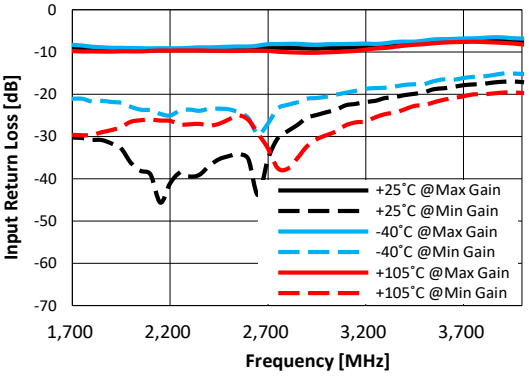


Figure 38. Input Return Loss vs. Frequency
over Temperature (Min/Max Gain State)



Typical RF Performance Plot - BVA304C EVK - PCB (Application Circuit:1700 ~ 4000MHz)

Typical Performance Data @ 25°C and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17

Figure 39. Output Return Loss vs. Frequency
over Major Attenuation States

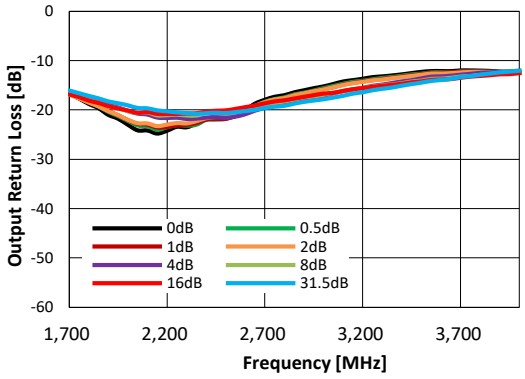


Figure 40. Output Return Loss vs. Frequency
over Temperature (Min/Max Gain State)

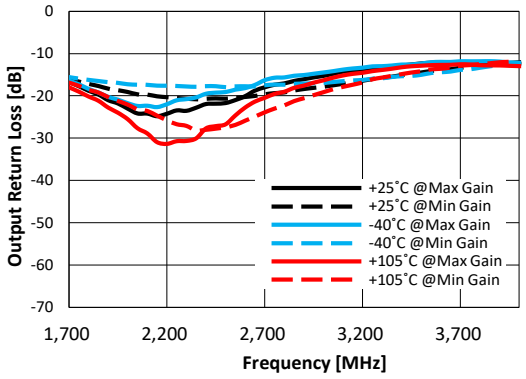


Figure 41. OIP3 vs. Frequency
Over Temperature (Max Gain State)

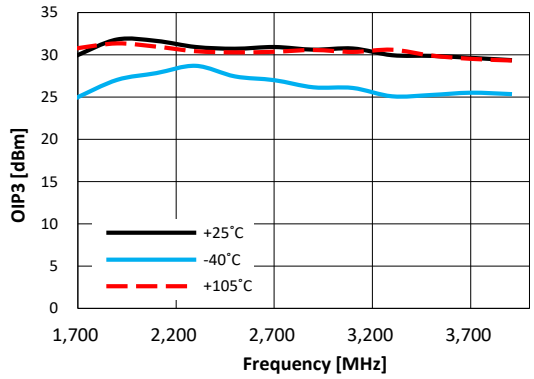


Figure 42. OIP3 vs. Frequency
Over Temperature (15.5dB Attenuation State)

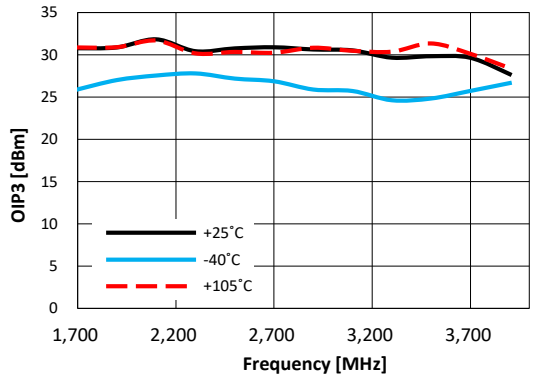


Figure 43. P1dB vs. Frequency
Over Temperature (Max Gain State)

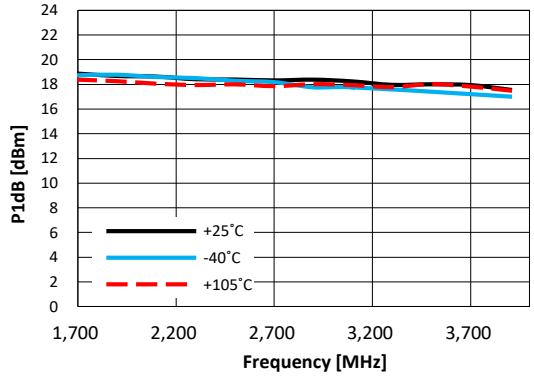
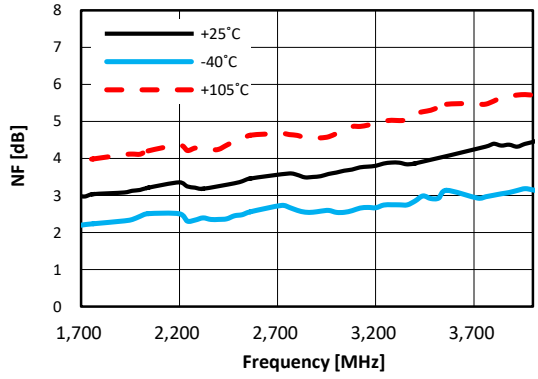


Figure 44. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA304C EVK - PCB (Application Circuit:1700 ~ 4000MHz)

Typical Performance Data @ 25°C and VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17

Figure 45. Attenuation Error vs Frequency
over Major Attenuation Steps

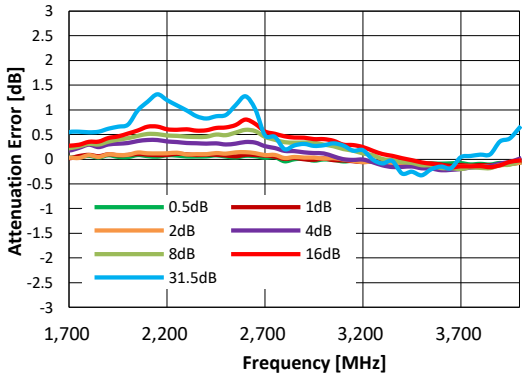


Figure 46. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

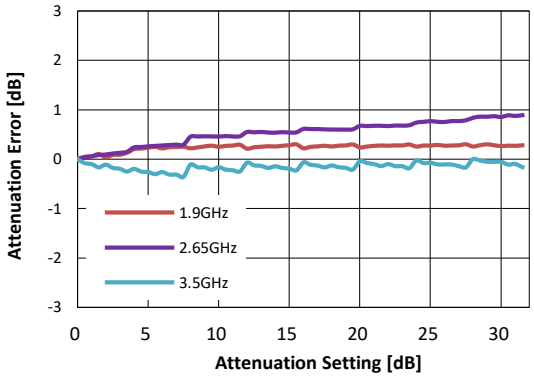


Figure 47. 0.5dB Step Attenuation vs Attenuation Setting
over Major Frequency (Max Gain State)

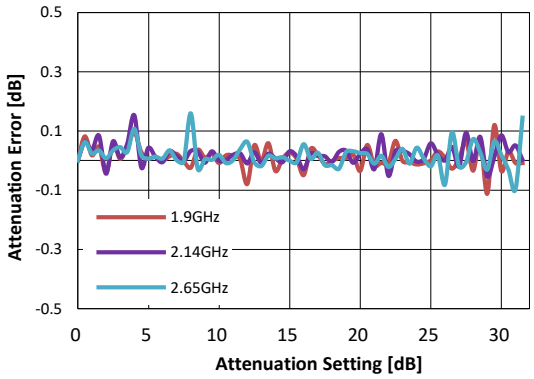


Figure 48. Attenuation Error at 1.9GHz vs Temperature
Over All Attenuation States

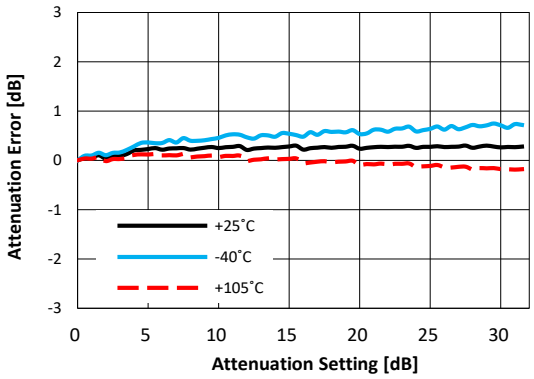


Figure 49. Attenuation Error at 2.65GHz vs Temperature
Over All Attenuation States

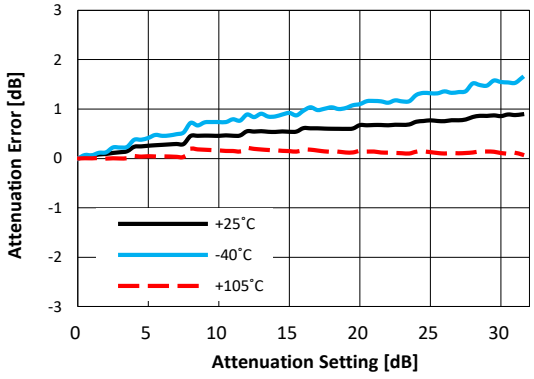


Figure 50. Attenuation Error at 3.5GHz vs Temperature
Over All Attenuation States

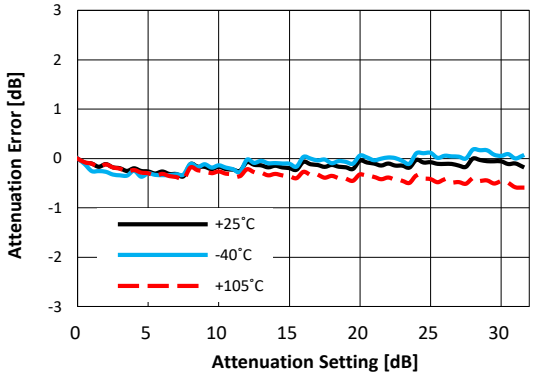


Figure 51. Evaluation Board Schematic

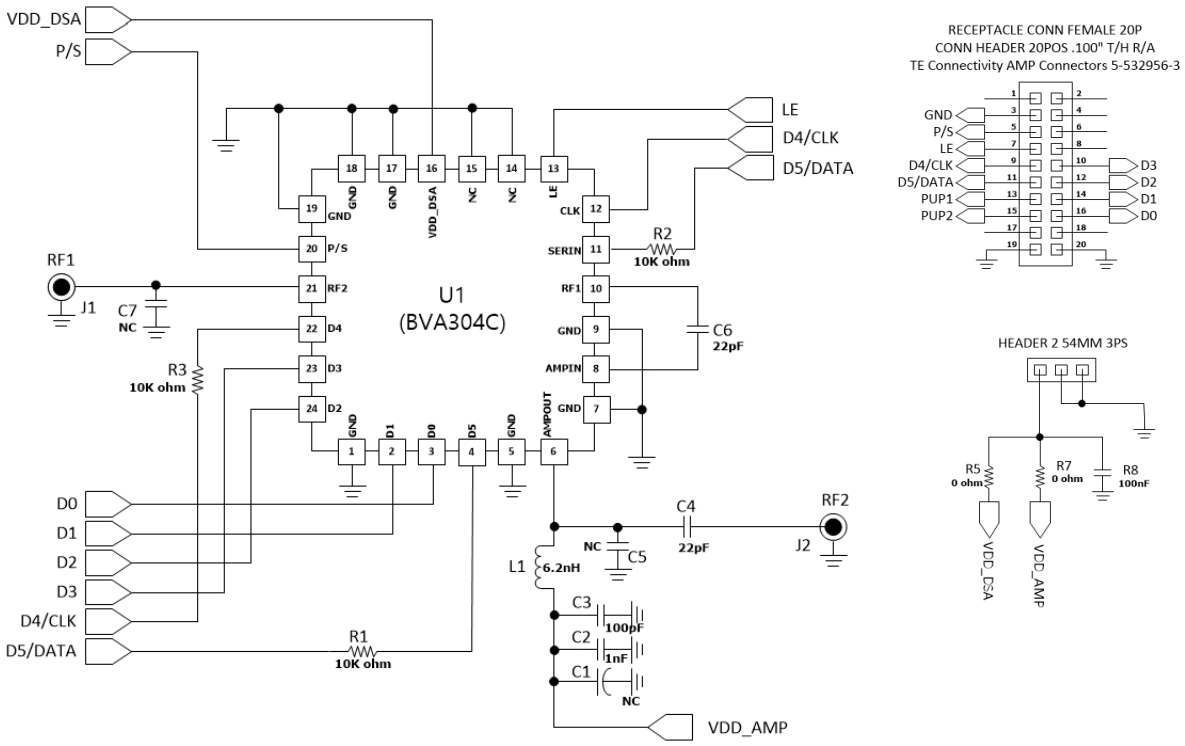


Figure 52. Evaluation Board PCB

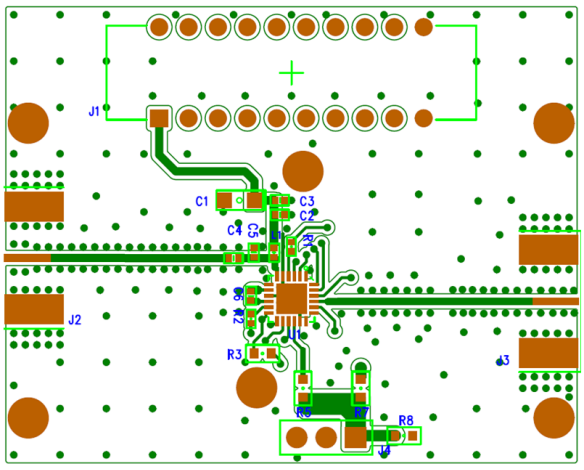


Table 18. Application Circuit

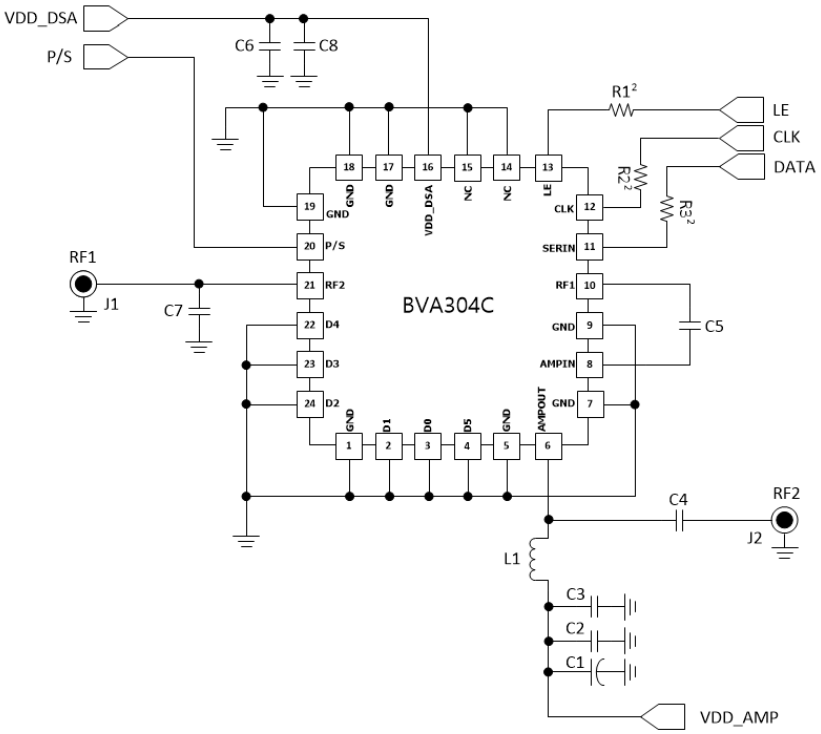
Application Circuit Values Example			
Frequency band	IF Circuit 50MHz - 500MHz	RF Circuit 500MHz - 1.7GHz	RF Circuit 1.7GHz - 4GHz
C6/C4	2.2nF	56pF	22pF
L1	330nH	22nH	6.2nH

Table 19. Bill of Material - Evaluation Board

No.	Ref Des	Part Qty	Part Number	REMARK
1	C4,C6	2	CAP 0402 22pF	Another circuit refer to table 18
2	C2	1	CAP 0402 100nF	
3	C1	1	NC	
4	C22	1	CAP 0402 100nF	
5	L1	1	IND 0402 6.2nH	Another circuit refer to table 18
6	C3	1	CAP 0402 100pF	
7	R1,R2	2	RES 0402 10Kohm	
8	R3	1	RES 0603 10Kohm	
9	R4,R5,R7	3	RES 0603 0ohm	
10	J1	1	Receptacle connector	
11	U1	1	QFN4X4_24L_BVA304C	
12	J2,J3	2	SMA_END_LAUNCH	

Notice: Evaluation Board for Marketing Release was set to 1.7GHz to 4GHz application circuit (Refer to Table 17)

Figure 53. Recommended Serial mode Application Circuit schematic



1. BVA304C is set to default minimum gain state when it is initially powered up. (Maximum attenuation state)
2. Recommended to add the R1/R2/R3 with value of 1k ohm.

Figure 54. Suggested PCB Land Pattern and PAD Layout

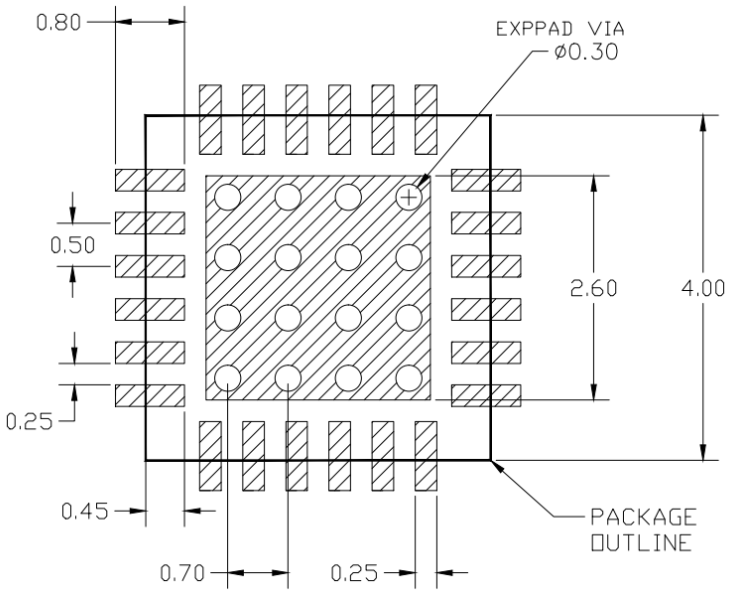
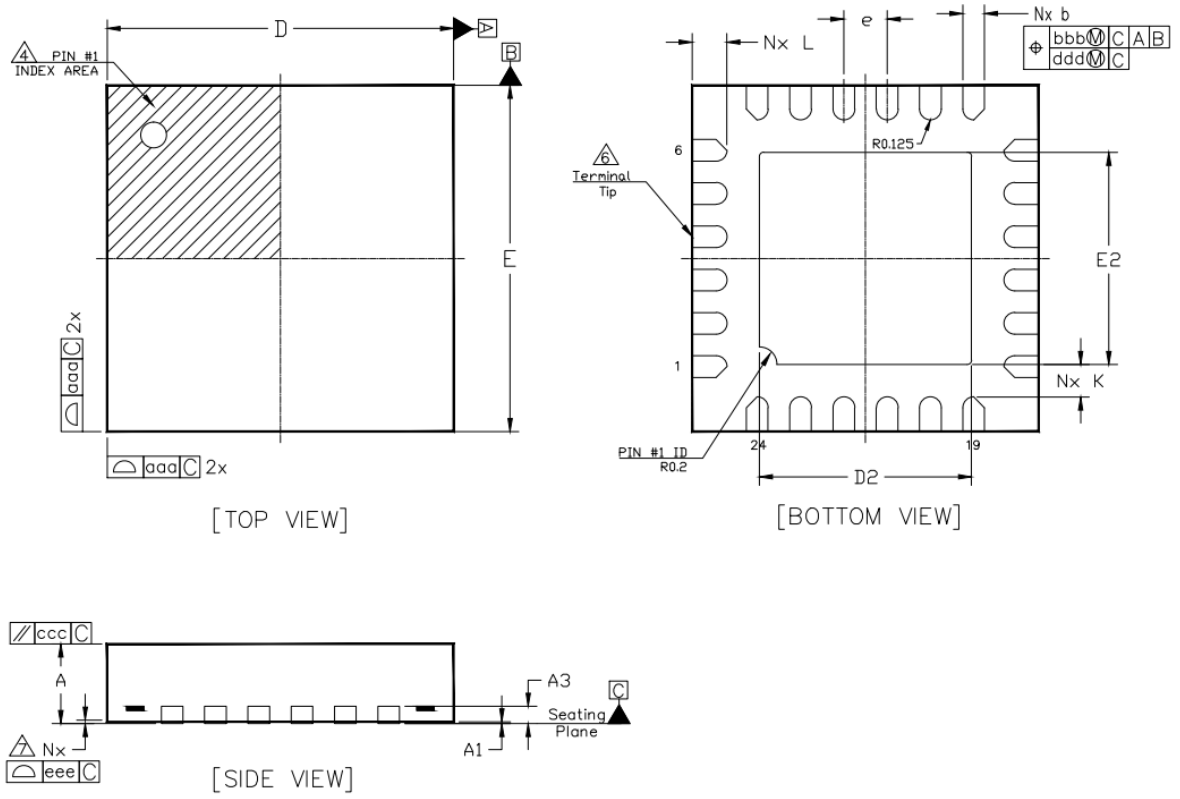


Figure 55. Package Outline Dimension



NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5–2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals each D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.3mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

Dimension Table (Notes 1,2)				
Symbol Thickness	Min	Nominal	Max	Note
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref.	---	
b	0.18	0.25	0.30	6
D		4.00 BSC		
E		4.00 BSC		
e		0.50 BSC		
D2	2.30	2.45	2.55	
E2	2.30	2.45	2.55	
K	0.2	---	---	
L	0.30	0.40	0.50	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		24		3
ND		6		5
NE		6		5

Figure 56. Evaluation Board PCB Layer Information

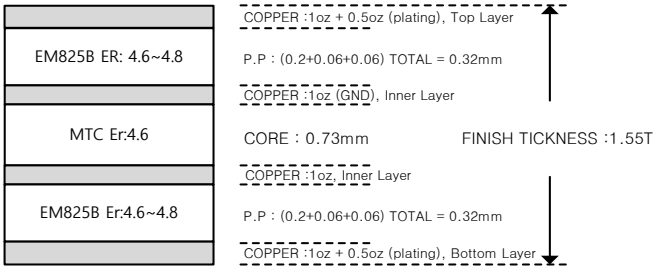
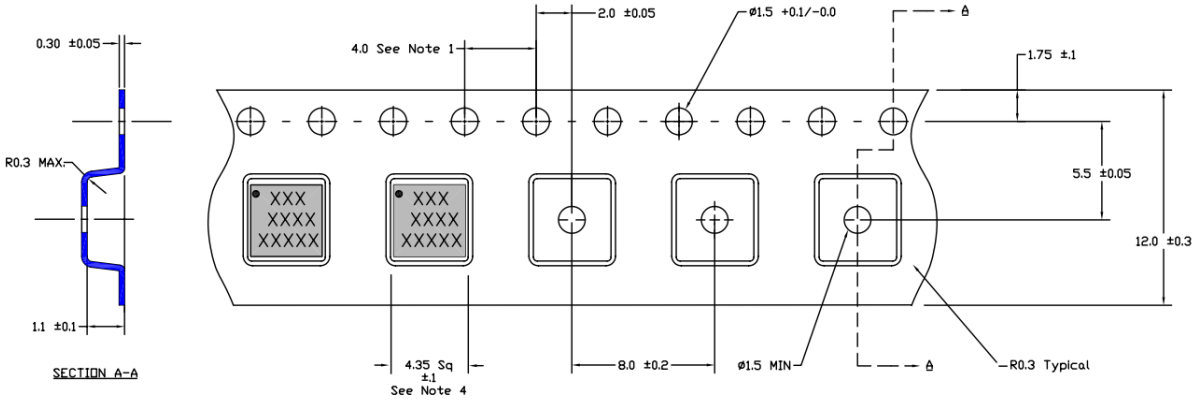


Figure 57. Tape & Reel



Packaging information:	
Tape Width	12mm
Reel Size	7”
Device Cavity Pitch	8mm
Devices Per Reel	1K

Figure 58. Package Marking

Marking information:	
BVA304C	Device Name
YY	Year
WW	Work Week
XX	LOT Number

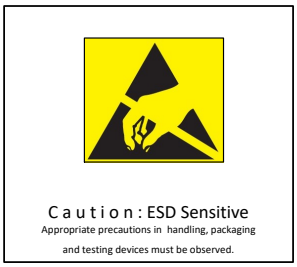
Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1C
Value:	1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2017
MSL Rating:	**Level 1 at +260°C convection reflow**
Standard:	JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

2	**N**	**9**	**6**	**F**