Rev 1; 4/09

5.0V 8-Bit Programmable Timing Element

DS1124

General Description

The DS1124 is an 8-bit programmable timing element similar in function to the DS1021-25. The 256-delay intervals are programmed by using a 3-wire serial interface. With a 0.25ns step size, the DS1124 can provide a delay time from 20ns up to 84ns with an integral nonlinearity of ±3ns.

Applications

LCD Televisions

Telecommunications

Digital Test Equipment

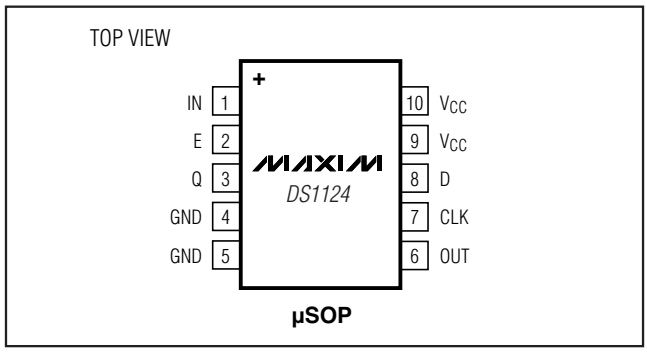
Digital Video Projection

Signal Generators and Analyzers

Features

- **0.25ns Step Size**
- **Leading- and Trailing-Edge Accuracy**
- **CMOS/TTL Compatible**
- **Can Delay Signals by a Full Period or More**
- **3-Wire Serial Programming Interface**
- **Single 5.0V Power Supply**
- **10-pin µSOP Package**

Pin Configuration

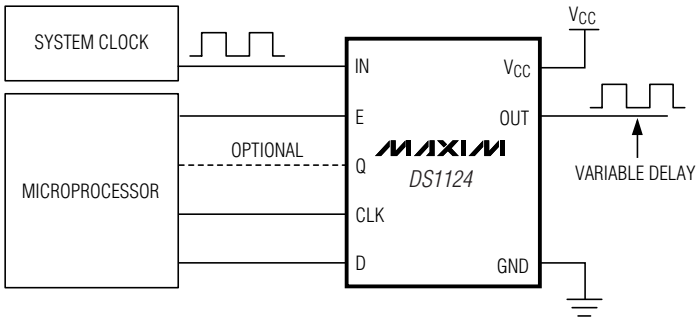


Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1124U-25+	-40°C to +85°C	10 µSOP
DS1124U-25+T	-40°C to +85°C	10 µSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Pin Relative to Ground .....-0.5V to +6.0V
Voltage Range on IN, E, D, and CLK
Relative to Ground* .....-0.5V to (V_{CC} + 0.5V)
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Short-Circuit Output Current .....50mA for 1 second
Soldering Temperature.....See J-STD-020 Specification

**Not to exceed +6.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	4.75		5.25	V
Input Logic 1	V_{IH}		2.2		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Current	I_{CCA}			15	30	mA
High-Level Output Current	I_{OH}	V_{CC} = min, V_{OH} = 2.3V			-1.0	mA
Low-Level Output Current	I_{OL}	Q pin, V_{CC} = min, V_{OL} = 0.5V			4.0	mA
		OUT pin, V_{CC} = min, V_{OL} = 0.5V			8.0	
Input Leakage	I_L		-1.0		+1.0	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{CLK}				10	MHz
Input Pulse Width (E, CLK)	t_{EW}, t_{CW}		50			ns
Data Setup to Clock	t_{DSC}		30			ns
Data Hold from Clock	t_{DHC}		0			ns
Data Setup to Enable	t_{DSE}		30			ns
Data Hold to Enable	t_{DHE}		0			ns
Enable Setup to Clock	t_{ES}		0			ns
Enable Hold from Clock	t_{EH}		30			ns
E to Q Valid	t_{EQV}				50	ns
E to Q High Impedance	t_{EQZ}		0		50	ns
CLK to Q Valid	t_{CQV}				50	ns
CLK to Q Invalid	t_{CQX}		0			ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
E to Delay Valid	t_{EDV}				50	µs
E to Delay Invalid	t_{EDX}		0			ns
Power-Up Time	t_{PU}				100	ms
Delay Step Size	t_{STEP}	T_A = +25°C	-0.75	+0.25	+1	ns
Step 0 Delay	t_{D0}	(Note 2)	17	20	23	ns
Step 0 Delay Initial Accuracy		V_{CC} = 5V, T_A = +25°C	-0.6		+0.6	ns
Step 0 Voltage Variation			-0.4		+0.4	ns
Step 0 Temperature Variation		0°C to +70°C	-1		+1	ns
Step 0 Temperature Variation		-40°C to +85°C	-1		+1	ns
Step 255 Delay	t_{D255}	(Note 2)	77	83.75	88	ns
Step 255 Delay Initial Accuracy		V_{CC} = 5V, T_A = +25°C	-0.6		+0.6	ns
Step 255 Voltage Variation			-0.4		+0.4	ns
Step 255 Temperature Variation		0°C to +70°C	-3		+3	ns
Step 255 Temperature Variation		-40°C to +85°C	-5		+5	ns
Integral Nonlinearity (Deviation from Straight Line)	t_{ERR}	V_{CC} = 5V, T_A = +25°C (Note 3)	-2	0	+2	ns
Minimum Input Pulse Width	t_{WI}	(Note 4)	40			ns
Minimum Input Period	t_{PER}	(Note 5)	80			ns
Input Rise and Fall Times	t_R, t_F	(Note 6)	0		1	µs

Note 1: All voltages are referenced to ground.

Note 2: Measured from rising edge of the input to the rising edge of the output. The programmed delay, t_D, can be programmed with values from 0 to 255. See Figure 1.

Note 3: See the *Integral Nonlinearity* section and Figure 5.

Note 4: This is the minimum allowable interval between transitions on the input to ensure accurate device operation. This parameter can be violated but timing accuracy may be impaired and ultimately very narrow pulse widths will result in no output from the device. See Figure 1.

Note 5: When a 50% duty cycle input clock is used, this defines the highest usable clock frequency. When asymmetrical clock inputs are used, the maximum usable clock frequency must be reduced to conform to the minimum input pulse-width requirement. See Figure 1.

Note 6: Faster rise and fall times give the greatest accuracy in measured delay. Slow edges (outside the specification maximum) can result in erratic operations.

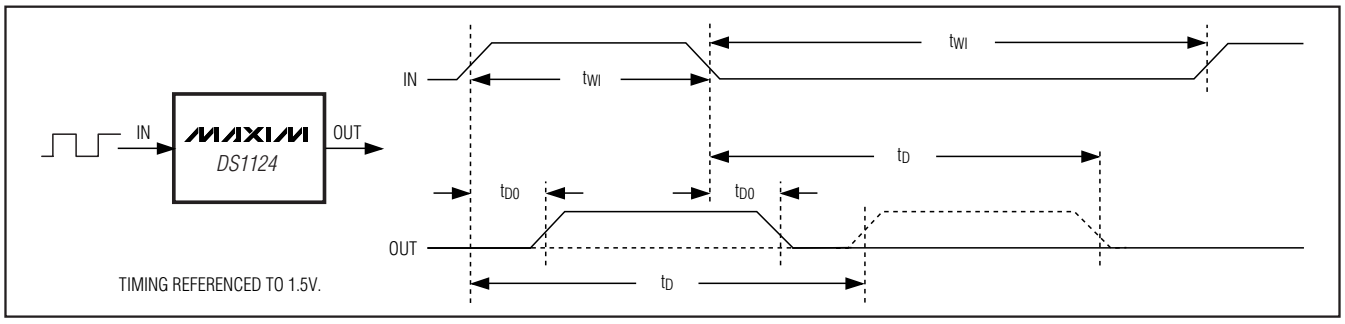


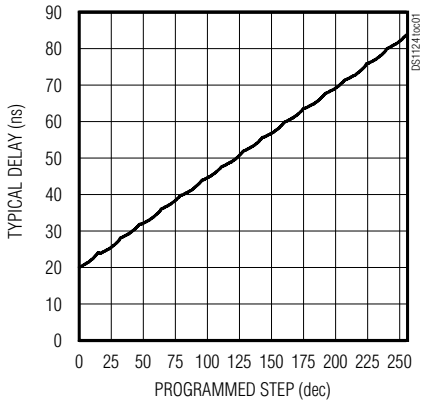
Figure 1. Delay Timing Diagram

5.0V 8-Bit Programmable Timing Element

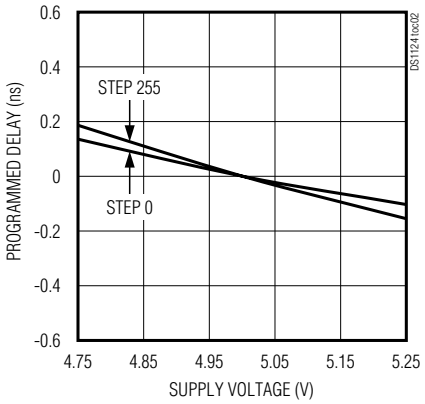
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

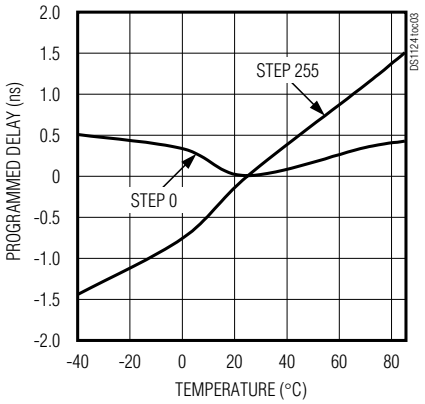
TYPICAL DELAY vs. PROGRAMMED STEP



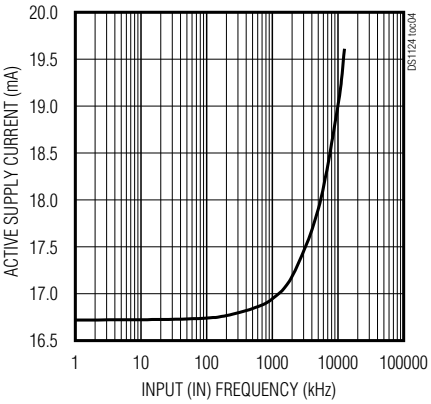
CHANGE FROM NOMINAL DELAY vs. SUPPLY VOLTAGE



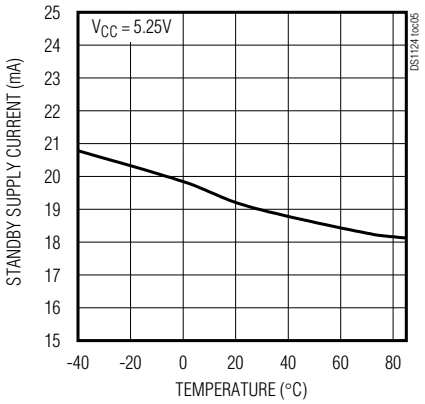
CHANGE FROM NOMINAL DELAY vs. TEMPERATURE



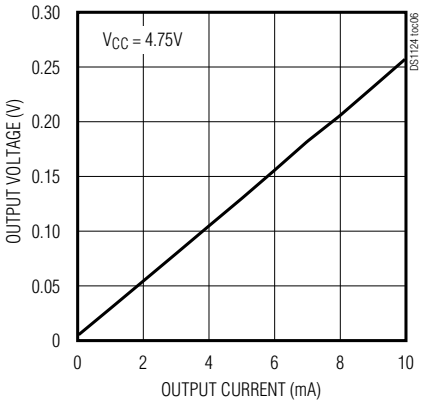
ACTIVE SUPPLY CURRENT vs. INPUT FREQUENCY



STANDBY SUPPLY CURRENT vs. TEMPERATURE



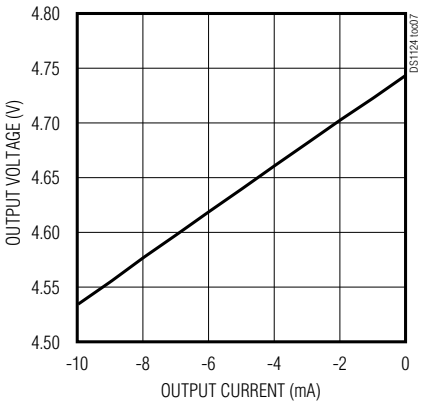
OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT



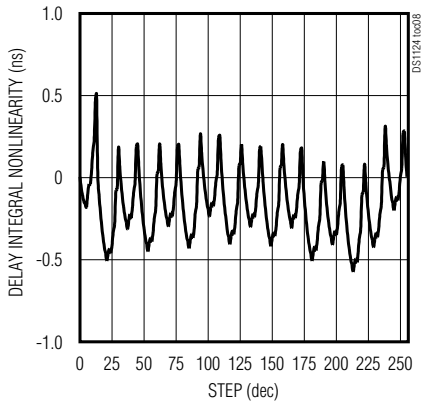
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

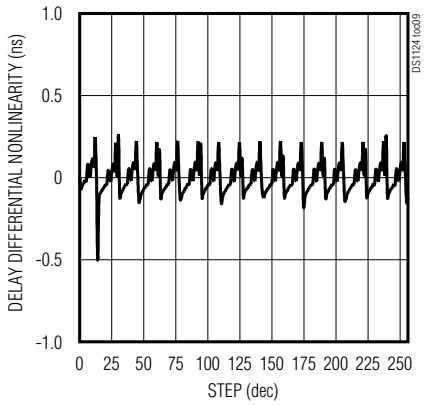
OUTPUT VOLTAGE HIGH vs. OUTPUT CURRENT



DELAY INTEGRAL NONLINEARITY vs. STEP



DELAY DIFFERENTIAL NONLINEARITY vs. STEP



Pin Description

PIN	NAME	FUNCTION
1	IN	Delay Input Signal
2	E	Input Enable
3	Q	Serial Data Output
4, 5	GND	Ground. Both grounds must be connected.
6	OUT	Delay Output Signal
7	CLK	Serial Clock Input
8	D	Serial Data Input
9, 10	V_{CC}	Power Supply. Both supplies must be connected.

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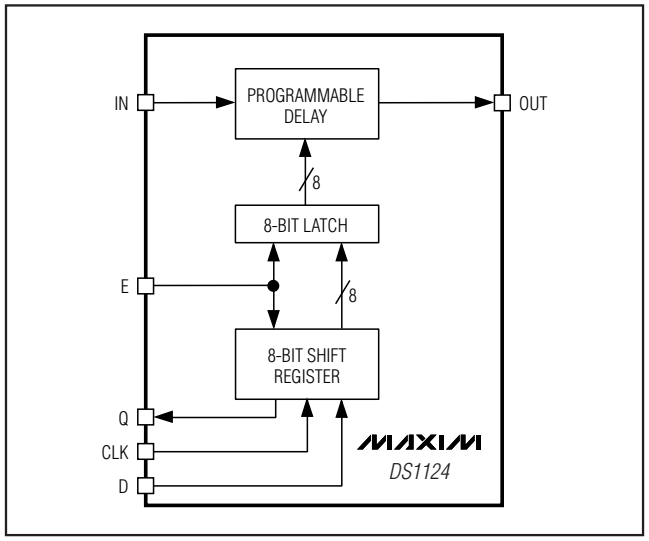
Block Diagram



Detailed Description

The DS1124 is an 8-bit programmable delay line that can be adjusted between 256 different delay intervals. The DS1124 architecture (see Figure 2) allows some signals to be delayed by more than one period, which lets the phase of the signal to be adjusted up to a full 360°. Programming is performed by a 3-wire serial interface. Using the 3-wire interface, it is possible to cascade multiple devices together for systems requiring multiple programmable delays without using additional I/O resources.

Using the Serial Programming Interface

Serial mode operates similar to a shift register. When the E pin is set at a high logic level, it enables the shift register and CLK clocks the data, D, into the register one bit at a time starting with the most significant bit. After all 8 bits are shifted into the DS1124, E must be pulled low to end the data transfer and activate the new value. A settling time (t_{EDV}) is required after E is pulled low before the signal delay will meet its specified accuracy. A timing diagram for the serial interface is shown in Figure 3.

The 3-wire interface also has an output (Q) that can be used to cascade multiple 3-wire devices, and it can be used to read the current value of the devices on the bus. To read the current values stored by the 3-wire device(s), the latch must be enabled and the value of Q must be read and then written back to D before the register is clocked. This causes the current value of the register to be written back into the DS1124 as it is being read. This can be accomplished in a couple of different ways. If the microprocessor has an I/O pin that is high impedance when set as an input, a feedback resistor (R_{FB}, generally between 1kΩ and 10kΩ) can be used to write the data on Q back to D as the value is read, see Figure 4A. If the microprocessor has an internal pullup on its I/O pins, or only offers separate input and output pins, the value in the register can still be read. The circuit shown in Figure 4B allows the Q values to read by the microprocessor, which must write the Q value to D before it can clock the bus to read the next bit. If the Q values are read without writing them to D (with the pullup or otherwise), the read will be destructive. A destructive read cycle likely results in an undesirable change in the delay setting.

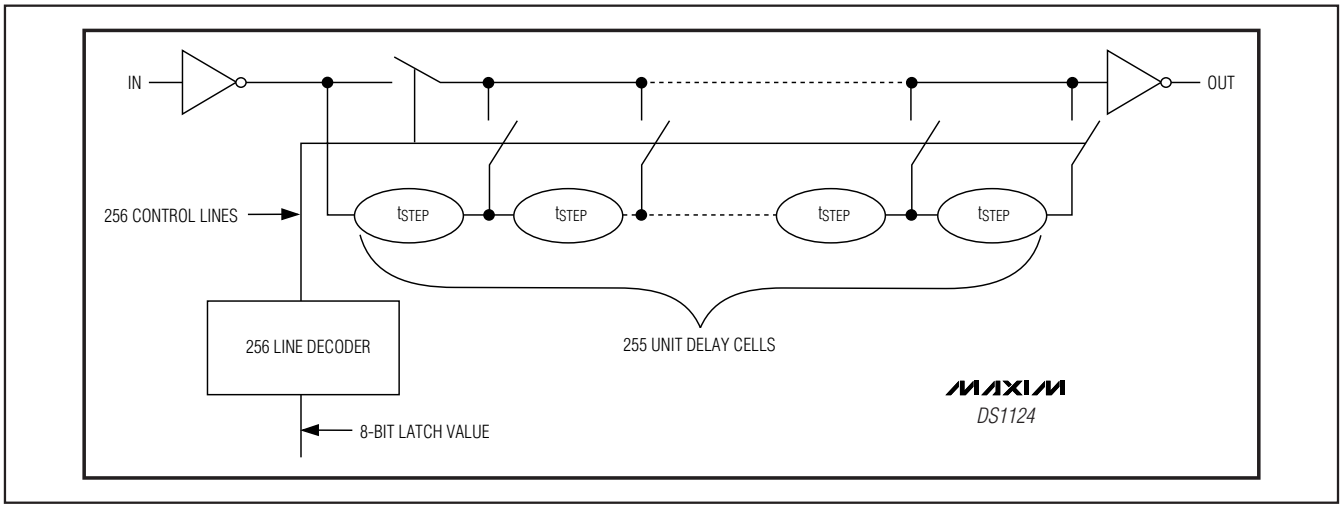


Figure 2. Conceptual Design

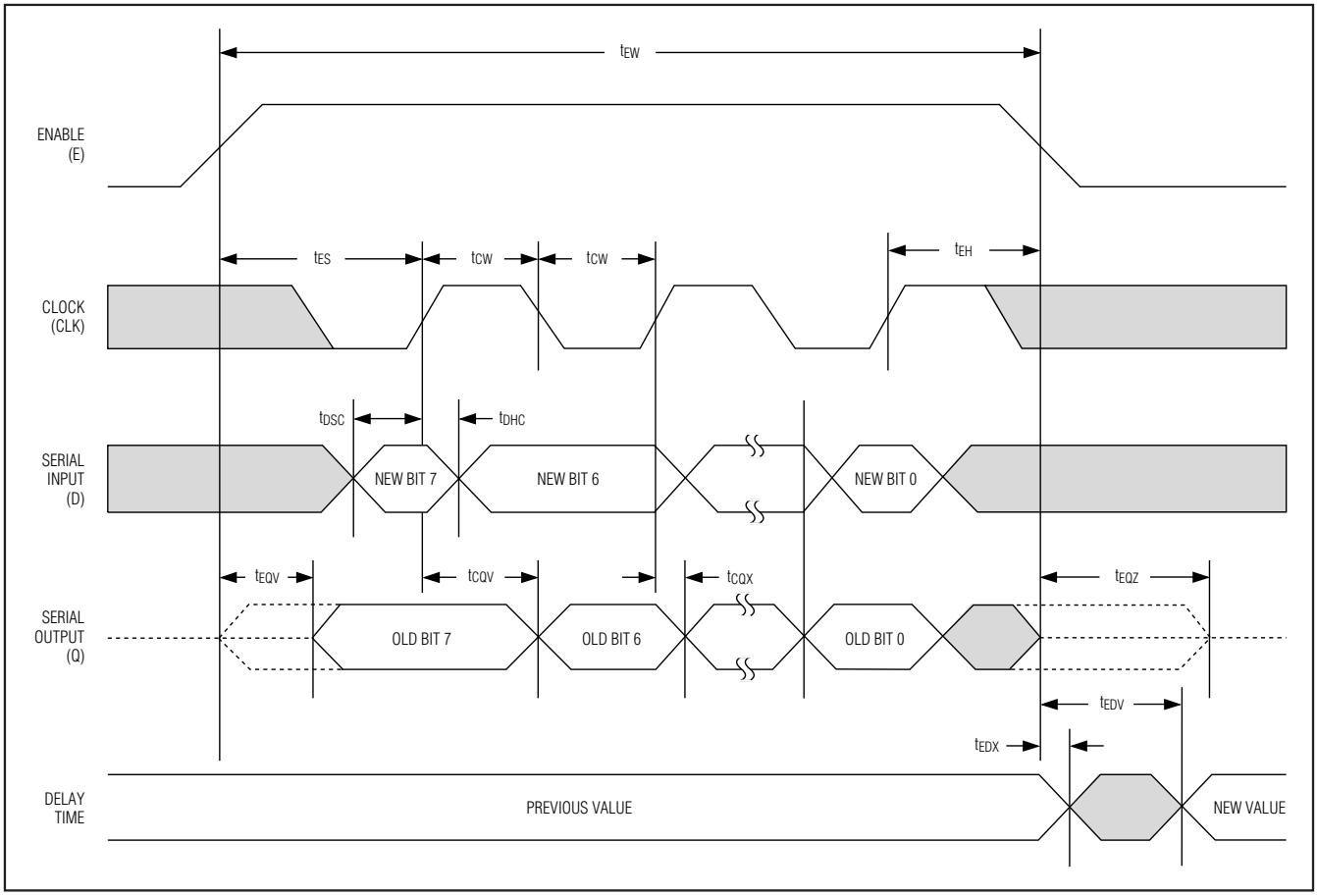


Figure 3. Serial Interface Timing Diagram

Figure 4C shows how to cascade multiple DS1124s onto the same 3-wire bus. One important detail of writing software for cascaded 3-wire devices is that all the devices on the bus must be written to or read from during each read or write cycle. Attempting to write to only the first device (U1) would cause the data stored in U1 to be shifted to U2, U2's data would be shifted to U3, etc. As shown, the microprocessor would have to shift 24 bits during each read or write cycle to avoid inadvertently changing the settings in any of the 3-wire devices. Also note that the feedback resistor or a separate input (not shown) can still be used to read the 3-wire device settings when multiple devices are cascaded.

Integral Nonlinearity

Integral nonlinearity (INL) is defined as the deviation from a straight line response drawn between the measured step zero delay (t_{D0}) and the measured step 255 delay (t_{D255}) with respect to the step 0 delay. Figure 5 shows INL's effect on delay performance graphically.

Application Information

Power-Supply Decoupling

To achieve the best results when using the DS1124, decouple the power supply with a 0.01µF and a 0.1µF capacitor. Use high-quality, ceramic, surface mount capacitors, and mount the capacitors as close as possible to the V_{CC} and GND pins of the DS1124 to minimize lead inductance. The DS1124 may not perform as specified if good decoupling practices are not followed.

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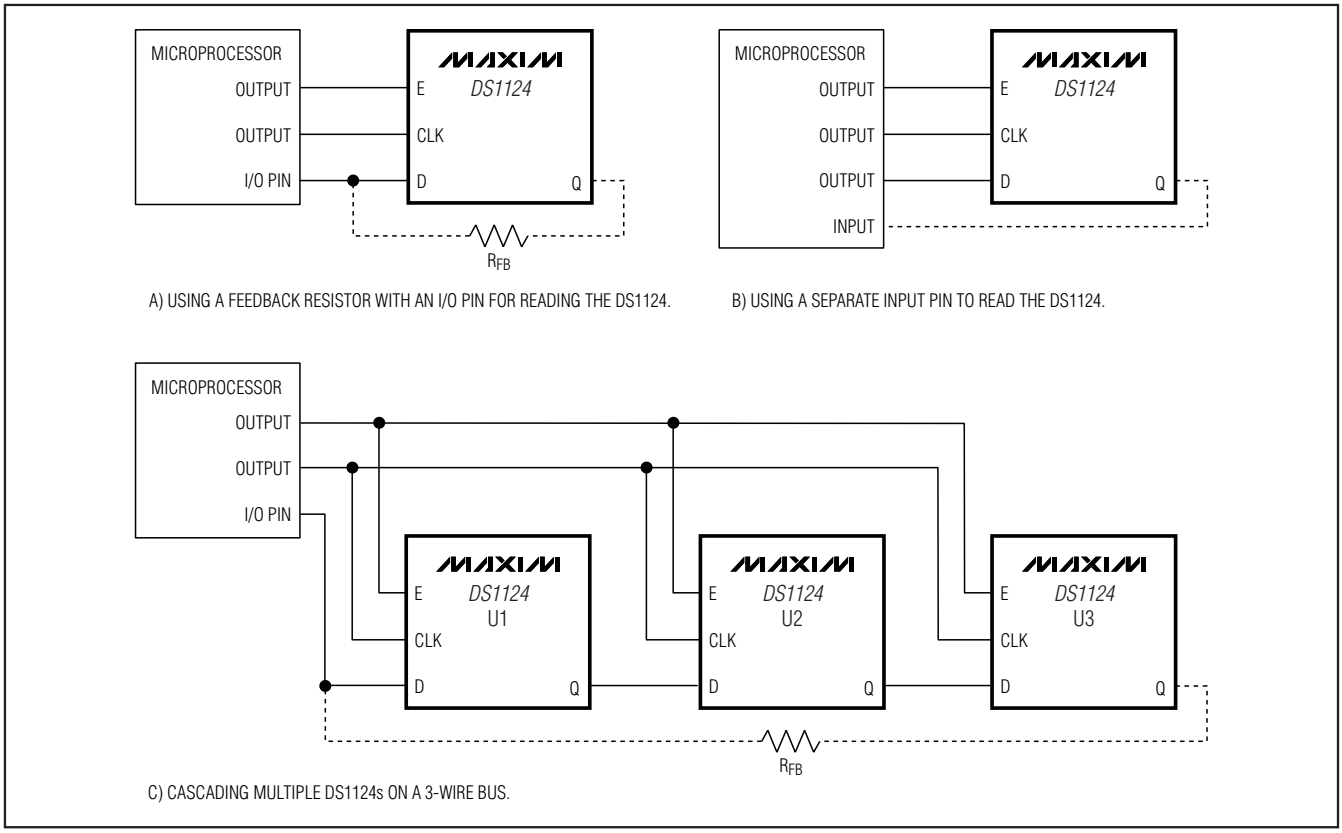

Figure 4. Examples Using the Serial Interface

Test Conditions

Input:

Ambient Temperature:	25°C ±3°C
Supply Voltage (V_{CC}):	5.0V ±0.1V
Input Pulse:	High = 3.0V ±0.1V
	Low = 0.0V ±0.1V
Source Impedance:	50Ω max
Rise and Fall Times:	3.0ns max (measured between 0.6V and 2.4V)
Pulse Width:	250ns
Period:	10µs

Output: The outputs are loaded with 15pF. Delay is measured between the 1.5V level of the rising or falling edge of the input signal and the corresponding edge of the output signal.

Note: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

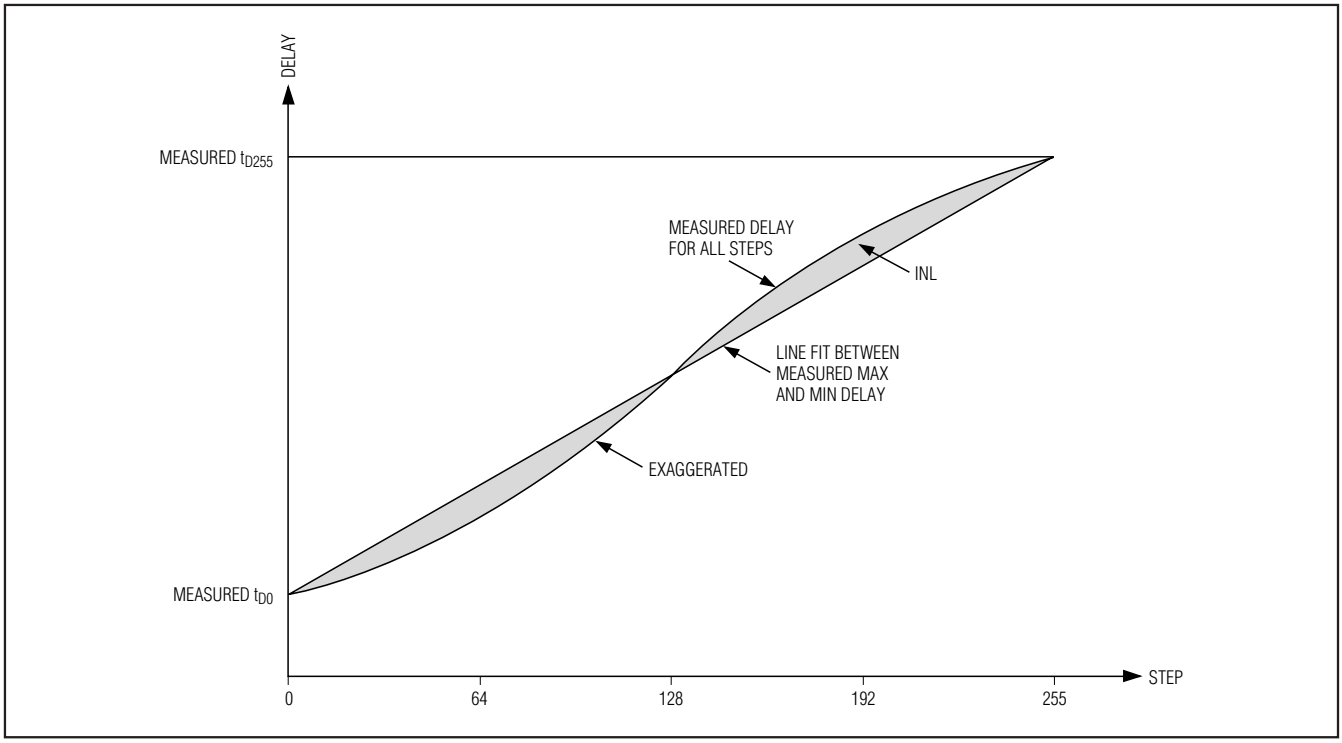

Figure 5. Integral Nonlinearity

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 µSOP	—	**21-0061**

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/07	Initial release.	—
1	4/09	Added V_{CC} = 5V to the t_{ERR} specification in the *Electrical Characteristics* table, indicating that it is only tested at T_A = 25°C and V_{CC} = 5V.	3

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