PCN

AO-PCN-2022-016-A

Introduction of 2nd source for classic InGaAlP chip and backend production location Wuxi for Multi TOPLED

Published by ams-OSRAM AG
Tobelbader Strasse 30, 8141 Premstaetten, Austria
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ams-osram.com

01.07.2022

Dear Customer,

please review this **PCN** and provide your feedback in the **Customer approval form** (at the end of this PCN document) to your ams OSRAM sales partner before **05.08.2022** *).

Please take note, that this PCN is published for the introduction of **additional source(s)**.

Your prompt reply will help ams OSRAM to assure a smooth and well executed transition. If ams OSRAM does not hear from your side by the due date, we will assume your (if you are a Distributor: and your customer's) full acceptance to this proposed change and its implementation.

ams OSRAM understands the time requirements your organization needs to approve this PCN.
However, if you can provide ams OSRAM an estimated date your organization will have finalized this PCN review, ams OSRAM can use this date to plan continued production to secure your order needs during the expansion with additional source(s).

Your attention and response to this matter is highly appreciated.

Please direct your inquiries to your local Sales office.

*) ams OSRAM aligns with the widely recognized JEDEC/ECIA/IPC Joint Standard No. 46, which stipulates:

- Customers should acknowledge receipt of the PCN within 30 days of delivery of the PCN.
- Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change.
- After acknowledgement, lack of additional response within the 90 day period constitutes acceptance of the change. If the customer requires additional time to perform sample testing, beyond the 90 day review period, an extension must be negotiated with the supplier.

Subject of change:	Introduction of 2nd source for classic InGaAlP chip and backend production location Wuxi for Multi TOPLED	
Affected products:	**Standard:** LSG T676, LSY T676 **Low current:** LSG T67K, LYG T67K	
Reason for change:	• Secure continuous supply • Introduction of additional supplier chips • Harmonization of back end production location	
Description of change:	Current status Inhouse chips	New status Inhouse chips + 2nd (and 3rd) source chips provided by supplier(s)
	Production location Penang/Malaysia	Production location Wuxi/China
	For details refer to file 2_cip_AO-PCN-2022-016-A	
Time schedule for PCN material: (after implementation of change):	Final qualification report:	01.08.2022
	Samples available:	01.08.2022*) *) For details refer to file 2_cip_AO-PCN-2022-016-A
	Intended Start of delivery:	01.12.2022**) **) or earlier if released by customer and upon mutual agreement
	Customer Review Finalization:	01.07.2023***) ***) Expected final feedback of customer. Released order volume is related to deliveries of material from both previous and additional source(s).
Assessment:	**No change in fit, form and reliability → no change in Datasheets**	
Documentation:	Customer information package 2_cip_AO-PCN-2022-016-A 3_cip_AO-PCN-2022-016-A_Qual	

Note:
Pre-PCN material: Products of current status, means before implementation of the changes as described in the PCN.
PCN material: Products with implementation of the changes as described in the PCN.

Customer approval form AO-PCN-2022-016-A

Introduction of 2nd source for classic InGaAlP chip and backend production location Wuxi for Multi TOPLED

Please list product(s) affected in your application(s):

Please check the appropriate box below:

◯ **Approval:** We agree with the proposed change and accept start of the shipment upon availability of PCN material	◯ **Not relevant:** Change is not relevant for products in use.

◯ **Change cannot be accepted:**

- **We have objections:**
- **We request following Information:**
- **We request following Samples:**
- **Expected approval date:**
- **Volume requirements for Pre-PCN material:**

◯ **Remarks:**

Sender:

Company:

Address / Location:

Signature: **Date:**

Please return this approval form to your Sales partner.

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Introduction of 2nd source for classic InGaAlP chip and backend production location Wuxi for Multi TOPLED

Customer information package

S&MK EM FQE/OS Q CQM A ITR
2022-07-01

Agenda

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Introduction of 2nd source for classic InGaAlP chip and backend production location Wuxi for Multi TOPLED

Reason for change

Item	Description
1.	Secure continuous supply
2.	Introduction of additional supplier chips
3.	Harmonization of back end production location

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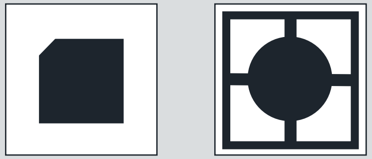
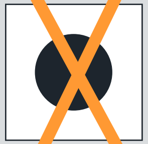
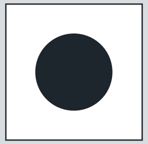
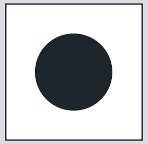
Introduction of 2nd source for classic InGaAlP chip and backend production location Wuxi for Multi TOPLED

Description of change for standard chips

Item	Current status	2nd source chip A	2nd source chip A	2nd source chip B
Wafer size [mm]	100	100		
Wafer substrate	GaAs	GaAs		
Height [µm]	220	180		
Chip dicing process	Sawing	Sawing		
Picture (schematic)				
Chip size [µm]	200 x 200	200 x 200	180 x 180	180 x 180
Front metal type	Al	Au		
Front metal thickness [µm]	1.5	2.25 - 2.9		
Back metal type	Au	Au		
Back metal thickness [µm]	0.25	0.35 - 0.50		
Bond pad size [µm]	100	100		

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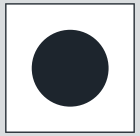
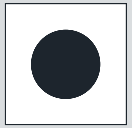
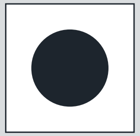
Description of change for low current chips

Item	Current status	2nd source chip C	2nd source chip D
Wafer size [mm]	100	100	
Wafer substrate	GaAs	GaAs	
Height [µm]	190	180	
Chip dicing process	Sawing	Sawing	
Picture (schematic)			
Chip size [µm]	170 x 170	160 x 160	170 x 170
Front metal type	Al	Au	
Front metal thickness [µm]	1.5	2.25-2.9	
Back metal type	Au	Au	
Back metal thickness [µm]	0.25	0.35-0.50	
Bond pad size [µm]	100	90	100

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Description of change for all devices

Current status	New status
Backend production location Penang/Malaysia	Backend production location Wuxi/China

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Changes in the datasheets

No change in fit, form and function of affected devices → no change in Datasheets

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List of affected products

Brand	Standard	Low current
Multi TOPLED	LSG T676	LSG T67K
	LSY T676	LYG T67K

Due to complexity not all device/chip source combinations will be available at start of series production.

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PCN Samples

Standard	Low current
LSG T676	LSG T67K
LSY T676	LYG T67K

Color code: [light blue] available on 01.08.2022 [grey] on request

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Time schedule

for PCN material (after implementation of change):		
Final qualification report	01.08.2022	
Samples available	01.08.2022	
Intended Start of delivery	01.12.2022*)	*) or earlier if released by customer and upon mutual agreement

Customer Review Finalization:	01.07.2023 **)	**) Expected final feedback of customer. Released order volume is related to deliveries of material from both previous and additional source(s).

Note:
PCN material: Products with implementation of the changes as described in the PCN.

Sensing is life

Qualification Results overview 220121C1

Subject	Qualification for 2nd source Chip introduction for classic InGaAlP Multi TOPLED devices
Date	01.07.2022
Tested device	Chip A: LSY T676 Chip B: LSG T676 Chip C: LSG T67K, LYG T67K Chip D: LSG T67K, LYG T67K
Brand (including sub brands)	Multi TOPLED
Applies to	LSY T676, LSG T676, LSG T67K, LYG T67K

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Pre-conditioning according to Jedec Level II where applicable as per AEC-Q102 AEC-Q102 #A1 **LSY T676 (Chip A)**

Test Performed	Condition	Duration	Sample Size	Failures El. AEC-Q102 #E1	Failures Opt. AEC-Q102 #E1	Failures Vis AEC-Q102 #E0
Wet High Temperature Operating Life WHTOL1 *JESD22-A101* AEC-Q102 #A2a Test PCB: IMS-Al	T_A = 85°C; r.H. = 85%; T_s = 95°C; T_j = 115°C I_F = 20 mA $T_{on/off}$ = 30 min	1000 h	3x26	0	0	0
Wet High Temperature Operating Life WHTOL2 *JESD22-A101* AEC-Q102 #A2b Test PCB: FR4	T_A = 85°C; r.H. = 85% I_F = 5 mA	1000 h	3x26	0	0	0
Powered Temperature Cycle PTC *JESD22-A105* AEC-Q102 #A3a Test PCB: IMS-Al	T_A = -40°C/+100°C T_s = 105°C; T_j = 125°C I_F = 15 mA $t_{on/off}$ = 5 min	1000 c	3x26	0	0	0
Temperature Cycling TC *JESD22-A104* AEC-Q102 #A4a Test PCB: FR4	T_A = -40°C/+100°C 15 min each extreme	1000 c	3x26	0	0	0
High Temperature Operating Life HTOL1 *JESD22-A108* AEC-Q102 #B1a Test PCB: IMS-Al	T_A = 85°C; T_s = 95 °C T_j = 115 °C; I_F = 20 mA	1000 h	3x26	0	0	0
Pulsed Operating Life PLT *JESD22-A108* AEC-Q102 #B3 Test PCB: FR4	T_A = 25°C I_F = 55 mA; t_p = 0,1ms; D = 3%	1000 h	3x26	0	0	0
Dew DEW *AEC-Q102-001* AEC-Q102#C7 Test PCB: FR4	$T_{A,min}$ = 10°C $T_{A,max}$ = 80°C r.H. = 53-100%	10 c	3x26	0	0	0
Solderability SD *IEC 60068-2-58* AEC-Q102 #C10	T_A = 235°C method 2 (reflow simulation)	1x	3x10	-	-	0
Hydrogen Sulphide H2S *IEC 60068-2-43* AEC-Q102 #C12 Test PCB: FR4	15 ppm H_2S 40°C/90% r.H.	336 h	3x26	0	0	0
Flowing Mixed Gas FMG *IEC 60068-2-60* AEC-Q102 #C13 Test PCB: FR4	T_A = 25°C, r.H. = 75% Test method 4	500 h	3x26	0	0	0
Board Flex Test BF *AEC-Q102-002* AEC-Q102 #C14 Test PCB: FR4	2 mm	1x	3x10	0	0	0
Electrostatic Discharge HBM *ANSI/ESDA/ JEDEC JS-001* AEC-Q102 #E3 Test PCB: FR4	Human Body Model	2000 V	3x10	0	0	0

Constant Acceleration CA	*MIL-STD-750-2* AEC-Q102 #G1	Method 2006 2000 gf; 1 min in x/y/z (+/- direction)	1x	3x10	for uncasted packages only
Vibration Variable Frequency VVF	*JESD22-B103* AEC-Q102 #G2	20g, 20-2000Hz; 4min / cy; 4cy/axis service condition 1	1x	sequential samples	
Mechanical Shock MS	*JESD22-B110* AEC-Q102 #G3	1500g for 0.5ms, 5 blows, 3 orientations	1x	sequential samples	
Hermeticity HER	*JESD22-A109* AEC-Q102 #G4	Leak Test: Fine & Gross	1x	sequential samples	

Additional Tests to AEC Q102

Test Performed		Condition	Duration	Sample Size	Failures El.	Opt.	Vis
Electrostatic Discharge MM	*JESD22-A115* Test PCB: FR4	Machine Model	200 V	3x10	0	0	0

Failure criteria:

Electrical failures:	red:	V_f (I_f =20 mA)	> 2,3 V; ± 10% from initial value
	yellow:	V_f (I_f =20 mA)	> 2,4 V; ± 10% from initial value
Optical failures:	I_v (I_f =20 mA)		absolute limit: ± 50% max.
	λ_{dom} (I_f = 20 mA)		± 2 nm initial value
Visual failures:	acc JEDEC JESD22-B101		

Conclusion: The tested devices representing the product family as stated in the applies to section fulfill the reliability requirements of AEC-Q102 Initial/Rev-A.

Pre-conditioning according to Jedec Level II where applicable as per AEC-Q102 AEC-Q102 #A1 **LSG T676 (Chip B)**

Test Performed	Condition	Duration	Sample Size	Failures El. AEC-Q102 #E1	Failures Opt. AEC-Q102 #E1	Failures Vis AEC-Q102 #E0
Wet High Temperature Operating Life WHTOL1 *JESD22-A101* AEC-Q102 #A2a Test PCB: IMS-Al	T_A = 85°C; r.H. = 85%; T_s = 95°C; T_j = 120°C I_F = 20 mA $T_{on/off}$ = 30 min	1000 h	3x26	0	0	0
Wet High Temperature Operating Life WHTOL2 *JESD22-A101* AEC-Q102 #A2b Test PCB: FR4	T_A = 85°C; r.H. = 85% I_F = 5 mA	1000 h	3x26	0	0	0
Powered Temperature Cycle PTC *JESD22-A105* AEC-Q102 #A3a Test PCB: IMS-Al	T_A = -40°C/+100°C T_s = 105°C; T_j = 125°C I_F = 15 mA $t_{on/off}$ = 5 min	1000 c	3x26	0	0	0
Temperature Cycling TC *JESD22-A104* AEC-Q102 #A4a Test PCB: FR4	T_A = -40°C/+100°C 15 min each extreme	1000 c	3x26	0	0	0
High Temperature Operating Life HTOL1 *JESD22-A108* AEC-Q102 #B1a Test PCB: IMS-Al	T_A = 85°C; T_s = 95°C T_j = 120°C; I_F = 20 mA	1000 h	3x26	0	0	0
Pulsed Operating Life PLT *JESD22-A108* AEC-Q102 #B3 Test PCB: FR4	T_A = 25°C I_F = 55 mA; t_p = 0,1ms; D = 3%	1000 h	3x26	0	0	0
Dew DEW *AEC-Q102-001* AEC-Q102#C7 Test PCB: FR4	$T_{A,min}$ = 10°C $T_{A,max}$ = 80°C r.H. = 53-100%	10 c	3x26	0	0	0
Solderability SD *IEC 60068-2-58* AEC-Q102 #C10	T_A = 235°C method 2 (reflow simulation)	1x	3x10	-	-	0
Hydrogen Sulphide H2S *IEC 60068-2-43* AEC-Q102 #C12 Test PCB: FR4	15 ppm H_2S 40°C/90% r.H.	336 h	3x26	0	0	0
Flowing Mixed Gas FMG *IEC 60068-2-60* AEC-Q102 #C13 Test PCB: FR4	T_A = 25°C, r.H. = 75% Test method 4	500 h	3x26	0	0	0
Board Flex Test BF *AEC-Q102-002* AEC-Q102 #C14 Test PCB: FR4	2 mm	1x	3x10	0	0	0
Electrostatic Discharge HBM *ANSI/ESDA/ JEDEC JS-001* AEC-Q102 #E3 Test PCB: FR4	Human Body Model	2000 V	3x10	0	0	0

Constant Acceleration CA	*MIL-STD-750-2* AEC-Q102 #G1	Method 2006 2000 gf; 1 min in x/y/z (+/- direction)	1x	3x10	for uncasted packages only
Vibration Variable Frequency VVF	*JESD22-B103* AEC-Q102 #G2	20g, 20-2000Hz; 4min / cy; 4cy/axis service condition 1	1x	sequential samples	
Mechanical Shock MS	*JESD22-B110* AEC-Q102 #G3	1500g for 0.5ms, 5 blows, 3 orientations	1x	sequential samples	
Hermeticity HER	*JESD22-A109* AEC-Q102 #G4	Leak Test: Fine & Gross	1x	sequential samples	

Additional Tests to AEC Q102

Test Performed		Condition	Duration	Sample Size	Failures El.	Failures Opt.	Failures Vis
Electrostatic Discharge MM	*JESD22-A115* Test PCB: FR4	Machine Model	200 V	3x10	0	0	0

Failure criteria:

Electrical failures:	red:	V_f (I_f =20 mA)	> 2,3 V; ± 10% from initial value
	green:	V_f (I_f =20 mA)	> 2,4 V; ± 10% from initial value
Optical failures:		I_v (I_f =20 mA)	absolute limit: ± 50% max.
		λ_{dom} (I_f = 20 mA)	± 2 nm initial value
Visual failures:		acc JEDEC JESD22-B101	

Conclusion: The tested devices representing the product family as stated in the applies to section fulfill the reliability requirements of AEC-Q102 Initial/Rev-A.

Pre-conditioning according to Jedec Level II where applicable as per AEC-Q102 AEC-Q102 #A1 **LSG T67K (Chip C)**

Test Performed	Condition	Duration	Sample Size	Failures El. AEC-Q102 #E1	Failures Opt. AEC-Q102 #E1	Failures Vis AEC-Q102 #E0
Wet High Temperature Operating Life WHTOL1 *JESD22-A101* AEC-Q102 #A2a Test PCB: IMS-Al	T_A = 85°C; r.H. = 85%; T_s = 85°C; T_j = 105°C I_F = 15 mA $T_{on/off}$ = 30 min	1000 h	1x26	0	0	0
Wet High Temperature Operating Life WHTOL2 *JESD22-A101* AEC-Q102 #A2b Test PCB: FR4	T_A = 85°C; r.H. = 85% I_F = 5 mA	1000 h	1x26	0	0	0
Powered Temperature Cycle PTC *JESD22-A105* AEC-Q102 #A3a Test PCB: IMS-Al	T_A = -40°C/+100°C T_s = 100°C; T_j = 120°C I_F = 15 mA $t_{on/off}$ = 5 min	1000 c	1x26	0	0	0
Temperature Cycling TC *JESD22-A104* AEC-Q102 #A4a Test PCB: FR4	T_A = -40°C/+100°C 15 min each extreme	1000 c	1x26	0	0	0
High Temperature Operating Life HTOL1 *JESD22-A108* AEC-Q102 #B1a Test PCB: IMS-Al	T_A = 100°C; T_s = 100°C T_j = 120°C; I_F = 15 mA	1000 h	1x26	0	0	0
Pulsed Operating Life PLT *JESD22-A108* AEC-Q102 #B3 Test PCB: FR4	T_A = 25°C I_F = 35 mA; t_p = 0,1ms; D = 3%	1000 h	1x26	0	0	0
Dew DEW *AEC-Q102-001* AEC-Q102#C7 Test PCB: FR4	$T_{A,min}$ = 10°C $T_{A,max}$ = 80°C r.H. = 53-100%	10 c	1x26	0	0	0
Solderability SD *IEC 60068-2-58* AEC-Q102 #C10	T_A = 235°C method 2 (reflow simulation)	1x	1x10	-	-	0
Hydrogen Sulphide H2S *IEC 60068-2-43* AEC-Q102 #C12 Test PCB: FR4	15 ppm H_2S 40°C/90% r.H.	336 h	1x26	0	0	0
Flowing Mixed Gas FMG *IEC 60068-2-60* AEC-Q102 #C13 Test PCB: FR4	T_A = 25°C, r.H. = 75% Test method 4	500 h	1x26	0	0	0
Board Flex Test BF *AEC-Q102-002* AEC-Q102 #C14 Test PCB: FR4	2 mm	1x	1x10	0	0	0
Electrostatic Discharge HBM *ANSI/ESDA/ JEDEC JS-001* AEC-Q102 #E3 Test PCB: FR4	Human Body Model	2000 V	1x10	0	0	0

Constant Acceleration CA *MIL-STD-750-2* AEC-Q102 #G1	Method 2006 2000 gf; 1 min in x/y/z (+/- direction)	1x	1x10	for uncasted packages only
Vibration Variable Frequency VVF *JESD22-B103* AEC-Q102 #G2	20g, 20-2000Hz; 4min / cy; 4cy/axis service condition 1	1x	sequential samples	
Mechanical Shock MS *JESD22-B110* AEC-Q102 #G3	1500g for 0.5ms, 5 blows, 3 orientations	1x	sequential samples	
Hermeticity HER *JESD22-A109* AEC-Q102 #G4	Leak Test: Fine & Gross	1x	sequential samples	

Additional Tests to AEC Q102

Test Performed	Condition	Duration	Sample Size	Failures El.	Opt.	Vis
Electrostatic Discharge MM *JESD22-A115* Test PCB: FR4	Machine Model	200 V	1x10	0	0	0

Failure criteria:

Electrical failures:	red: V_f (I_f =2 mA)	> 2,2 V; ± 10% from initial value
	green: V_f (I_f =2 mA)	> 2,2 V; ± 10% from initial value
Optical failures:	I_v (I_f =2 mA)	absolute limit: ± 50% max.
	λ_{dom} (I_f = 2 mA)	± 2 nm initial value
Visual failures:	acc JEDEC JESD22-B101	

Conclusion: The tested devices representing the product family as stated in the applies to section fulfill the reliability requirements of AEC-Q102 Initial/Rev-A.

Pre-conditioning according to Jedec Level II where applicable as per AEC-Q102 AEC-Q102 #A1 LYG T67K (Chip C)

Test Performed	Condition	Duration	Sample Size	Failures El. AEC-Q102 #E1	Failures Opt. AEC-Q102 #E1	Failures Vis AEC-Q102 #E0
Wet High Temperature Operating Life WHTOL1 *JESD22-A101* AEC-Q102 #A2a Test PCB: IMS-Al	T_A = 85°C; r.H. = 85%; T_s = 85°C; T_j = 105°C I_F = 15 mA $T_{on/off}$ = 30 min	1000 h	2x26	0	0	0
Wet High Temperature Operating Life WHTOL2 *JESD22-A101* AEC-Q102 #A2b Test PCB: FR4	T_A = 85°C; r.H. = 85% I_F = 5 mA	1000 h	2x26	0	0	0
Powered Temperature Cycle PTC *JESD22-A105* AEC-Q102 #A3a Test PCB: IMS-Al	T_A = -40°C/+100°C T_s = 100°C; T_j = 120°C I_F = 15 mA $t_{on/off}$ = 5 min	1000 c	2x26	0	0	0
Temperature Cycling TC *JESD22-A104* AEC-Q102 #A4a Test PCB: FR4	T_A = -40°C/+100°C 15 min each extreme	1000 c	2x26	0	0	0
High Temperature Operating Life HTOL1 *JESD22-A108* AEC-Q102 #B1a Test PCB: IMS-Al	T_A = 100°C; T_s = 100°C T_j = 120°C; I_F = 15 mA	1000 h	2x26	0	0	0
Pulsed Operating Life PLT *JESD22-A108* AEC-Q102 #B3 Test PCB: FR4	T_A = 25°C I_F = 35 mA; t_p = 0,1ms; D = 3%	1000 h	2x26	0	0	0
Dew DEW *AEC-Q102-001* AEC-Q102#C7 Test PCB: FR4	$T_{A,min}$ = 10°C $T_{A,max}$ = 80°C r.H. = 53-100%	10 c	2x26	0	0	0
Solderability SD *IEC 60068-2-58* AEC-Q102 #C10	T_A = 235°C method 2 (reflow simulation)	1x	2x10	-	-	0
Hydrogen Sulphide H2S *IEC 60068-2-43* AEC-Q102 #C12 Test PCB: FR4	15 ppm H_2S 40°C/90% r.H.	336 h	2x26	0	0	0
Flowing Mixed Gas FMG *IEC 60068-2-60* AEC-Q102 #C13 Test PCB: FR4	T_A = 25°C, r.H. = 75% Test method 4	500 h	2x26	0	0	0
Board Flex Test BF *AEC-Q102-002* AEC-Q102 #C14 Test PCB: FR4	2 mm	1x	2x10	0	0	0
Electrostatic Discharge HBM *ANSI/ESDA/ JEDEC JS-001* AEC-Q102 #E3 Test PCB: FR4	Human Body Model	2000 V	2x10	0	0	0

Constant Acceleration CA *MIL-STD-750-2* AEC-Q102 #G1	Method 2006 2000 gf; 1 min in x/y/z (+/- direction)	1x	2x10	for uncasted packages only	
Vibration Variable Frequency VVF *JESD22-B103* AEC-Q102 #G2	20g, 20-2000Hz; 4min / cy; 4cy/axis service condition 1	1x	sequential samples		
Mechanical Shock MS *JESD22-B110* AEC-Q102 #G3	1500g for 0.5ms, 5 blows, 3 orientations	1x	sequential samples		
Hermeticity HER *JESD22-A109* AEC-Q102 #G4	Leak Test: Fine & Gross	1x	sequential samples		

Additional Tests to AEC Q102

Test Performed	Condition	Duration	Sample Size	Failures El.	Failures Opt.	Failures Vis
Electrostatic Discharge MM *JESD22-A115* Test PCB: FR4	Machine Model	200 V	2x10	0	0	0

Failure criteria:

Electrical failures:	yellow: V_f (I_f =2 mA)	> 2,2 V; ± 10% from initial value
	green: V_f (I_f =2 mA)	> 2,2 V; ± 10% from initial value
Optical failures:	I_v (I_f =2 mA)	absolute limit: ± 50% max.
	λ_{dom} (I_f = 2 mA)	± 2 nm initial value
Visual failures:	acc JEDEC JESD22-B101	

Conclusion: The tested devices representing the product family as stated in the applies to section fulfill the reliability requirements of AEC-Q102 Initial/Rev-A.

Pre-conditioning according to Jedec Level II where applicable as per AEC-Q102 AEC-Q102 #A1 **LSG T67K (Chip D)**

Test Performed	Condition	Duration	Sample Size	Failures El. AEC-Q102 #E1	Failures Opt. AEC-Q102 #E1	Failures Vis AEC-Q102 #E0
Wet High Temperature Operating Life WHTOL1 *JESD22-A101* AEC-Q102 #A2a Test PCB: IMS-Al	T_A = 85°C; r.H. = 85%; T_s = 85°C; T_j = 105°C I_F = 15 mA $T_{on/off}$ = 30 min	1000 h	2x26	0	0	0
Wet High Temperature Operating Life WHTOL2 *JESD22-A101* AEC-Q102 #A2b Test PCB: FR4	T_A = 85°C; r.H. = 85% I_F = 5 mA	1000 h	2x26	0	0	0
Powered Temperature Cycle PTC *JESD22-A105* AEC-Q102 #A3a Test PCB: IMS-Al	T_A = -40°C/+100°C T_s = 100°C; T_j = 120°C I_F = 15 mA $t_{on/off}$ = 5 min	1000 c	2x26	0	0	0
Temperature Cycling TC *JESD22-A104* AEC-Q102 #A4a Test PCB: FR4	T_A = -40°C/+100°C 15 min each extreme	1000 c	2x26	0	0	0
High Temperature Operating Life HTOL1 *JESD22-A108* AEC-Q102 #B1a Test PCB: IMS-Al	T_A = 100°C; T_s = 100°C T_j = 120°C; I_F = 15 mA	1000 h	2x26	0	0	0
Pulsed Operating Life PLT *JESD22-A108* AEC-Q102 #B3 Test PCB: FR4	T_A = 25°C I_F = 35 mA; t_p = 0,1ms; D = 3%	1000 h	2x26	0	0	0
Dew DEW *AEC-Q102-001* AEC-Q102#C7 Test PCB: FR4	$T_{A,min}$ = 10°C $T_{A,max}$ = 80°C r.H. = 53-100%	10 c	2x26	0	0	0
Solderability SD *IEC 60068-2-58* AEC-Q102 #C10	T_A = 235°C method 2 (reflow simulation)	1x	2x10	-	-	0
Hydrogen Sulphide H2S *IEC 60068-2-43* AEC-Q102 #C12 Test PCB: FR4	15 ppm H_2S 40°C/90% r.H.	336 h	2x26	0	0	0
Flowing Mixed Gas FMG *IEC 60068-2-60* AEC-Q102 #C13 Test PCB: FR4	T_A = 25°C, r.H. = 75% Test method 4	500 h	2x26	0	0	0
Board Flex Test BF *AEC-Q102-002* AEC-Q102 #C14 Test PCB: FR4	2 mm	1x	2x10	0	0	0
Electrostatic Discharge HBM *ANSI/ESDA/ JEDEC JS-001* AEC-Q102 #E3 Test PCB: FR4	Human Body Model	2000 V	2x10	0	0	0

Constant Acceleration CA *MIL-STD-750-2* AEC-Q102 #G1	Method 2006 2000 gf; 1 min in x/y/z (+/- direction)	1x	2x10	for uncasted packages only
Vibration Variable Frequency VVF *JESD22-B103* AEC-Q102 #G2	20g, 20-2000Hz; 4min / cy; 4cy/axis service condition 1	1x	sequential samples	
Mechanical Shock MS *JESD22-B110* AEC-Q102 #G3	1500g for 0.5ms, 5 blows, 3 orientations	1x	sequential samples	
Hermeticity HER *JESD22-A109* AEC-Q102 #G4	Leak Test: Fine & Gross	1x	sequential samples	

Additional Tests to AEC Q102

Test Performed	Condition	Duration	Sample Size	Failures El.	Failures Opt.	Failures Vis
Electrostatic Discharge MM *JESD22-A115* Test PCB: FR4	Machine Model	200 V	2x10	0	0	0

Failure criteria:

Electrical failures:	red: V_f (I_f =2 mA)	> 2,2 V; ± 10% from initial value
	green: V_f (I_f =2 mA)	> 2,2 V; ± 10% from initial value
Optical failures:	I_v (I_f =2 mA)	absolute limit: ± 50% max.
	λ_{dom} (I_f = 2 mA)	± 2 nm initial value
Visual failures:	acc JEDEC JESD22-B101	

Conclusion: The tested devices representing the product family as stated in the applies to section fulfill the reliability requirements of AEC-Q102 Initial/Rev-A.

Pre-conditioning according to Jedec Level II where applicable as per AEC-Q102 AEC-Q102 #A1 **LYG T67K (Chip C)**

Test Performed	Condition	Duration	Sample Size	Failures El. AEC-Q102 #E1	Failures Opt. AEC-Q102 #E1	Failures Vis AEC-Q102 #E0
Wet High Temperature Operating Life WHTOL1 *JESD22-A101* AEC-Q102 #A2a Test PCB: IMS-Al	T_A = 85°C; r.H. = 85%; T_s = 85°C; T_j = 105°C I_F = 15 mA $T_{on/off}$ = 30 min	1000 h	1x26	0	0	0
Wet High Temperature Operating Life WHTOL2 *JESD22-A101* AEC-Q102 #A2b Test PCB: FR4	T_A = 85°C; r.H. = 85% I_F = 5 mA	1000 h	1x26	0	0	0
Powered Temperature Cycle PTC *JESD22-A105* AEC-Q102 #A3a Test PCB: IMS-Al	T_A = -40°C/+100°C T_s = 100°C; T_j = 120°C I_F = 15 mA $t_{on/off}$ = 5 min	1000 c	1x26	0	0	0
Temperature Cycling TC *JESD22-A104* AEC-Q102 #A4a Test PCB: FR4	T_A = -40°C/+100°C 15 min each extreme	1000 c	1x26	0	0	0
High Temperature Operating Life HTOL1 *JESD22-A108* AEC-Q102 #B1a Test PCB: IMS-Al	T_A = 100°C; T_s = 100°C T_j = 120°C; I_F = 15 mA	1000 h	1x26	0	0	0
Pulsed Operating Life PLT *JESD22-A108* AEC-Q102 #B3 Test PCB: FR4	T_A = 25°C I_F = 35 mA; t_p = 0,1ms; D = 3%	1000 h	1x26	0	0	0
Dew DEW *AEC-Q102-001* AEC-Q102#C7 Test PCB: FR4	$T_{A,min}$ = 10°C $T_{A,max}$ = 80°C r.H. = 53-100%	10 c	1x26	0	0	0
Solderability SD *IEC 60068-2-58* AEC-Q102 #C10	T_A = 235°C method 2 (reflow simulation)	1x	1x10	-	-	0
Hydrogen Sulphide H2S *IEC 60068-2-43* AEC-Q102 #C12 Test PCB: FR4	15 ppm H_2S 40°C/90% r.H.	336 h	1x26	0	0	0
Flowing Mixed Gas FMG *IEC 60068-2-60* AEC-Q102 #C13 Test PCB: FR4	T_A = 25°C, r.H. = 75% Test method 4	500 h	1x26	0	0	0
Board Flex Test BF *AEC-Q102-002* AEC-Q102 #C14 Test PCB: FR4	2 mm	1x	1x10	0	0	0
Electrostatic Discharge HBM *ANSI/ESDA/ JEDEC JS-001* AEC-Q102 #E3 Test PCB: FR4	Human Body Model	2000 V	1x10	0	0	0

Constant Acceleration CA *MIL-STD-750-2* AEC-Q102 #G1	Method 2006 2000 gf; 1 min in x/y/z (+/- direction)	1x	1x10	for uncasted packages only
Vibration Variable Frequency VVF *JESD22-B103* AEC-Q102 #G2	20g, 20-2000Hz; 4min / cy; 4cy/axis service condition 1	1x	sequential samples	
Mechanical Shock MS *JESD22-B110* AEC-Q102 #G3	1500g for 0.5ms, 5 blows, 3 orientations	1x	sequential samples	
Hermeticity HER *JESD22-A109* AEC-Q102 #G4	Leak Test: Fine & Gross	1x	sequential samples	

Additional Tests to AEC Q102

Test Performed	Condition	Duration	Sample Size	Failures El.	Opt.	Vis
Electrostatic Discharge MM *JESD22-A115* Test PCB: FR4	Machine Model	200 V	1x10	0	0	0

Failure criteria:

Electrical failures:	yellow: V_f (I_f =2 mA)	> 2,2 V; ± 10% from initial value
	green: V_f (I_f =2 mA)	> 2,2 V; ± 10% from initial value
Optical failures:	I_v (I_f =2 mA)	absolute limit: ± 50% max.
	λ_{dom} (I_f = 2 mA)	± 2 nm initial value
Visual failures:	acc JEDEC JESD22-B101	

Conclusion: The tested devices representing the product family as stated in the applies to section fulfill the reliability requirements of AEC-Q102 Initial/Rev-A.

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1. The Data and curves shown in this Document are based on experiments carried out under laboratory conditions on a random sample size of LED/IRED/Laser/Detector with readouts at discrete readout times (where applicable). Thus, the Data above represent a limited number of production lots only and may differ between different assembly lots over time (including chip or package changes). Thus, the behavior of the LED/IRED/Laser/Detector in the final application may differ from the Data. The behavior of the LED/IRED/Laser/Detector at conditions or readout times deviating from those stated above may not be deduced from the Data.
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