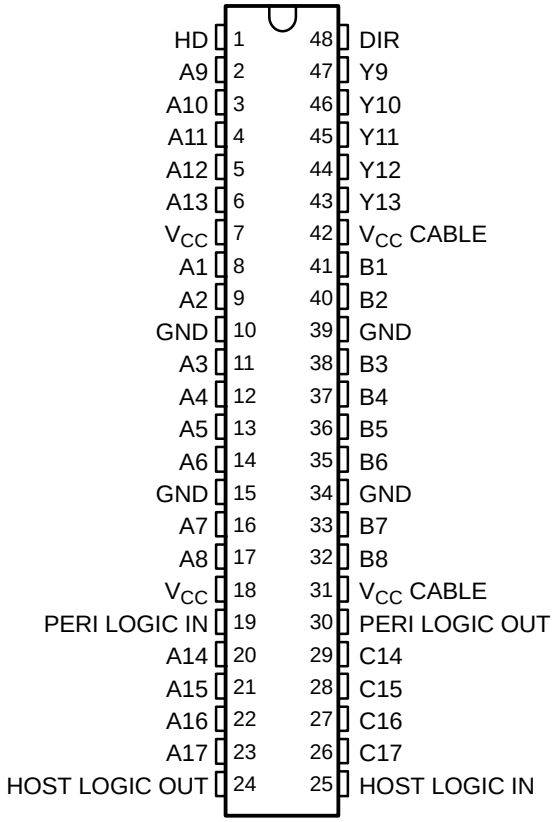
SN74LVCZ161284A
19-BIT IEEE STD 1284 TRANSLATION TRANSCEIVER WITH ERROR-FREE POWER UP

SCES358B – SEPTEMBER 2001 – REVISED MAY 2005

FEATURES

- **Power-On Reset (POR) Prevents Printer Errors When Printer Is Turned On, But No Valid Signal Is at Pins A9–A13**
- **Operates From 3 V to 3.6 V**
- **1.4-kΩ Pullup Resistors Integrated on All Open-Drain Outputs Eliminate the Need for Discrete Resistors**
- **Designed for IEEE Std 1284-I (Level-1 Type) and IEEE Std 1284-II (Level-2 Type) Electrical Specifications**
- **Flow-Through Architecture Optimizes PCB Layout**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **– 4000-V Human-Body Model (A114-A)**
  - **– 350-V Machine Model (A115-A)**
  - **– 1500-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74LVCZ161284A is designed for 3-V to 3.6-V V_{CC} operation. This device provides asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

This device has eight bidirectional bits; data can flow in the A-to-B direction when the direction-control (DIR) input is high and in the B-to-A direction when DIR is low. This device also has five drivers that drive the cable side and four receivers. The SN74LVCZ161284A has one receiver dedicated to the HOST LOGIC line and a driver to drive the PERI LOGIC line.

The output drive mode is determined by the high-drive (HD) control pin. When HD is high, the outputs are in a totem-pole configuration and in an open-drain configuration when HD is low. This meets the drive requirements as specified in the IEEE Std 1284-I (level-1 type) and IEEE Std 1284-II (level-2 type) parallel peripheral-interface specifications. Except for HOST LOGIC IN and peripheral logic out (PERI LOGIC OUT), all cable-side pins have a 1.4-kΩ integrated pullup resistor. The pullup resistor is switched off if the associated output driver is in the low state or if the output voltage is above V_{CC} CABLE. If V_{CC} CABLE is off, PERI LOGIC OUT is set to low.

The device has two supply voltages. V_{CC} is designed for 3-V to 3.6-V operation. V_{CC} CABLE supplies the inputs and output buffers of the cable side only and is designed for 3-V to 3.6-V and for 4.7-V to 5.5-V operation. Even when V_{CC} CABLE is 3 V to 3.6 V, the cable-side I/O pins are 5-V tolerant.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TSSOP – DGG	Tape and reel	SN74LVCZ161284AGR	LVCZ161284A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

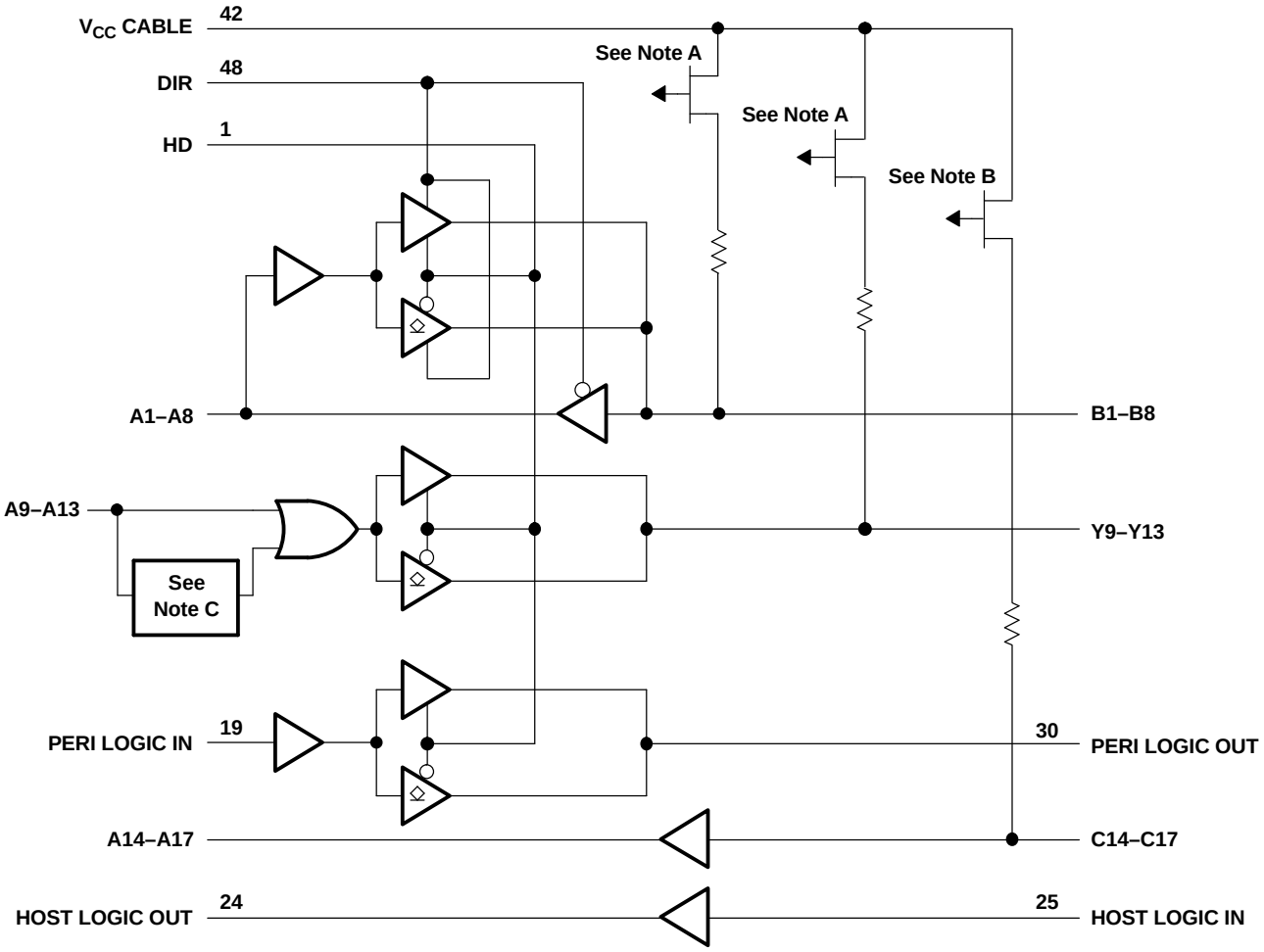
DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The power-on reset (POR) ensures that the Y outputs (Y9–Y13) stay in the high state after power on until an associated input (A9–A13) goes high. When an associated input goes high, all Y outputs are activated, and noninverting signals of the associated inputs are driven through Y outputs. This special feature prevents printer system errors caused by deasserting the BUSY signal in the cable at power on.

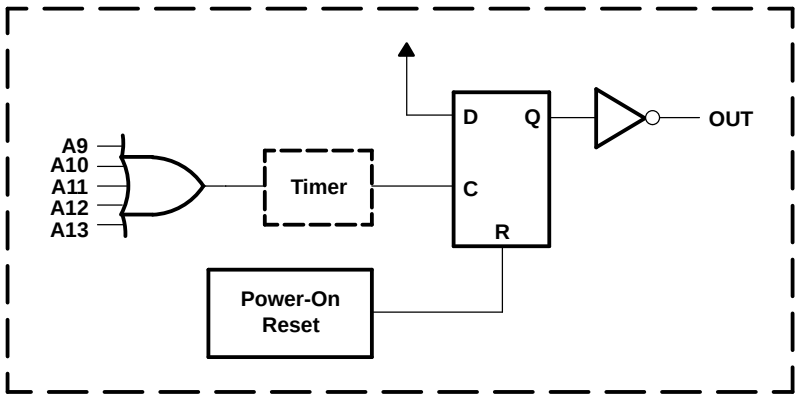
FUNCTION TABLE

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A9–A13 to Y9–Y13 and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	B1–B8 to A1–A8 and C14–C17 to A14–A17
L	H	Totem pole	B1–B8 to A1–A8, A9–A13 to Y9–Y13, PERI LOGIC IN to PERI LOGIC OUT, and C14–C17 to A14–A17
H	L	Open drain	A1–A8 to B1–B8, A9–A13 to Y9–Y13, and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	C14–C17 to A14–A17
H	H	Totem pole	A1–A8 to B1–B8, A9–A13 to Y9–Y13, C14–C17 to A14–A17, and PERI LOGIC IN to PERI LOGIC OUT

LOGIC DIAGRAM



NOTES: A. The PMOS transistors prevent backdriving current from the signal pins to V_{CC} CABLE when V_{CC} CABLE is open or at GND. The PMOS transistor is turned off when the associated driver is in the low state.
B. The PMOS transistor prevents backdriving current from the signal pins to V_{CC} CABLE when V_{CC} CABLE is open or at GND.
C. Active input detection circuit forces Y9–Y13 to the high state after power on, until one of the A9–A13 pins goes high (see below).



Active Input Detection Circuit

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} CABLE	Supply voltage range		–0.5	7	V
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I / V_O	Input and output voltage range	Cable side(2)(3)	–2	7	V
		Peripheral side(2)	–0.5	V_{CC} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	Except PERI LOGIC OUT		±50	mA
		PERI LOGIC OUT		±100	
	Continuous current through each V_{CC} or GND			±200	mA
I_{SK}	Output high sink current	V_O = 5.5 V and V_{CC} CABLE = 3 V		65	mA
θ_{JA}	Package thermal impedance(4)			70	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The ac input voltage pulse duration is limited to 40 ns if the amplitude is greater than –0.5 V.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC} CABLE	Supply voltage for the cable side, V_{CC} CABLE ≥ V_{CC}		3	5.5	V
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage	A, B, DIR, and HD	2		V
		C14–C17	2.3		
		HOST LOGIC IN	2.6		
		PERI LOGIC IN	2		
V_{IL}	Low-level input voltage	A, B, DIR, and HD		0.8	V
		C14–C17		0.8	
		HOST LOGIC IN		1.6	
		PERI LOGIC IN		0.8	
V_I	Input voltage	Peripheral side	0	V_{CC}	V
		Cable side	0	5.5	
V_O	Open-drain output voltage	HD low	0	5.5	V
I_{OH}	High-level output current	HD high, B and Y outputs		–14	mA
		A outputs and HOST LOGIC OUT		–4	
		PERI LOGIC OUT		–0.5	
I_{OL}	Low-level output current	B and Y outputs		14	mA
		A outputs and HOST LOGIC OUT		4	
		PERI LOGIC OUT		84	
T_A	Operating free-air temperature		0	70	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range, V_{CC} CABLE = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
ΔV_t Hysteresis ($V_{T+} - V_{T-}$)	All inputs except C inputs and HOST LOGIC IN		3.3 V	0.4			V
	HOST LOGIC IN			0.2			
	C inputs			0.8			
V_{OH}	HD high, B and Y outputs	I_{OH} = –14 mA	3 V	2.23			V
			3.3 V(2)	2.4			
	HD high, A outputs, and HOST LOGIC OUT	I_{OH} = –4 mA	3 V	2.4			
		I_{OH} = –50 µA		2.8			
	PERI LOGIC OUT	I_{OH} = –0.5 mA	3.15 V	3.1			
			3.3 V(2)	4.5			
V_{OL}	B and Y outputs	I_{OL} = 14 mA	3 V			0.77	V
	A outputs and HOST LOGIC OUT	I_{OL} = 50 µA				0.2	
		I_{OL} = 4 mA				0 4	
	PERI LOGIC OUT	I_{OL} = 84 mA				0.9	
I_I	C inputs	$V_I = V_{CC}$	3.6 V(3)			50	µA
		V_I = GND (pullup resistors)				–3.5	mA
	All inputs except B or C inputs	$V_I = V_{CC}$ or GND	3.6 V			±1	µA
I_{OZ}	A1–A8	$V_O = V_{CC}$ or GND	3.6 V			±20	µA
	B outputs	$V_O = V_{CC}$ CABLE	3.6 V			50	µA
		V_O = GND (pullup resistors)	3.6 V(3)			–3.5	mA
	Open-drain Y outputs	V_O = GND (pullup resistors)	3.6 V(3)			–3.5	mA
I_{OZPU}	B and Y outputs	V_O = 5.5 V	0 to 1.5 V(4)			350	µA
		V_O = GND				–5	mA
I_{OZPD}	B and Y outputs	V_O = 5.5 V	0 to 1.5 V(4)			350	µA
		V_O = GND				–5	mA
I_{off}	Power-down input leakage, except A1–A8 or B1–B8 inputs	V_I or V_O = 0 to 3.6 V	0(3)			100	µA
	Power-down output leakage, B1–B8 and Y9–Y13 outputs	V_I or V_O = 0 to 5.5 V				100	
I_{CC}		V_I = GND (12 × pullup)	3.6 V(5)			45	mA
			3.6 V			70	
		$V_I = V_{CC}$, I_O = 0	3.6 V			0.8	
C_i	All inputs	$V_I = V_{CC}$ or GND	3.3 V		3		pF
C_{io}	I/O ports	$V_O = V_{CC}$ or GND	3.3 V		7		pF
Z_O	Cable side	I_{OH} = –35 mA	3.3 V		45		Ω
R pullup	Cable side	V_O = 0 V (in high-impedance state)	3.3 V	1.15		1.65	kΩ

(1) Typical values are measured at V_{CC} = 3.3 V, V_{CC} CABLE = 5 V, and T_A = 25°C.
(2) V_{CC} CABLE = 4.7 V
(3) V_{CC} CABLE = 3.6 V
(4) Connect the V_{CC} pin and the V_{CC} CABLE pin.
(5) V_{CC} CABLE = 4.7 V

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2 and Figure 3)

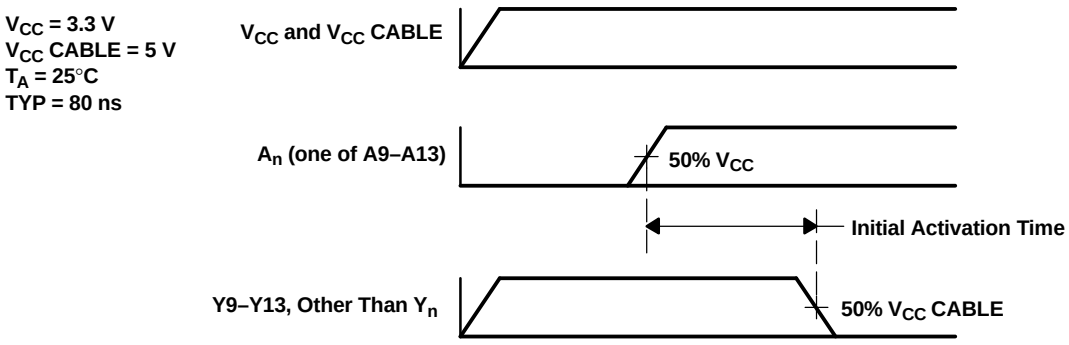
PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Totem pole	A1–A8	B1–B8	1		22	ns
t_{PHL}				1		22	
t_{PLH}	Totem pole	A9–A13	Y9–Y13	1		20	ns
t_{PHL}				1		20	
t_{PLH}	Totem pole	B1–B8	A1–A8	1		10	ns
t_{PHL}				1		10	
t_{PLH}	Totem pole	C14–C17	A14–A17	1		11	ns
t_{PHL}				1		11	
t_{PLH}	Totem pole	PERI LOGIC IN	PERI LOGIC OUT	1		13	ns
t_{PHL}				1		13	
t_{PLH}	Totem pole	HOST LOGIC IN	HOST LOGIC OUT	1		13	ns
t_{PHL}				1		13	
t_{slew}	Totem pole	B1–B8 and Y9–Y13 outputs		0.05		0.4	V/ns
t_{PZH}		HD	B1–B8, Y9–Y13, and PERI LOGIC OUT	1		20	ns
t_{PHZ}				1		15	
t_{en}–t_{dis}		DIR	A1–A8	1		15	ns
t_{PHZ}		DIR	B1–B8	1		15	ns
t_{PLZ}				1		15	
t_r, t_f	Open drain	A1–A13	B1–B8 or Y9–Y13	1		120	ns
$t_{sk(o)}$ (2)		A1–A8 or B1–B8	B1–B8 or A1–A8		2.5	10	ns

(1) Typical values are measured at V_{CC} = 3.3 V, V_{CC} CABLE = 5 V, and T_A = 25°C.
(2) Skew is measured at 1/2 (V_{OH} + V_{OL}) for signals switching in the same direction.

Operating Characteristics

V_{CC} = 3.3 V, T_A = 25°C

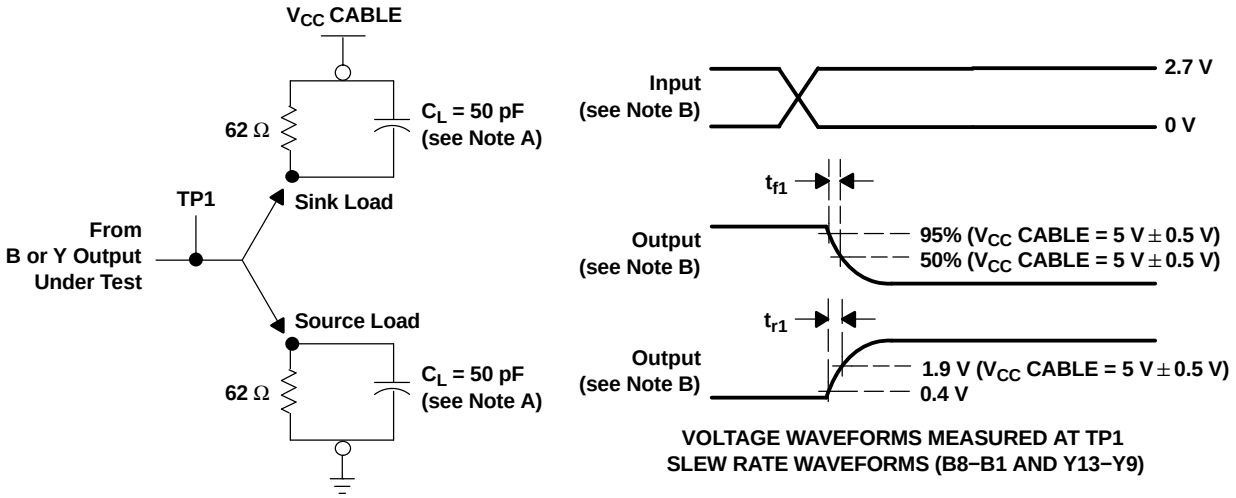
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0,	f = 10 MHz	45	pF



One of pins A9–A13 is switched as shown above, and the other four inputs are forced at low state.

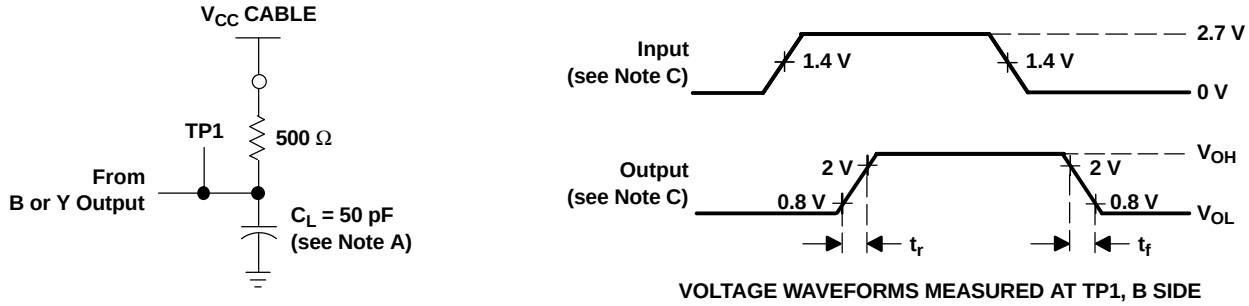
Figure 1. Error-Free Circuit Timing

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS MEASURED AT TP1
SLEW RATE WAVEFORMS (B8–B1 AND Y13–Y9)

SLEW RATE A-TO-B OR A-TO-Y LOAD (TOTEM POLE)



VOLTAGE WAVEFORMS MEASURED AT TP1, B SIDE

A-TO-B LOAD OR A-TO-Y LOAD (OPEN DRAIN)

NOTES: A. C_L includes probe and jig capacitance.

B. When V_{CC} CABLE is 3.3 V ± 0.3 V, slew rate is measured between 0.4 V and 0.9 V for the rising edge and between 2.4 V and 1.9 V for the falling edge. When V_{CC} CABLE is 5 V ± 0.5 V, slew rate is measured between 0.4 V and 1.9 V for the rising edge and between 95% V_{CC} CABLE and 50% V_{CC} CABLE for the falling edge.

$$t_{slew}\,\text{fall} = V_{CC}\left(\frac{95\% - 50\%}{t_{f1}}\right) \qquad t_{slew}\,\text{rise} = \left(\frac{1.9\ \text{V} - 0.4\ \text{V}}{t_{r1}}\right)$$

C. Input rise (t_r) and fall (t_f) times are 3 ns. Rise and fall times (open drain) are <120 ns.

D. The outputs are measured one at a time, with one transition per measurement.

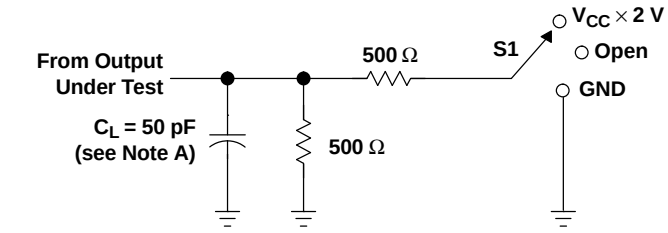
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuits and Voltage Waveforms

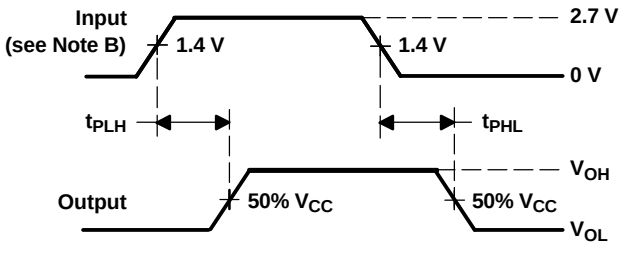
PARAMETER MEASUREMENT INFORMATION



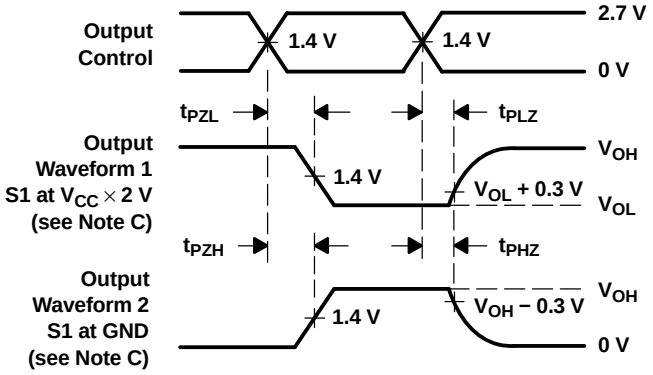
LOAD CIRCUIT

When Measuring the Cable Side, V_{CC} CABLE × 2 V

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$V_{CC} \times 2$ V
t_{PHZ}/t_{PZH}	GND

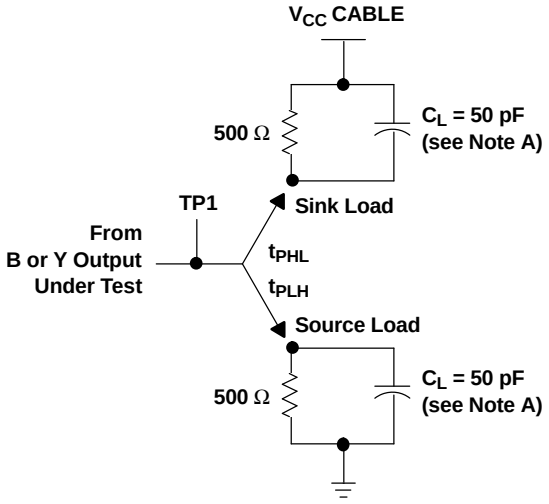


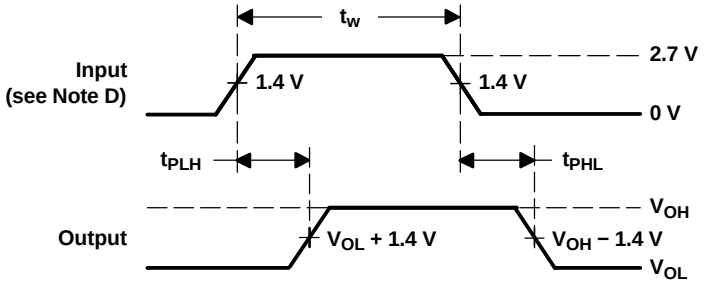
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

B-TO-A LOAD (TOTEM POLE)





VOLTAGE WAVEFORMS MEASURED AT TP1
PROPAGATION DELAY TIMES (A to B)

A-TO-B LOAD OR A-TO-Y LOAD (TOTEM POLE)

NOTES: A. C_L includes probe and jig capacitance.
B. Input rise and fall times are 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. Input rise and fall times are 3 ns. Pulse duration is 150 ns < t_w < 10 µs.
E. The outputs are measured one at a time, with one transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCZ161284AGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LVCZ161284A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

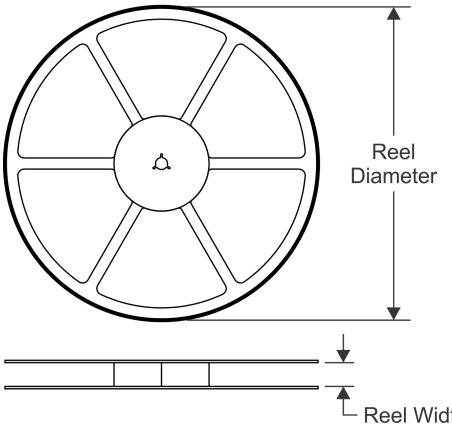
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

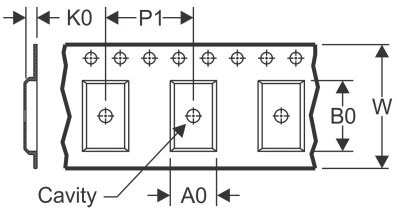
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

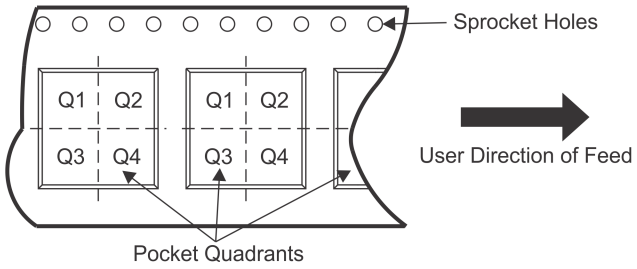


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

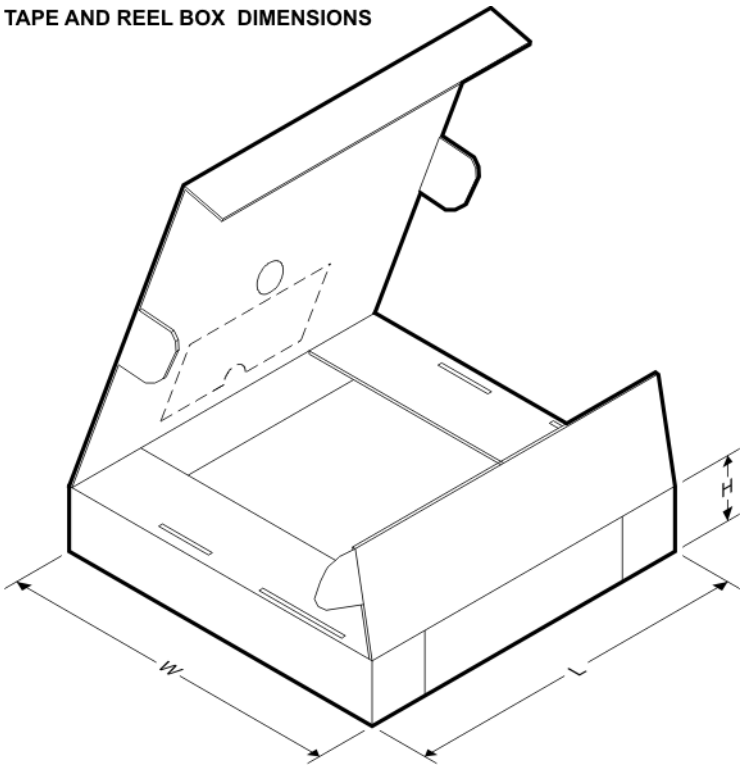
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

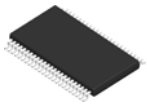
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCZ161284AGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCZ161284AGR	TSSOP	DGG	48	2000	367.0	367.0	45.0

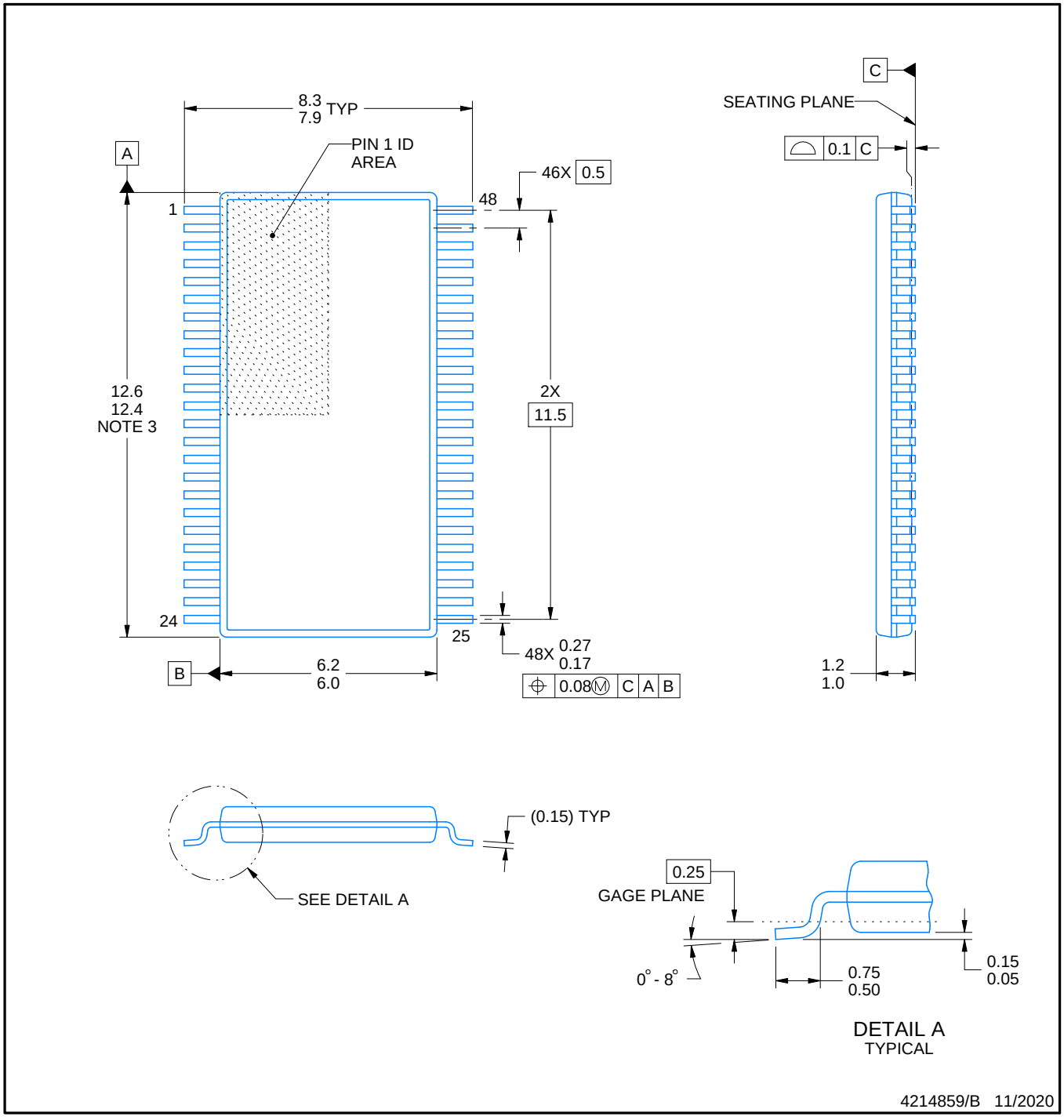


PACKAGE OUTLINE

DGG0048A

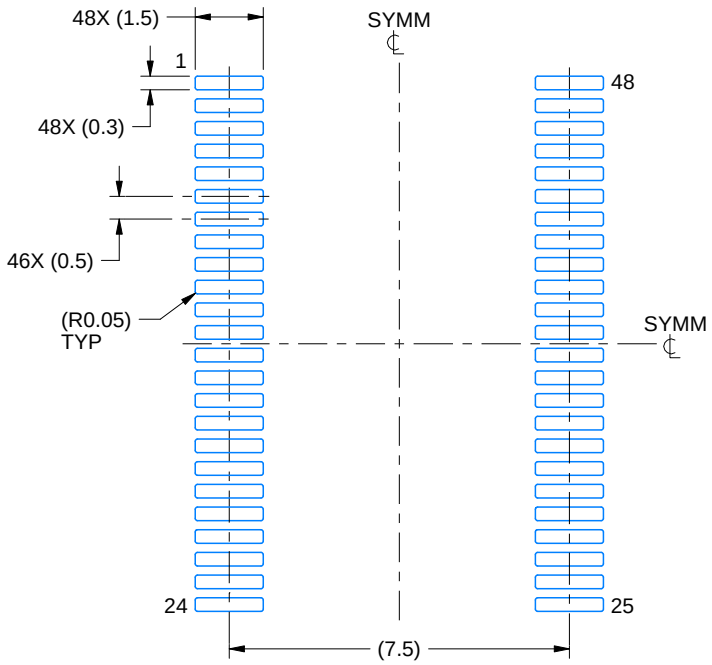
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

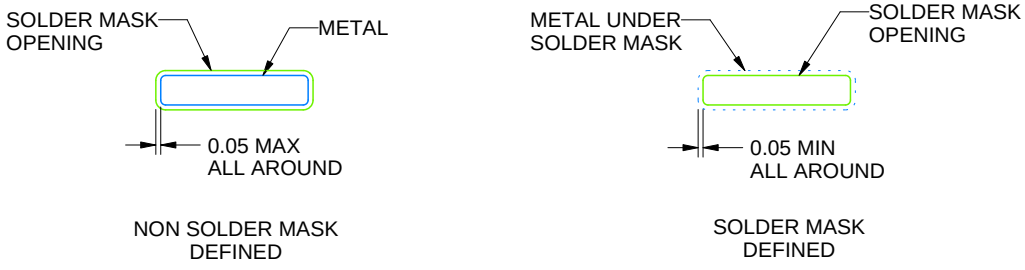


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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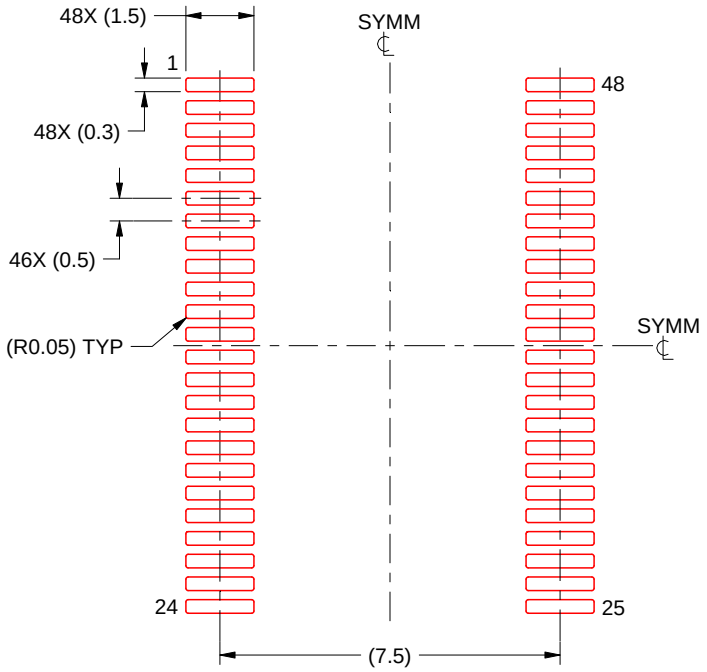
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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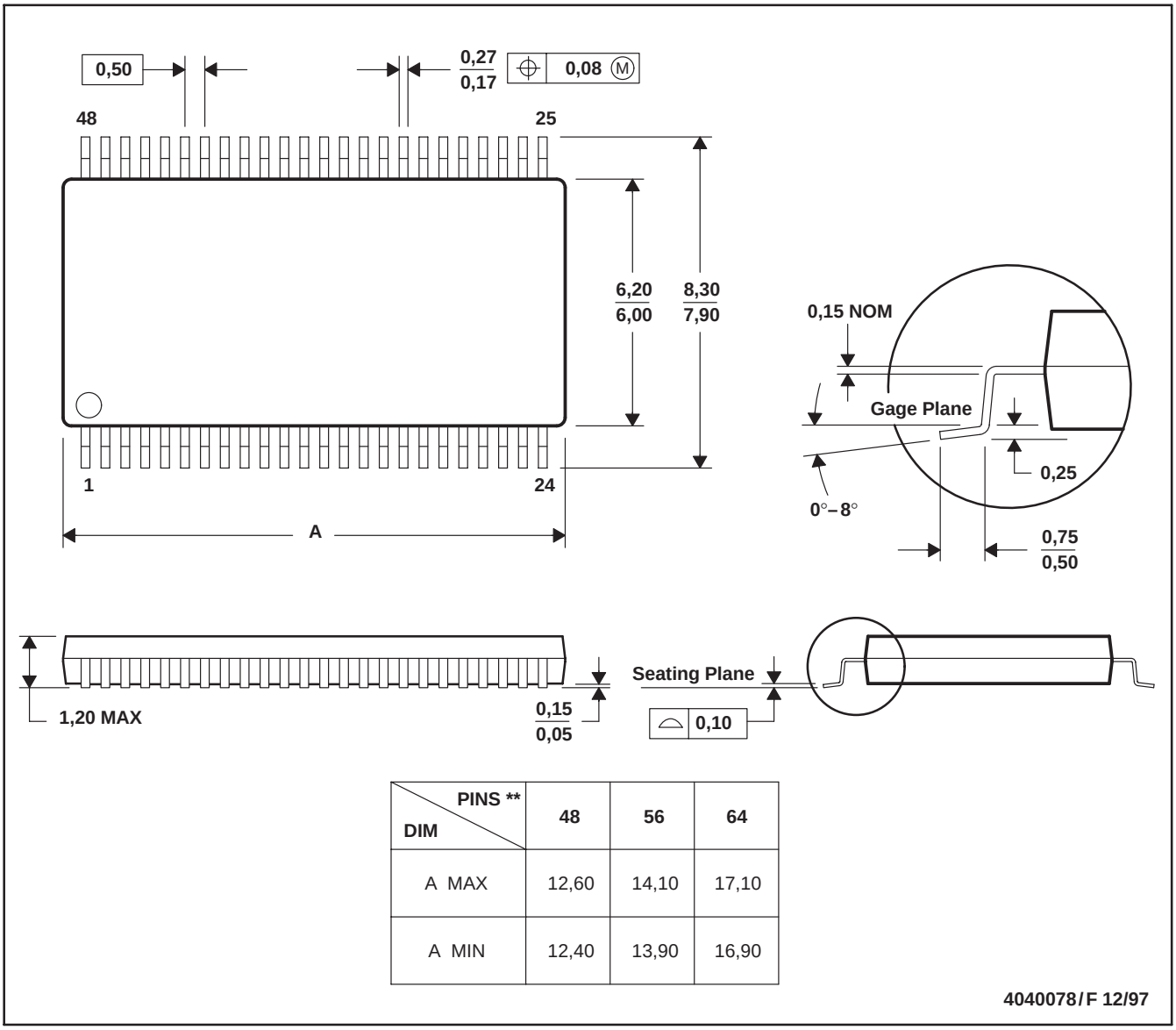
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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