

Features

- Fast Read Access Time - 150 ns
- Fast Byte Write - 200 μ s or 1 ms
- Self-Timed Byte Write Cycle
 - Internal Address and Data Latches
 - Internal Control Timer
 - Automatic Clear Before Write
- Direct Microprocessor Control
 - DATA POLLING
 - READY/BUSY Open Drain Output
- Low Power
 - 30 mA Active Current
 - 100 μ A CMOS Standby Current
- High Reliability
 - Endurance: 10^4 or 10^5 Cycles
 - Data Retention: 10 Years
- 5V \pm 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

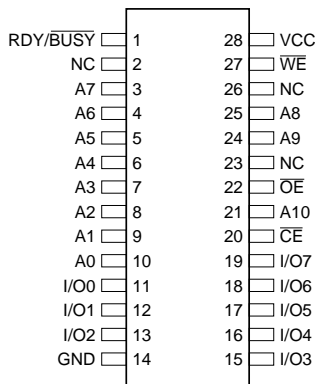
The AT28C17 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C17 is a 16K memory organized as 2,048 words by 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

(continued)

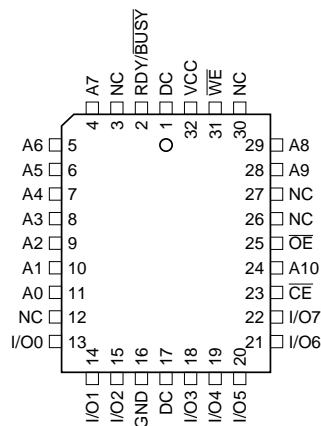
Pin Configurations

| Pin Name | Function |
|-------------------------------|---------------------|
| A0 - A10 | Addresses |
| $\overline{\text{CE}}$ | Chip Enable |
| $\overline{\text{OE}}$ | Output Enable |
| $\overline{\text{WE}}$ | Write Enable |
| I/O0 - I/O7 | Data Inputs/Outputs |
| RDY/ $\overline{\text{BUSY}}$ | Ready/Busy Output |
| NC | No Connect |
| DC | Don't Connect |

PDIP, SOIC
Top View



PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.



16K (2K x 8)
Parallel
EEPROMs

AT28C17

Rev. 0541B-10/98

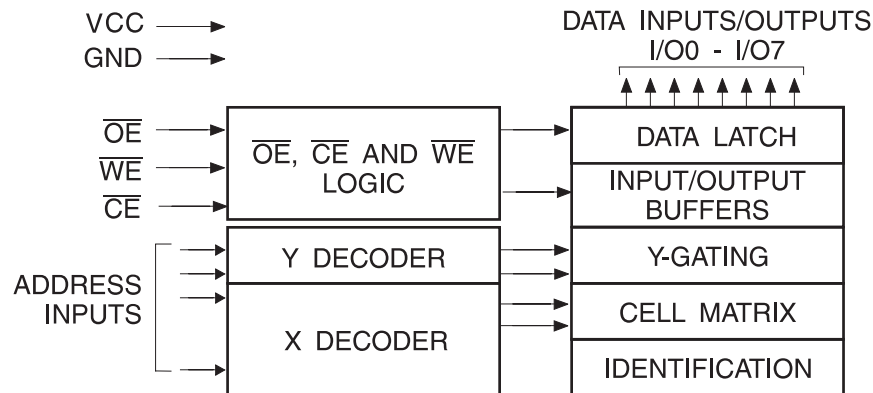


The AT28C17 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/BUSY and DATA POLLING of I/O₇. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 μA.

Atmel's 28C17 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of EEPROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

| | |
|--|--------------------------|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| All Input Voltages (including NC Pins) with Respect to Ground | -0.6V to +6.25V |
| All Output Voltages with Respect to Ground | -0.6V to $V_{CC} + 0.6V$ |
| Voltage on \overline{OE} and A9 with Respect to Ground | -0.6V to +13.5V |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C17 is accessed like a Static RAM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever \overline{CE} or \overline{OE} is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C17 is similar to writing into a Static RAM. A low pulse on the \overline{WE} or \overline{CE} input with \overline{OE} high and \overline{CE} or \overline{WE} low (respectively) initiates a byte write. The address location is latched on the last falling edge of \overline{WE} (or \overline{CE}); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC} , a read operation will effectively be a polling operation.

FAST BYTE WRITE: The AT28C17E offers a byte write time of 200 μ s maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

READY/BUSY: Pin 1 is an open drain $\overline{RDY}/\overline{BUSY}$ output that can be used to detect the end of a write cycle. $\overline{RDY}/\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain

connection allows for OR-tying of several devices to the same $\overline{RDY}/\overline{BUSY}$ line.

DATA POLLING: The AT28C17 provides \overline{DATA} POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power on delay once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit—holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C17 may be set to the high state by the CHIP CLEAR operation. By setting \overline{CE} low and \overline{OE} to 12 volts, the chip is cleared when a 10 msec low pulse is applied to \overline{WE} .

DEVICE IDENTIFICATION: An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to $12 \pm 0.5V$ and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.



DC and AC Operating Range

| | | AT28C17-15 |
|------------------------------|------|--------------|
| Operating Temperature (Case) | Com. | 0°C - 70°C |
| | Ind. | -40°C - 85°C |
| V _{CC} Power Supply | | 5V ± 10% |

Operating Modes

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | I/O |
|-----------------------|-----------------|-------------------------------|-----------------|------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | D _{OUT} |
| Write ⁽²⁾ | V _{IL} | V _{IH} | V _{IL} | D _{IN} |
| Standby/Write Inhibit | V _{IH} | X ⁽¹⁾ | X | High Z |
| Write Inhibit | X | X | V _{IH} | |
| Write Inhibit | X | V _{IL} | X | |
| Output Disable | X | V _{IH} | X | High Z |
| Chip Erase | V _{IL} | V _H ⁽³⁾ | V _{IL} | High Z |

- Notes:
1. X can be V_{IL} or V_{IH}.
 2. Refer to AC Programming Waveforms.
 3. V_H = 12.0V ± 0.5V.

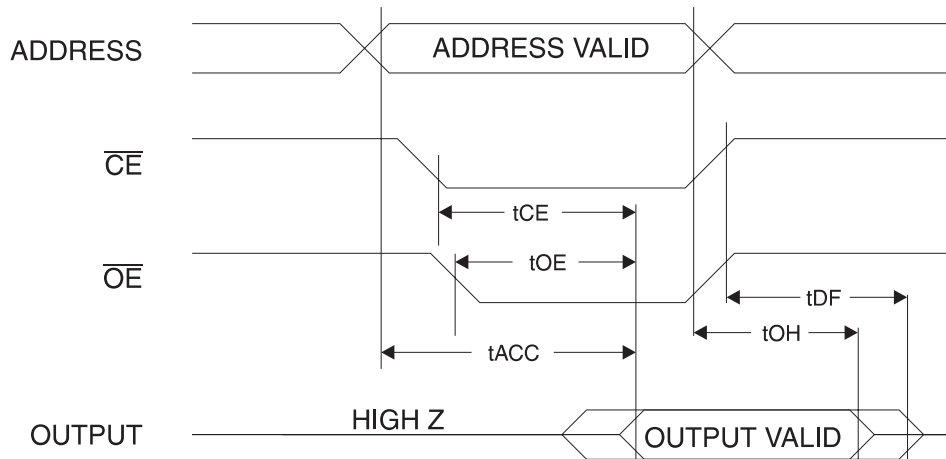
DC Characteristics

| Symbol | Parameter | Condition | Min | Max | Units |
|------------------|--------------------------------------|--|------|-----|-------|
| I _{LI} | Input Load Current | V _{IN} = 0V to V _{CC} + 1V | | 10 | μA |
| I _{LO} | Output Leakage Current | V _{I/O} = 0V to V _{CC} | | 10 | μA |
| I _{SB1} | V _{CC} Standby Current CMOS | $\overline{CE} = V_{CC} - 0.3V$ to V _{CC} + 1.0V | | 100 | μA |
| I _{SB2} | V _{CC} Standby Current TTL | $\overline{CE} = 2.0V$ to V _{CC} + 1.0V | Com. | 2 | mA |
| | | | Ind. | 3 | mA |
| I _{CC} | V _{CC} Active Current AC | f = 5 MHz; I _{OUT} = 0 mA $\overline{CE} = V_{IL}$ | Com. | 30 | mA |
| | | | Ind. | 45 | mA |
| V _{IL} | Input Low Voltage | | | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.0 | | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1 mA = 4.0 for RDY/ \overline{BUSY} | | .4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -400 μA | 2.4 | | V |

AC Read Characteristics

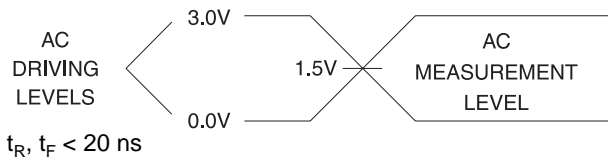
| Symbol | Parameter | AT28C17-15 | | Units |
|-------------------|---|------------|-----|-------|
| | | Min | Max | |
| t_{ACC} | Address to Output Delay | | 150 | ns |
| $t_{CE}^{(1)}$ | \overline{CE} to Output Delay | | 150 | ns |
| $t_{OE}^{(2)}$ | \overline{OE} to Output Delay | 10 | 70 | ns |
| $t_{DF}^{(3)(4)}$ | \overline{CE} or \overline{OE} High to Output Float | 0 | 50 | ns |
| t_{OH} | Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first | 0 | | ns |

AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

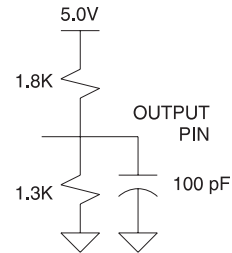


- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first ($C_L = 5 \text{ pF}$).
 - This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

$f = 1 \text{ MHz}, T = 25^\circ\text{C}^{(1)}$

| Symbol | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 4 | 6 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 8 | 12 | pF | $V_{OUT} = 0V$ |

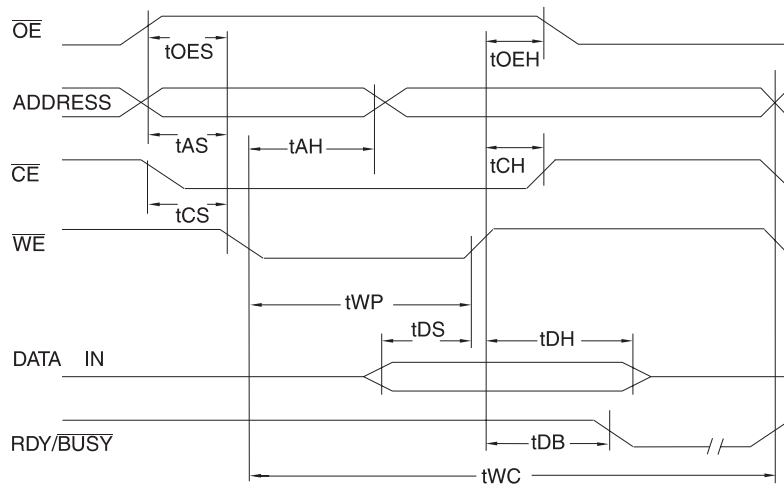
- Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

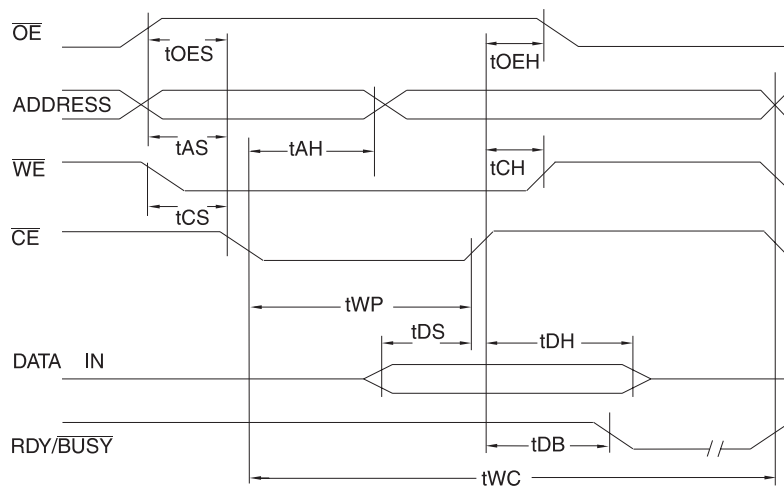
| Symbol | Parameter | Min | Typ | Max | Units |
|-------------------|--|----------|-----|------|---------|
| t_{AS}, t_{OES} | Address, \overline{OE} Set-up Time | 10 | | | ns |
| t_{AH} | Address Hold Time | 50 | | | ns |
| t_{WP} | Write Pulse Width (\overline{WE} or \overline{CE}) | 100 | | 1000 | ns |
| t_{DS} | Data Set-up Time | 50 | | | ns |
| t_{DH}, t_{OEH} | Data, \overline{OE} Hold Time | 10 | | | ns |
| t_{CS}, t_{CH} | \overline{CE} to \overline{WE} and \overline{WE} to \overline{CE} Set-up and Hold Time | 0 | | | ns |
| t_{DB} | Time to Device Busy | | | 50 | ns |
| t_{WC} | Write Cycle Time | AT28C17 | 0.5 | 1.0 | ms |
| | | AT28C17E | 100 | 200 | μ s |

AC Write Waveforms

\overline{WE} Controlled



\overline{CE} Controlled

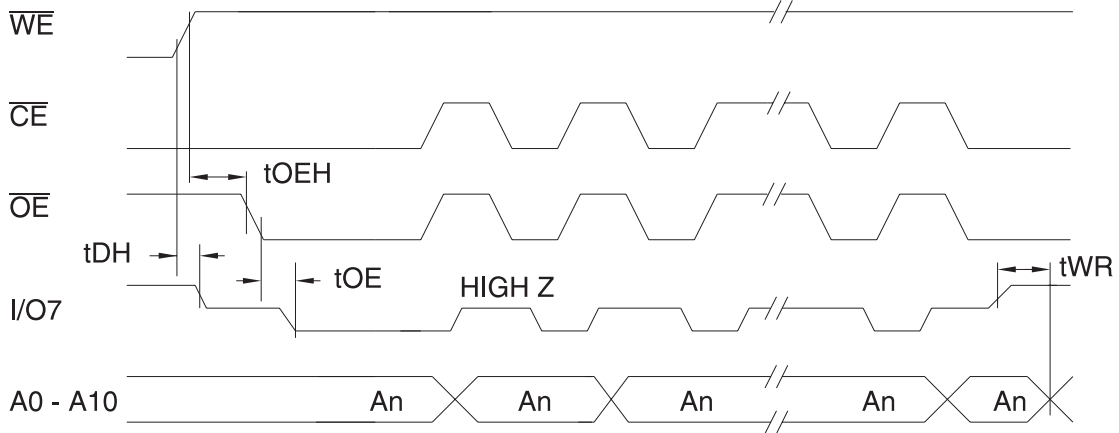


Data Polling Characteristics⁽¹⁾

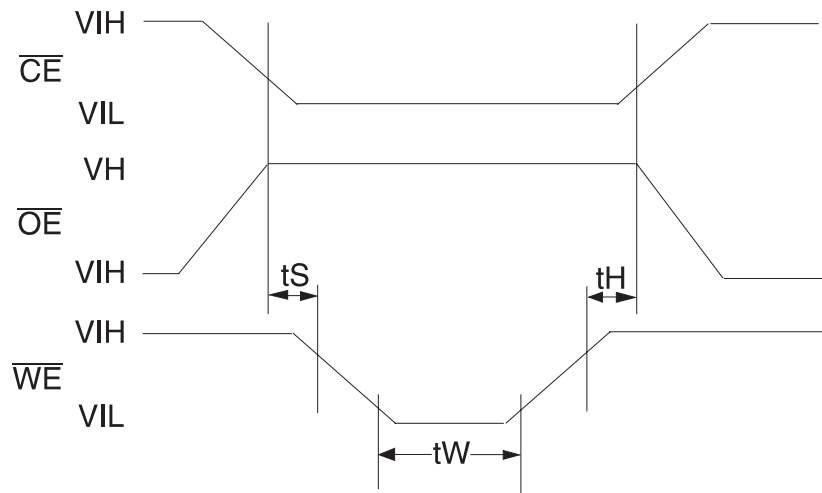
| Symbol | Parameter | Min | Typ | Max | Units |
|-----------------|---|-----|-----|-----|-------|
| t_{DH} | Data Hold Time | 10 | | | ns |
| $t_{OE\bar{H}}$ | $\bar{O}\bar{E}$ Hold Time | 10 | | | ns |
| t_{OE} | $\bar{O}\bar{E}$ to Output Delay ⁽²⁾ | | | | ns |
| t_{WR} | Write Recovery Time | 0 | | | ns |

Notes: 1. These parameters are characterized and not 100% tested.
 2. See AC Read Characteristics.

Data Polling Waveforms

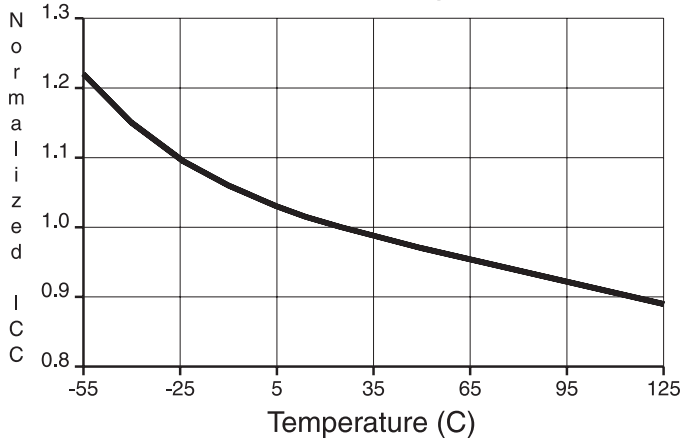


Chip Erase Waveforms

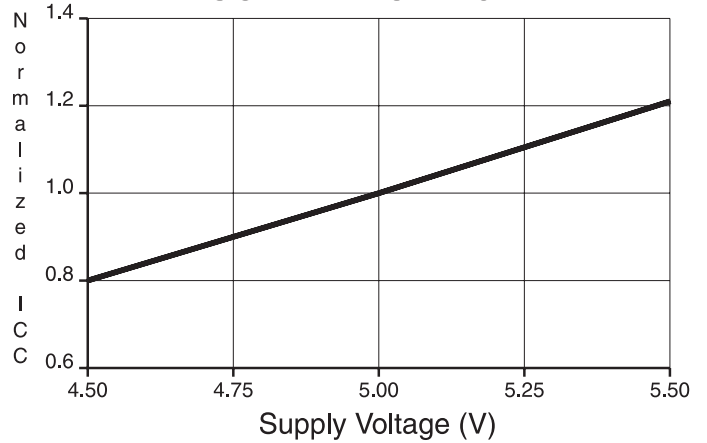


$t_S = t_H = 1 \mu\text{sec (min.)}$
 $t_W = 10 \text{ msec (min.)}$
 $V_H = 12.0 \pm 0.5V$

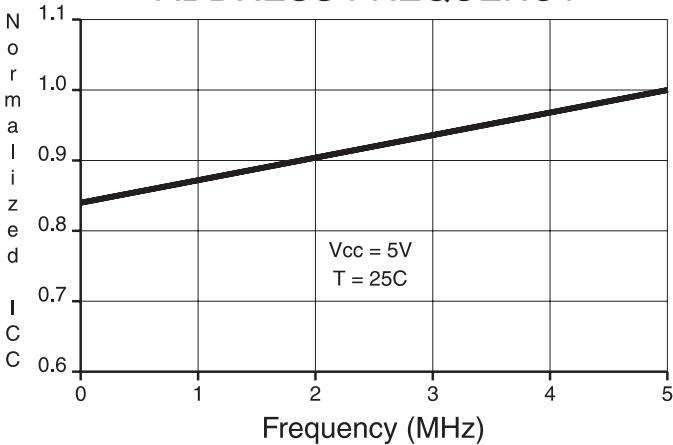
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



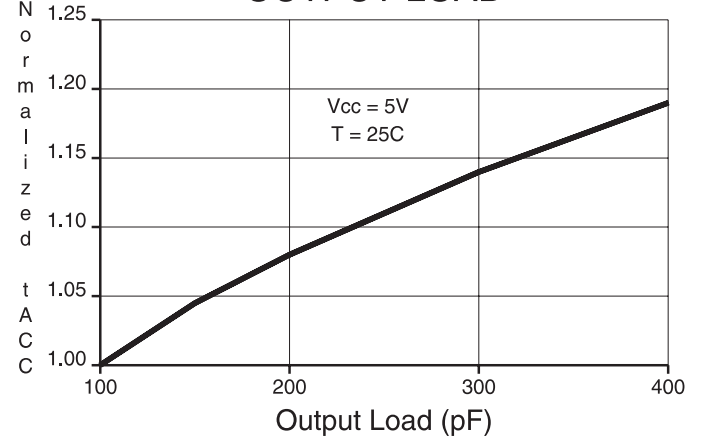
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



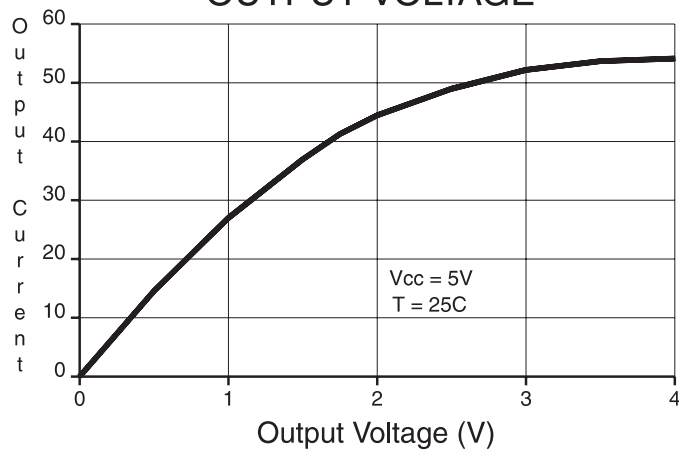
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



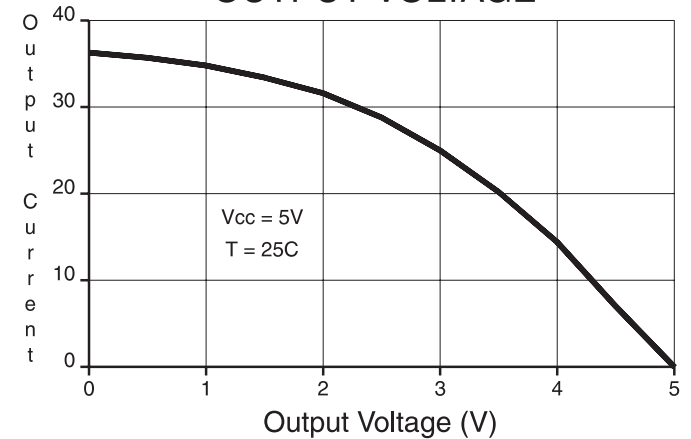
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information⁽¹⁾

| t _{ACC} (ns) | I _{CC} (mA) | | Ordering Code | Package | Operation Range |
|--------------------------|----------------------|---------|---|--------------------|-------------------------------|
| | Active | Standby | | | |
| 150 | 30 | 0.1 | AT28C17(E)-15JC AT28C17(E)-15PC AT28C17(E)-15SC | 32J 28P6 28S | Commercial (0°C to 70°C) |
| | 45 | 0.1 | AT28C17(E)-15JI AT28C17(E)-15PI AT28C17(E)-15SI | 32J 28P6 28S | Industrial (-40°C to 85°C) |

- Notes:
1. See Valid Part Numbers table below.
 2. The 28C17 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 150 ns T_{AA} offering.
 3. The 28C17 ceramic and LCC package offerings have been removed. New designs should utilize the 28C256 ceramic offerings.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

| Device Numbers | Speed | Package and Temperature Combinations |
|----------------|-------|--------------------------------------|
| AT28C17 | 15 | JC, JI, PC, PI, SC, SI |
| AT28C17E | 15 | JC, JI, PC, PI, SC, SI |
| AT28C17 | - | W |

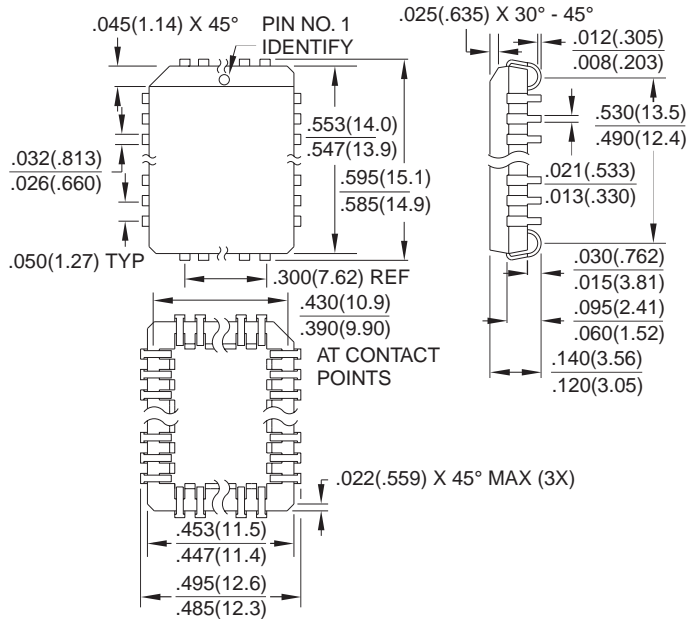
Die Products

Reference Section: Parallel EEPROM Die Products

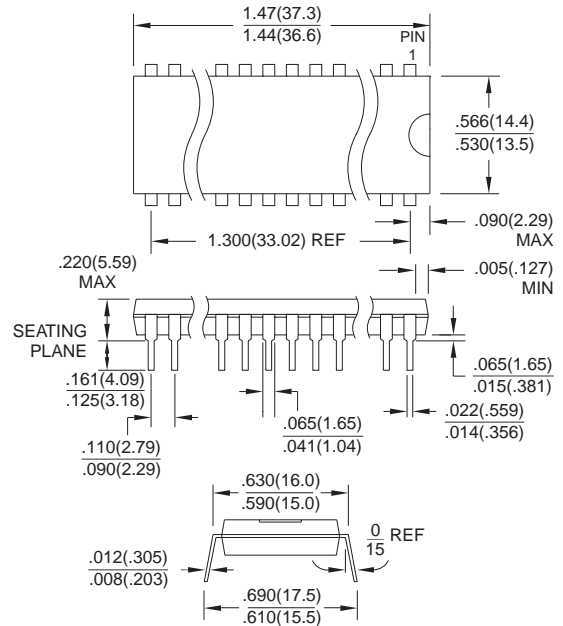
| Package Type | |
|--------------|---|
| 32J | 32-Lead, Plastic J-Leaded Chip Carrier (PLCC) |
| 28P6 | 28-Lead, 0.600" Wide, Plastic Dull Inline Package (PDIP) |
| 28S | 28-Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC) |
| W | Die |
| Options | |
| Blank | Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms |
| E | High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 μs |

Packaging Information

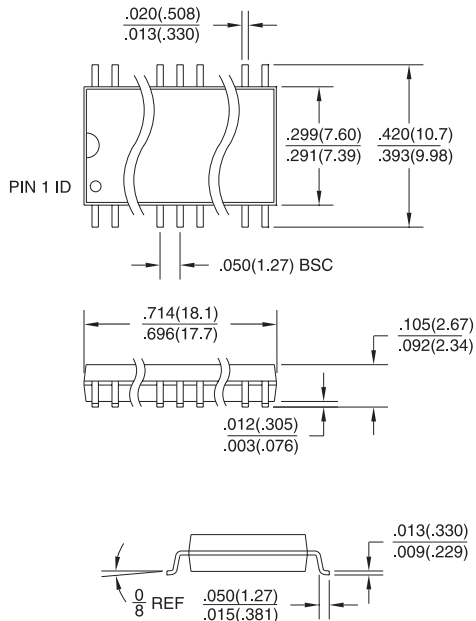
32J, 32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-018 AA



28P6, 28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-011 AB



28S, 24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
 Dimensions in Inches and (Millimeters)





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