NCP5358

Gate Driver for Desktop Power Systems

The NCP5358 is a high performance two channel gate driver. It combines two single NCP5359 gate drivers together and provides an optimized solution for multi−phase application. Each channel gate driver has both high−side and low side power MOSFETs in a synchronous buck converter. Also, it can drive up to 3 nF load with a 25 ns propagation delay and 20 ns transition time.

An adaptive non−overlap and power saving operation circuit has built in. It can provide a low switching loss and high efficiency solution in notebook and desktop systems. Thus, this controller has three protection functions, under voltage lockout (UVLO), over voltage protection (OVP) and thermal shutdown.

The NCP5358 is available in 4x4 mm QFN16 package.

Features

- Faster Rise and Fall Times
- Thermal Shutdown Protection
- Adaptive−Non−Overlap Circuit
- Floating Top Driver Accommodates Boost voltage of up to 30 V
- Output Disable Control Turn Off Both MOSFETs
- Complies with VR11.1 Specifications
- Under−Voltage Lock Out
- Power Saving Operation under Light Load Condition
- Thermally Enhanced Package Available
- These are Pb−Free Devices

Typical Applications

- Power Solutions for Desktop and Notebook system.

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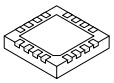
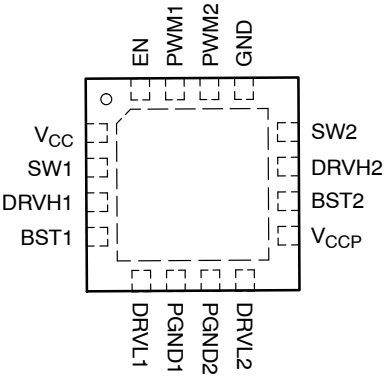


QFN−16
CASE 485D
4x4 mm

MARKING DIAGRAM

N5358	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5358MNTXG	QFN−16 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

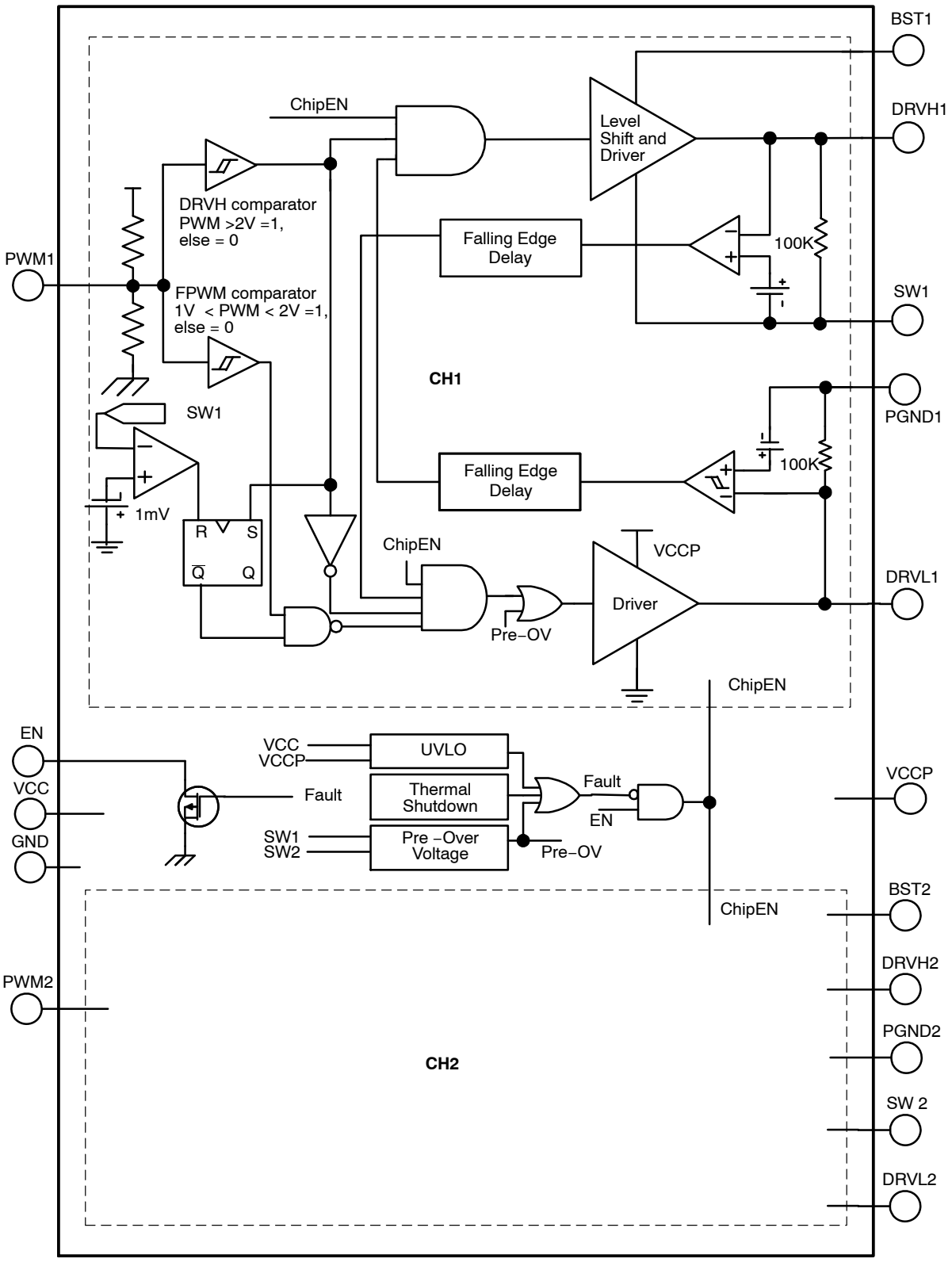


Figure 1. Internal Block Diagram and Typical Application

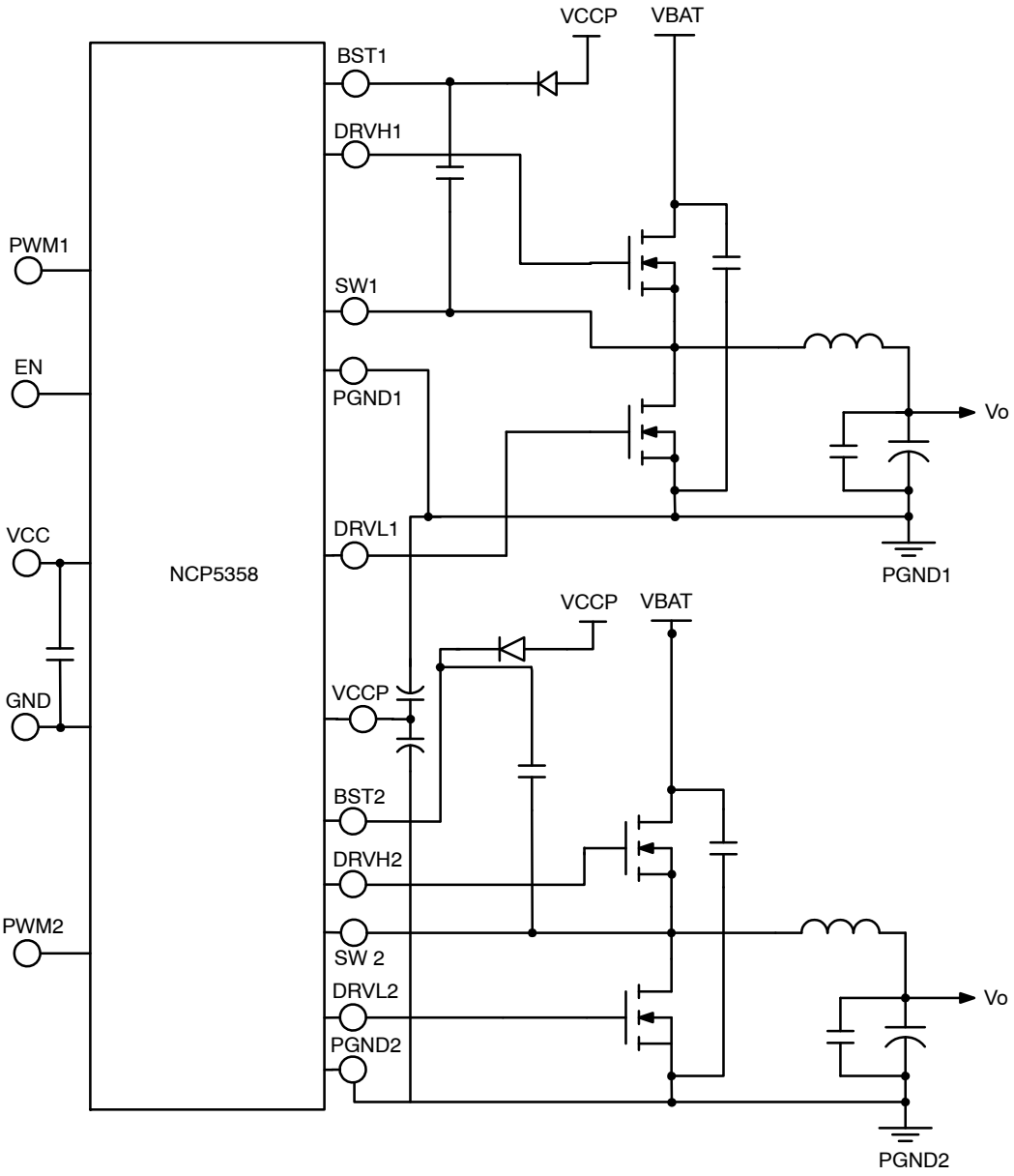


Figure 2. Typical Applications

PIN DESCRIPTION

Pin NO.	Symbol	Descriptions
1	V_{CC}	Analog logic input power pin
2	SW 1	PWM 1 Switch Node pin
3	DRVH 1	PWM 1 High side gate drive output
4	BST1	Upper MOSFET floating bootstrap supply pin
5	DRVL 1	PWM 1 Low side gate drive output
6	PGND 1	PWM 1 Ground pin
7	PGND 2	PWM 2 Ground pin
8	DRVL 2	PWM 2 Low side gate drive output
9	V_{CCP}	Connect to input power supply 10 V to 13.2 V
10	BST 2	Upper MOSFET floating bootstrap supply pin
11	DRVH 2	PWM 2 High side gate drive output
12	SW 2	PWM 2 Switch Node pin
13	GND	Analog logic ground pin
14	PWM 2	PWM2 input pin When PWM voltage is higher than 2 V, DRVH will set to 1 and DRVL set to 0 When PWM voltage is lower than 1 V, DRVL set to 1 and DRVH set to 0 When 1 V < PWM < 2V and SW < 0, DRVL will set to 1 When 1 V < PWM < 2V and SW > 0, DRVL will set to 0
15	PWM 1	PWM1 input pin When PWM voltage is higher than 2 V, DRVH will set to 1 and DRVL set to 0 When PWM voltage is lower than 1 V, DRVL set to 1 and DRVH set to 0 When 1 V < PWM < 2 V and SW < 0, DRVL will set to 1 When 1 V < PWM < 2 V and SW > 0, DRVL will set to 0
16	EN	Both Channel Enable pin When OVP, TSD or UVLO has happened, the gate driver will pull the pin to low

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Thermal Characteristics Plastic Package, Thermal Resistance, Junction to Air (1 in^2 of 2 oz copper)	$R_{\theta JA}$	110	°C/W
Operating Junction Temperature Range	T_J	0 to + 150	°C
Operating Ambient Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Moisture Sensitivity Level	MSL	1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}
V_{CC}	Main Supply Voltage input	15 V	−0.3 V
V_{CCP}	Main Supply Voltage input	15 V	−0.3 V
BST1, BST2	Bootstrap Supply voltage	30 V wrt / GND 35 V ≤ 50 ns wrt / GND 15 wrt / SW	−0.3 V
SW1,SW2	Switching Node (Bootstrap Supply Return)	30 V	−1 VDC −10 V (200 ns)
DRVH1, DRVH2	High Side Driver output	BST + 0.3 V 35 V ≤ 50 ns wrt / GND 15 wrt / SW	−0.3 V −2 V (200 ns)
DRVL1, DRVL2	Low Side Driver output	Vcc + 0.3 V	−0.3 V −2 V (200 ns)
PWM1, PWM2	DRVH and DRVL Control Input	6 V	−0.3 V
EN	Enable Pin	6 V	−0.3 V
GND	Ground	0	0 V

1. Latchup Current Maximum Rating: 100 mA per JEDEC standard: JESD78.
2. Moisture Sensitivity Level (MSL): 1&3 per IPC/JEDEC standard: J−STD−020A.
3. The maximum package power dissipation limit must not be exceeded.

$$PD = \frac{TJ(max) - TA}{R\theta JA}$$

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, T_A = 0°C to 85°C, V_{EN} = 5 V, unless other noted.)

Characteristics		Symbol	Test Conditions	Min	Typ	Max	Units
SUPPLY VOLTAGE							
V_{CC} Operating Voltage		V_{CC}		10	–	13.2	V
Power ON Reset Threshold		V_{POR}		–	3.2	–	V
SUPPLY CURRENT							
V_{CCP} Quiescent Supply Current in Normal Operation		I_{VCCP_NORM}	EN = 5 V, PWM1 = PWM2 = OSC, F_{SW} = 100 K, duty cycle = 50%. C_{LOAD} = 0 p		1.5	4	mA
V_{CC} Quiescent Supply Current in Normal Operation		I_{VCC_NORM}	EN = 5 V, PWM1 = PWM2 = OSC, F_{SW} = 100 K, duty cycle = 50%. C_{LOAD} = 0 p		1.5	2.5	mA
V_{CCP} Standby Current		I_{VCCP_SBC}	EN = GND; No switching	–	0.1	0.5	mA
V_{CC} Standby Current		I_{VCC_SBC}	EN = GND; No switching	–	0.9	1.5	mA
BST1 Quiescent Supply Current in Normal Operation		I_{BST1_normal}	PWM1 = +5 V		1.0	1.5	mA
		I_{BST1_normal}	PWM1 = GND		1.0	1.5	
BST2 Quiescent Supply Current in Normal Operation		I_{BST2_normal}	PWM2 = +5 V		1.0	1.5	mA
		I_{BST2_normal}	PWM2 = GND		1.0	1.5	
BST1 Standby Current		I_{BST1_SD}	PWM1 = +5 V		0.25		mA
		I_{BST1_SD}	PWM1 = GND		0.25		
BST2 Standby Current		I_{BST2_SD}	PWM2 = +5 V		0.25		mA
		I_{BST2_SD}	PWM2 = GND		0.25		
UNDER VOLTAGE LOCKOUT							
V_{CCP} Start Threshold		$VCCP_{TH}$		8.2	8.7	9.5	V
V_{CCP} UVLO Hysteresis		$VCCP_{HYS}$			1.0		V
V_{CC} Start Threshold		VCC_{TH}		8.2	8.7	9.5	V
V_{CC} UVLO Hysteresis		VCC_{HYS}			1.0		V
Output Overvoltage Trip Threshold at channel 1 Startup		OVP1_SU	Power Startup time, V_{CC} > 9 V. (Without trimming)	1.8		2.0	V
Output Overvoltage Trip Threshold at channel 2 Startup		OVP2_SU	Power Startup time, V_{CC} > 9 V. (Without trimming)	1.8		2.0	V
EN INPUT							
Input Voltage High		V_{EN_HI}		2.0			V
Input Voltage Low		V_{EN_LOW}				1.0	V
Hysteresis (Note 6)		V_{EN_HYS}			500		mV
Enable Pin Sink Current		I_{EN_SINK}	V_{CC} = 5.5 V	5.0			mA
Propagation Delay Time (Note 6)		TpdhEN			20	60	ns
		TpdlEN			20	60	ns
PWM INPUT							
PWM Input Self Bias Voltage	CH1	V_{PWM1}		1.4	1.5	1.6	V
	CH2	V_{PWM2}					
DRVH Comparator Rise Threshold	CH1	VTH_DRVH1		2.2			V
	CH2	VTH_DRVH2					
DRVL Comparator Rise Threshold	CH1	VTH_DRVL1				0.8	V
	CH2	VTH_DRVL2					

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, T_A = 0°C to 85°C, V_{EN} = 5 V, unless other noted.)

Characteristics		Symbol	Test Conditions	Min	Typ	Max	Units
PWM INPUT							
Input Current	CH1	I_{PWM1}	PWM1 = 0 V, EN = GND		30		μA
	CH2	I_{PWM2}	PWM2 = 0 V, EN = GND				
HIGH SIDE DRIVER							
Output Resistance, Sourcing	CH1	R_{H_TG1}	$V_{BST1} - V_{SW1}$ = 12 V		2.0	3.5	Ohms
	CH2	R_{H_TG2}	$V_{BST2} - V_{SW2}$ = 12 V				
Output Resistance, Sinking	CH1	R_{H_TG1}	$V_{BST1} - V_{SW1}$ = 12 V		1.0	2.5	Ohms
	CH2	R_{H_TG2}	$V_{BST2} - V_{SW2}$ = 12 V				
Transition Time (Note 6)	CH1	Tr_{DRVH1}	C_{LOAD} = 3 nF, $V_{BST1} - V_{SW1}$ = 12 V		16	25	ns
		Tf_{DRVH1}	C_{LOAD} = 3 nF, $V_{BST1} - V_{SW1}$ = 12 V		11	15	
	CH2	Tr_{DRVH2}	C_{LOAD} = 3 nF, $V_{BST2} - V_{SW2}$ = 12 V		16	25	
		Tf_{DRVH2}	C_{LOAD} = 3 nF, $V_{BST2} - V_{SW2}$ = 12 V		11	15	
Propagation Delay (Notes 5 & 6)	CH1	$Tpdh_{DRVH1}$	Driving High, C_{LOAD} = 3 nF	10		40	ns
		$Tpdl_{DRVH1}$	Driving Low, C_{LOAD} = 3 nF	10		40	
	CH2	$Tpdh_{DRVH2}$	Driving High, C_{LOAD} = 3 nF	10		30	
		$Tpdl_{DRVH2}$	Driving Low, C_{LOAD} = 3 nF	10		30	
LOW SIDE DRIVER							
Output Resistance, Sourcing	CH1	R_{H_BG1}	SW = GND		2.0	3.5	Ohms
	CH2	R_{H_BG2}	SW = GND				
Output Resistance, Sinking	CH1	R_{L_BG1}	SW = V_{CC}		1.0	2.5	Ohms
	CH2	R_{L_BG2}	SW = V_{CC}				
Transition Time (Note 6)	CH1	TrDRVL1	C_{LOAD} = 3 nF		16	25	ns
		TfDRVL1	C_{LOAD} = 3 nF		11	15	
	CH2	TrDRVL2	C_{LOAD} = 3 nF		16	25	
		TfDRVL2	C_{LOAD} = 3 nF		11	15	
Propagation Delay (Notes 5 & 6)	CH1	$Tpdh_{DRVL1}$	Driving High, C_{LOAD} = 3 nF	10		40	ns
		$Tpdl_{DRVL1}$	Driving Low, C_{LOAD} = 3 nF	10		40	
	CH2	$Tpdh_{DRVL2}$	Driving High, C_{LOAD} = 3 nF	10		30	
		$Tpdl_{DRVL2}$	Driving Low, C_{LOAD} = 3 nF	10		30	
Negative Current Detector Threshold	CH1	V_{NCDT1}	(Note 4)		−1.0		mV
	CH2	V_{NCDT2}	(Note 4)				
THERMAL SHUTDOWN							
Thermal Shutdown		Tsd	(Note 6)	150	170	–	°C
Thermal Shutdown Hysteresis		Tsdhys	(Note 6)		20		°C

4. Design guaranteed
5. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low.
6. Guaranteed by design; not tested in production

Table 1. Decoder Truth Table:

PWM 1 or PWM 2 Input	ZCD	DRVL	DRVH
Greater than 2.0 V	X	Low	High
Greater than 1.0 V, but less than 2.0 V	High (current through MOSFET is greater than 0)	High	Low
Greater than 1.0 V, but less than 2.0 V	Low (current through MOSFET is less than 0)	Low	Low
Less than 1.0 V	X	High	Low

Application Information

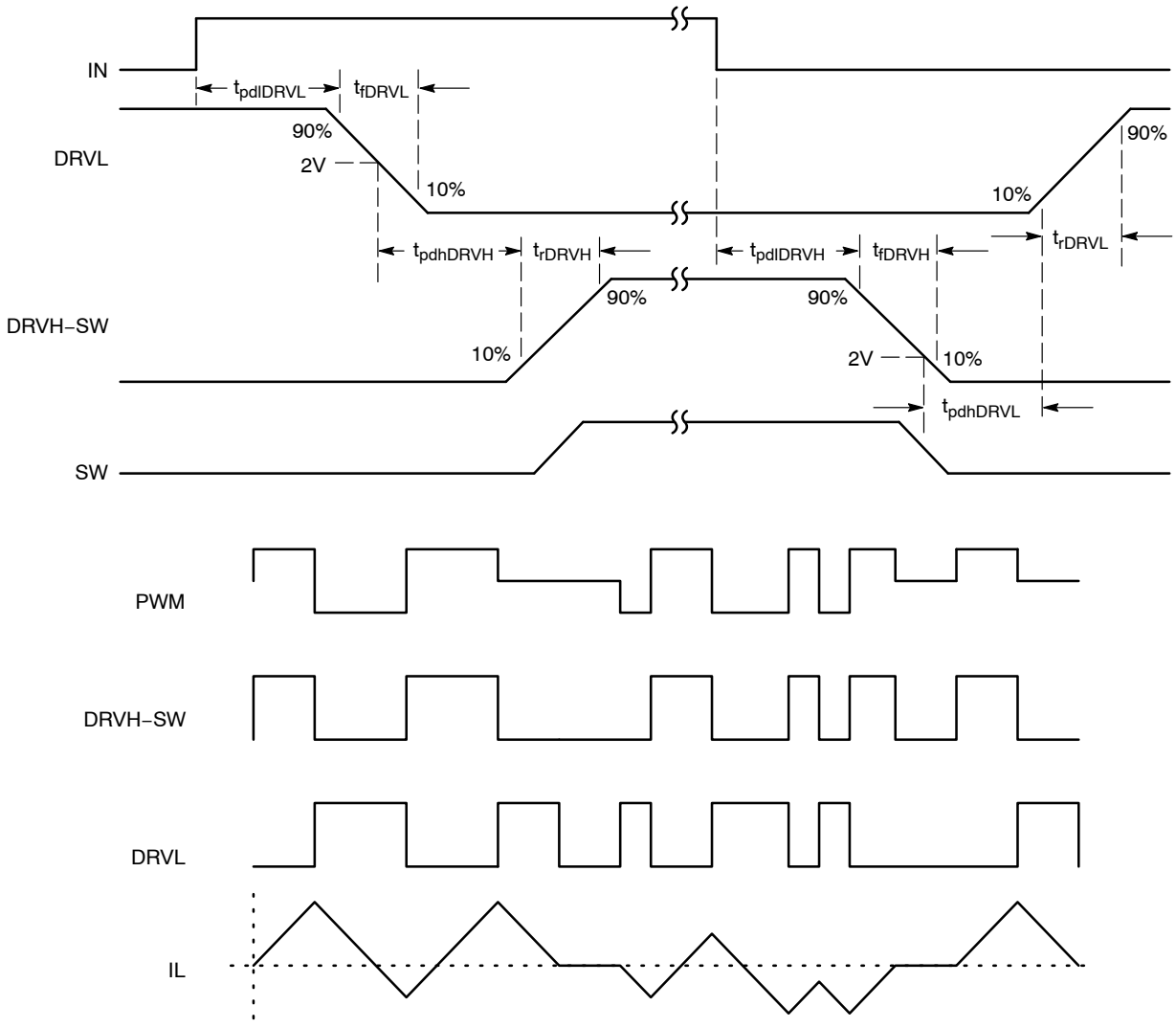


Figure 3. Timing Diagram

The NCP5358 gate driver is a dual phase MOSFET driver, each phase designed for driving two N−channel MOSFETs in a synchronous buck converter topology. This driver is compatible with the Signal channel NCP5359 gate drive. This gate drives has a Bi−direction fault detection and multi−level PWM input feature. When the gate driver works with ON's NCP539X controller, it can provide a difference output logic status through multi−level PWM input. For this new feature, higher efficiency can be provided. For the bi−direction fault detection function, it is used to provide a driver state information to other gate drivers and controller in a multi−phase buck converter. e.g over voltage protection (OVP) function at startup, thermal shutdown and under voltage lockout (UVLO). This feature can provide an additional protection function for the multi−phase system when the fault condition occurs in one channel. With this additional feature, converter overall system will be more reliable and safe.

Enable Pin

The bi−direction enable pin is connected with an open drain MOSFET. This pin is controlled by internal or external signal. There are three conditions will be triggered:

1. The voltage at SW1 or SW2 pin is higher than preset voltage at power start up.
2. The controller hits the UVLO at V_{CC} pin or V_{CCP} pin.
3. The controller hits the thermal shutdown.

When the internal fault has been detected, EN pin will be pull low. In this case, both channel drive output DRVH and DRVL will be forced low, until the fault mode remove then restart automatic.

Under Voltage Lockout

The DRVH1, DRVH2 and DRVL1, DRVL2 are held low until V_{CC} or V_{CCP} reaches 9 V during startup. The PWM signals will control the gate status when V_{CC} threshold is exceeded. If V_{CC} decreases to 3.2 V below the threshold, the output gate will be forced low until input voltage V_{CC} rises above the startup threshold.

Power ON Reset

Power on reset feature is used to protect a gate driver avoid abnormal status driving the start up condition. When the initial soft start voltage V_{CC} is higher than 3.2 V, the gate driver will monitor the switching node SW pin. If SW1 or SW2 pin high than 1.9 V, bottom gate will be force to high for discharge the output capacitor. The fault mode will be latch and EN pin will force both channel to be low, unless the driver is recycle. When input voltage is higher than 9 V, the gate driver will normal operation, top gate driver DRVH and bottom gate driver will follow the PWM signal decode to a status.

Adaptive Non−overlap

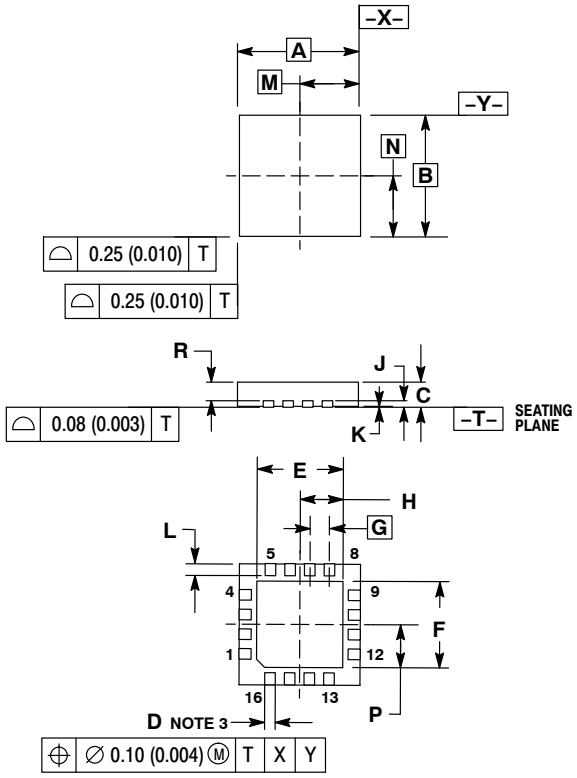
The non−overlap dead time control is used to avoid the shoot through damage the power MOSFETs. When the PWM signal pull high, DRVL will go low after a propagation delay, the controller will monitors the switching node (SW) pin voltage and the gate voltage of the MOSFET to know the status of the MOSFET. When the low side MOSFET status is off an internal timer will delay turn on of the high−side MOSFET. When the PWM pull low, gate DRVH will go low after the propagation delay (tpdDRVH). The time to turn off the high side MOSFET is depending on the total gate charge of the high−side MOSFET. A timer will be triggered once the high side MOSFET is turn off to delay the turn on the low−side MOSFET.

Layout Guidelines

Layout is very important thing for design a DC−DC converter. Bootstrap capacitor and V_{CC} capacitor are most critical items, it should be placed as close as to the driver IC. Another item is using a GND plane. Ground plane can provide a good return path for gate drives for reducing the ground noise. Therefore GND pin should be directly connected to the ground plane and close to the low−side MOSFET source pin in every channel. Also, the gate drive trace should be considered. The gate drives has a high di/dt when switching, therefore a minimized gate drives trace can reduce the di/dv, raise and fall time for reduce the switching loss.

PACKAGE DIMENSIONS

16 PIN QFN
CASE 485D−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.00 BSC		0.157 BSC	
B	4.00 BSC		0.157 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.35	0.009	0.014
E	2.75	2.85	0.108	0.112
F	2.75	2.85	0.108	0.112
G	0.65 BSC		0.026 BSC	
H	1.38	1.43	0.054	0.056
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	2.00 BSC		0.079 BSC	
N	2.00 BSC		0.079 BSC	
P	1.38	1.43	0.054	0.056
R	0.60	0.80	0.024	0.031

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