Evaluating the LT3073 3A, Ultra-Low Noise, High PSRR, 45 mV Dropout Ultra-Fast Linear Regulator

FEATURES

- Input voltage range: 0.6 V to 5.5 V
- BIAS voltage range: 2.375 V to 5.5 V
- Jumpers program output voltage according to selection matrix: 0.5 V to 4.2 V
- Maximum output current: 3 A
- BNC connectors for noise and PSRR measurement
- Jumper and resistor combinations select either 3.72 A or 1.5 A output current limit and commensurate monitoring or disable programmed current limit and monitoring
- Jumper turns regulator on or off
- Terminals provide output current, temperature, and output regulation status monitoring
- Jumper to margin output voltage ±2.5%
- The VIOC pin of the LT3073 manages power dissipation and PSRR
- Banana jacks minimize V_{IN} and V_{OUT} connection voltage drops
- VO+, VO−, and VI+ terminals for regulation and dropout monitoring
- Thermally enhanced, 22-lead, 3 mm × 4 mm x 0.95 mm, LQFN package

EVALUATION KIT CONTENTS

- EVAL-LT3073-AZ evaluation board

EQUIPMENT NEEDED

- DC power supplies
- Multimeters for voltage and current measurements
- Electronic or resistive load

DOCUMENTS NEEDED

- LT3073 data sheet

EVALUATION BOARD PHOTOGRAPH

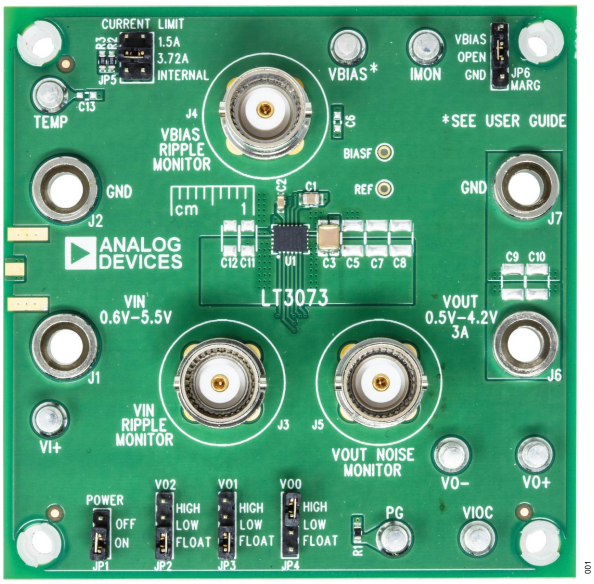

Figure 1. EVAL-LT3073-AZ Evaluation Board Photograph

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REVISION HISTORY

1/2023—Revision 0: Initial Version

GENERAL DESCRIPTION

The EVAL-LT3073-AZ evaluation board features the LT3073, a 3 A, ultra-low noise, high power-supply rejection ratio (PSRR), 45 mV dropout ultra-fast linear regulator. The input voltage (VIN) range for the VIN power is from 0.6 V to 5.5 V. There are jumpers to set a 3-bit trilevel code that determines the output voltage (VOUT) at preprogrammed levels that range from 0.5 V to 4.2 V. The maximum output current is 3 A. The EVAL-LT3073-AZ requires an external BIAS voltage (VBIAS) that is at least 1.2 V higher than VOUT and is between 2.375 V and 5.5 V.

The LT3073 of the EVAL-LT3073-AZ requires few external components; therefore, simplifying circuit design. External component choice along with careful printed circuit board (PCB) design help optimize noise, PSRR, load transient response, and V_{OUT} regulation performance. The LT3073 requires capacitors for the internal reference, power input, BIASF pin, and the power output. The internal reference is bypassed with a 16 V, 0805 sized, 4.7 µF capacitor to reduce output noise and program the soft-start. Larger capacitor case sizes and higher voltage ratings decrease 1/f noise for otherwise comparable capacitors. The 22 µF capacitor at the circuit output was chosen for high-frequency PSRR performance and to minimize VOUT deviation during load transients.

The capacitor that bypasses the VIN power for the LT3073 and the corresponding VIN PCB layout can affect PSRR (see the Best PSRR Performance: PCB Layout for Input Traces section for additional information). The EVAL-LT3073-AZ decouples the VIN power with a 47 µF capacitor. Less VIN capacitance can improve PSRR at high frequencies (see the LT3073 data sheet for the minimum capacitor value required for VIN). Note that a bulk 220 µF tantalum polymer capacitor further reduces VIN variation during load transients and reduces input voltage ringing that can be caused by inductive input power leads. The PCB has a footprint for an optional Subminiature Version A (SMA) connector that allows a shielded VIN power connection to the PCB edge, if required.

The EVAL-LT3073-AZ bypasses the BIASF pin with a 2.2 µF capacitor instead of the VBIAS supply input. Because the BIASF pin is isolated from VBIAS by a resistance that is internal to the LT3073, there is less PSRR degradation when BIASF is bypassed compared to when VBIAS is bypassed. Otherwise, the effect on PSRR of the VIN and VBIAS bypass capacitors is similar.

The EVAL-LT3073-AZ has resistors that allow a CURRENT LIMIT jumper to select output current limits of either 1.5 A or 3.72 A.

The CURRENT LIMIT jumper can also disable external current-limit programming by shorting the IMON pin to ground. An IMON terminal is available for current monitoring. The IMON voltage is the product of the resistance that externally programs current limit and the IMON pin current that is 1/3000 of the output current. Externally programmed current limit occurs when the IMON voltage is 1 V.

A POWER jumper (JP1) is available on the EVAL-LT3073-AZ to either connect the EN pin to VBIAS to turn the output on or to ground to disable the output. A TEMP terminal is also available for die temperature monitoring. There is a PG terminal that is pulled up to VBIAS by a 51 kΩ resistor and pulled down by the open-drain, negative channel metal-oxide semiconductor (NMOS) PG pin output for indication of regulator output status and other fault modes. The voltage input-to-output control (VIOC) terminal allows connections for automatically controlling a preregulation voltage. In addition, a MARG jumper can margin the output voltage to either ±2.5%.

Banana jacks minimize voltage drops on VIN and VOUT connections. Bayonet Neill-Concelman (BNC) connectors provide low noise connections to power VIN, VBIAS, and VOUT. The EVAL-LT3073-AZ PCB design uses a split capacitor technique to Kelvin connect the ground terminal of the REF capacitor to the ground terminal of the output capacitor, and the SENSE pin to the positive terminal of the output capacitor. The VO+, VO−, and VI+ terminals Kelvin connect to VIN and VOUT and are the optimum place to observe output voltage regulation and dropout voltage performance. There are test points for BIASF and REF voltages.

The EVAL-LT3073-AZ has placeholders identified on the schematic as optional OPT components that make it convenient to add capacitance (see Figure 8).

For full details on the LT3073, see the LT3073 data sheet, which must be consulted with this user guide when using the EVAL-LT3073-AZ evaluation board. The LT3073 of the EVAL-LT3073-AZ features a thermally enhanced, 22-lead, 3 mm x 4 mm x 0.95 mm LQFN package. Proper board layout is essential for maximum thermal performance.

Design files are available on the EVAL-LT3073-AZ evaluation board website page.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Table 1. Performance Summary

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE	V_{IN}					
Minimum					0.6	V
Maximum		I_{OUT} = 300 mA	5.5			V
		V_{OUT} = 1.5 V, I_{OUT} = 3 A	2[1]			V
BIAS VOLTAGE	V_{BIAS}					
Minimum		$V_{BIAS} \geq V_{OUT}$ + 1.2 V			2.375	V
Maximum			5.5			V
OUTPUT VOLTAGE	V_{OUT}	V_{OUT} = 0.5 V, 50 mA ≤ I_{OUT} ≤ 3 A, V_{IN} = 0.8 V	0.492	0.500	0.508	V
		V_{OUT} = 1.2 V, 10 mA ≤ I_{OUT} ≤ 3 A, V_{IN} = 1.5 V	1.182	1.200	1.218	V
		V_{OUT} = 3.3 V, 10 mA ≤ I_{OUT} ≤ 3 A, V_{IN} = 3.6 V	3.250	3.300	3.35	V
		V_{OUT} = 4.2 V, 10 mA ≤ I_{OUT} ≤ 3 A, V_{IN} = 4.5 V	4.137	4.200	4.263	V
OUTPUT CURRENT	I_{OUT}					
Maximum			3			A
Minimum		V_{OUT} < 0.8 V			50	mA
		V_{OUT} ≥ 0.8 V			10	mA
Limit		IMON resistor (R_{IMON}) = 2 kΩ (1.5 A jumper position)	1.41	1.50	1.59	A
		R_{IMON} = 806 Ω (3.72 A jumper position)	3.61	3.72	3.83	A
BIAS PIN NAP MODE CURRENT	I_{BIAS}	V_{BIAS} = 5.5 V, EN = 0 V, R1 = open			10	µA
IN PIN NAP MODE CURRENT	I_{IN}	V_{IN} = 5.5 V, EN = 0 V			500	µA

[1] The maximum power dissipation and, consequently, the maximum input voltage for an output that is programmed to 1 V with a 3 A load is set by the 60°C temperature rise of the LT3073 on the evaluation board. Higher input voltages can be reached if larger copper area or forced-air cooling is applied. In addition, consider the effect of ambient temperature and the maximum junction temperature that may occur. See the LT3073 data sheet for more information.

QUICK START PROCEDURE

To use the EVAL-LT3073-AZ to evaluate the performance of the LT3073, see Figure 2 for the proper measurement equipment setup and take the following steps:

1. With the input supplies off and turned down and the load turned down, make all the connections shown in Figure 2. Ensure that the VO2, VO1, and VO0 jumpers to set VOUT are in the proper positions for the desired VOUT according to the V_{OUT} selection matrix table in the LT3073 data sheet. In addition, ensure that the POWER jumper (JP1) is in the **ON** position, the CURRENT LIMIT jumper (JP5) is in the **3.72A** position, and the MARG jumper (JP6) is in the **OPEN** position.
2. Turn on the input and bias supplies and increase the input supply so it is at least 200 mV above the programmed output voltage. Adjust VBIAS so it is between 2.375 V and 5.5 V and at least 1.2 V higher than the programmed VOUT for proper operation. Note that when setting the input and bias voltages, a VIN or VBIAS that is too close to the programmed VOUT (too low) can cause dropout operation and a loss of VOUT regulation. Also, a VIN that is too high above the output can increase power dissipation to an unacceptable level.
3. Increase the load to the desired IOUT. Readjust the input supply so it is still at least 200 mV above the programmed output voltage. Verify that VOUT is the expected voltage programmed by the jumpers. Note that if VOUT is lower than expected, the load may be set too high. Temporarily disconnect the load to ensure that it is not set too high.
4. When the proper VOUT is established, adjust the input voltages and load within the operating ranges and observe the VOUT regulation, load transient response, and other parameters.
5. Refer to Application Note AN83 and Application Note AN159 for measuring output noise and PSRR. Note that J3, J4, and J5 are BNC connectors that are used for noise and PSRR measurements.
6. Note that the CURRENT LIMIT jumper can additionally select a **1.5 A** current limit or the **INTERNAL** current limit that the LT3073 provides. Monitor the output current at the IMON terminal when the **1.5 A** or **3.72 A** current limits are selected.
7. Use the MARG jumper to margin the output voltage higher or lower.
8. Monitor power good and temperature at the PG and TEMP terminals, respectively.
9. Refer to the LT3073 data sheet for the usage of the VIOC terminal.

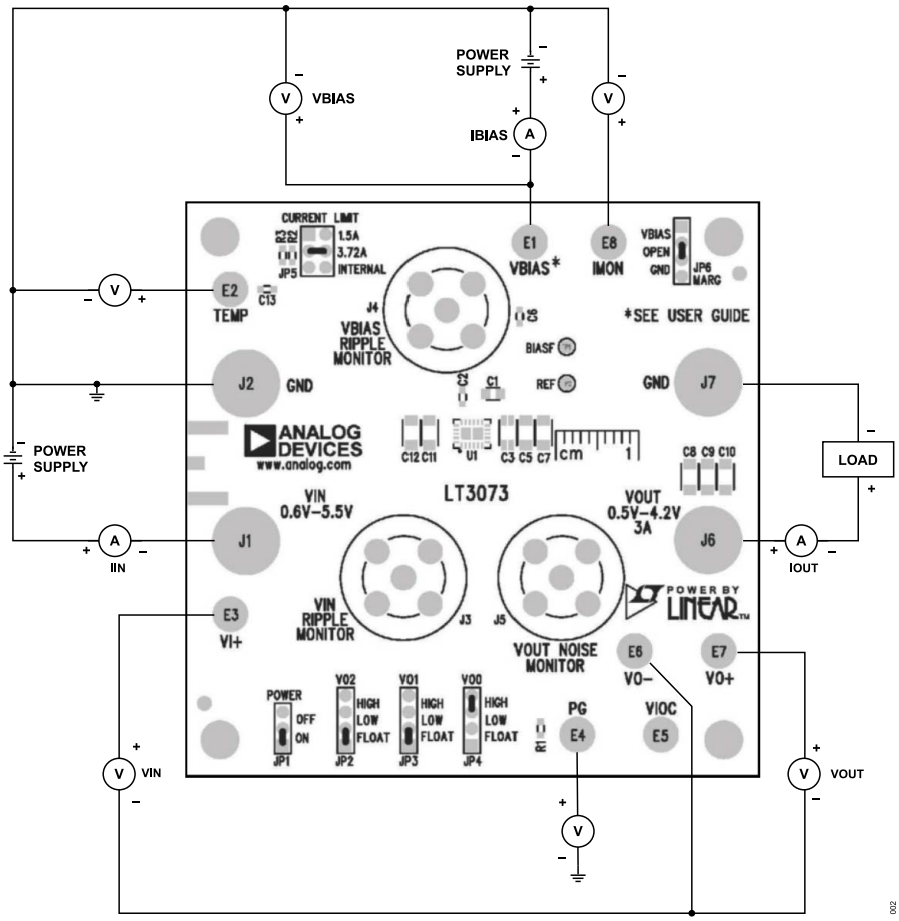

Figure 2. Proper Measurement Equipment Setup for the EVAL-LT3073-AZ

QUICK START PROCEDURE

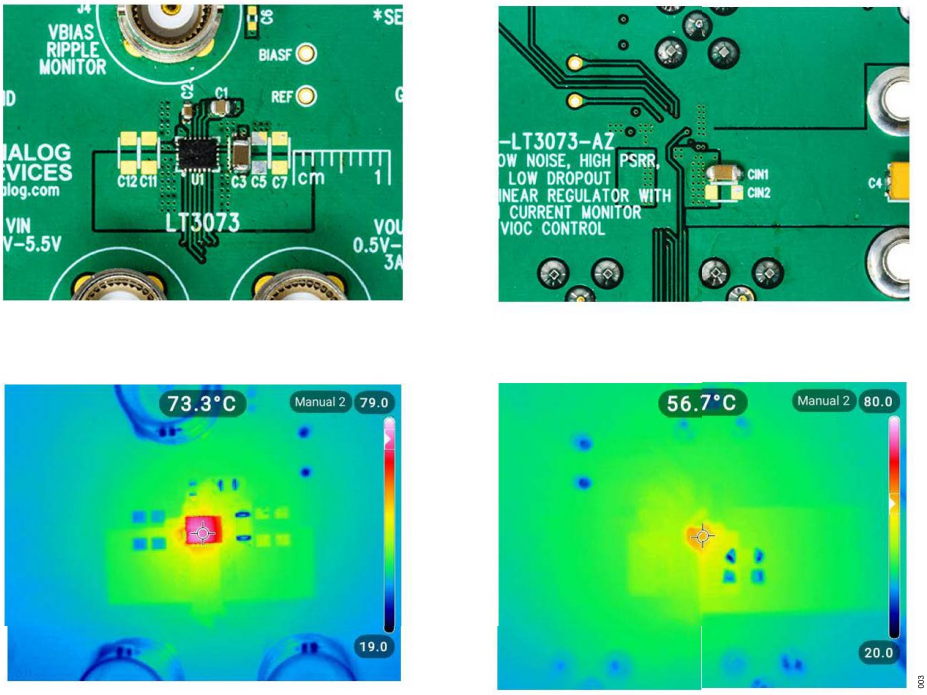

Figure 3. EVAL-LT3073-AZ Front Nonthermal (Top Left), Back Nonthermal (Top Right), Front Thermal (Lower Left), and Back Thermal (Lower Right) Images with a 2 V Input Voltage, a 5 V BIAS Voltage, a 1.5 V Output Voltage, and a 3 A Load Current, Vertical Orientation with No Forced Air

PRINTED CIRCUIT BOARD (PCB) LAYOUT

BEST PSRR PERFORMANCE: PCB LAYOUT FOR INPUT TRACES

For applications using the LT3073 for post-regulating switching converters, placing a capacitor directly at the LT3073 input results in AC current (at the switching frequency) to flow near the LT3073. Without careful attention to the PCB layout, this relatively high-frequency switching current generates an electromagnetic field (EMF) that couples to the LT3073 output, degrading its effective PSRR. While highly dependent on the PCB, the switching preregulator, the input capacitor size, among other factors, the PSRR can easily degrade at high frequencies. This degradation is present even if the LT3073 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional low PSRR low dropout (LDO) regulators, the high PSRR of the LT3073 requires careful attention to higher-order parasitics to realize the full performance offered by the regulator.

The EVAL-LT3073-AZ alleviates this degradation in PSRR by using a specialized layout technique. On Layer 3, the input trace (VIN) is highlighted in red (see Figure 4), with the return path (GND) highlighted on Layer 4 together with the CIN1 input capacitor (see Figure 5). When an AC voltage is applied to the input of the EVAL-LT3073-AZ, AC current flows on the path formed through CIN1 by the input and ground traces. Without the proper PCB layout, the AC current that flows on this path can generate EMFs that do not completely cancel and couple to the C3 output capacitor and related traces, making the PSRR appear worse than it actually is. With the input trace directly above the return path, the EMFs are in opposite directions, and consequently, cancel each other out. Ensure that these traces exactly overlap each other to maximize the cancellation effect and thus provide the maximum PSRR offered by the regulator.

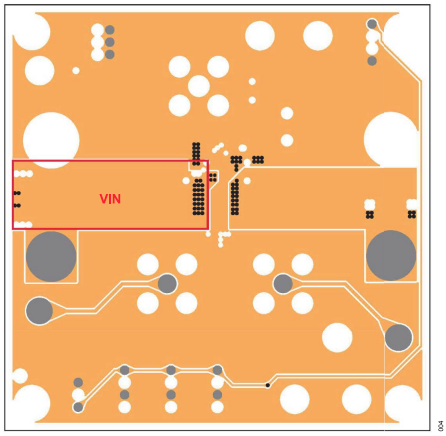

Figure 4. Layer 3 of EVAL-LT3073-AZ

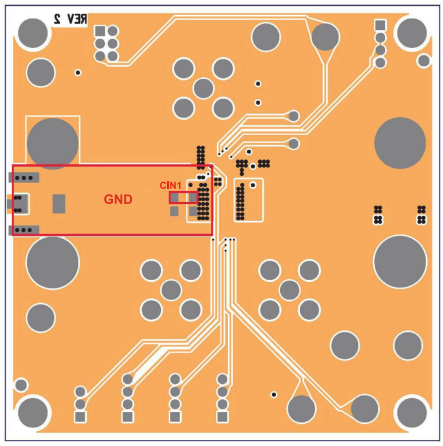

Figure 5. Layer 4 of EVAL-LT3073-AZ

PCB LAYOUT FOR THE C3 OUTPUT CAPACITOR

As previously mentioned, the EVAL-LT3073-AZ PCB design uses a split-capacitor technique to Kelvin connect the ground terminal of the REF capacitor to the ground terminal of the C3 output capacitor and the SENSE pin to the positive terminal of the output capacitor (see Figure 6 and Figure 7). This Kelvin connection regulates the output voltage at the output capacitor, which in turn, optimizes noise, PSRR, load transient, and regulation performance that is all measured at the output capacitor. The split-capacitor technique is useful in this case because it makes it possible to relocate the regulation point, if desired. Regulation of the output voltage at a new location requires leaving the C3 output-capacitor location open and wiring the split-capacitor pads corresponding to the REF capacitor ground terminal and SENSE to the new output capacitor location. Additional capacitance located from SENSE to the REF ground between the regulation point and the LT3073 decreases stability. The split-capacitor technique itself does not enhance LT3073 stability because of the type of pass transistor, even though the unity-gain bandwidth of the LT3073 bandwidth is relatively high and close to the self-resonance frequency of the output capacitor.

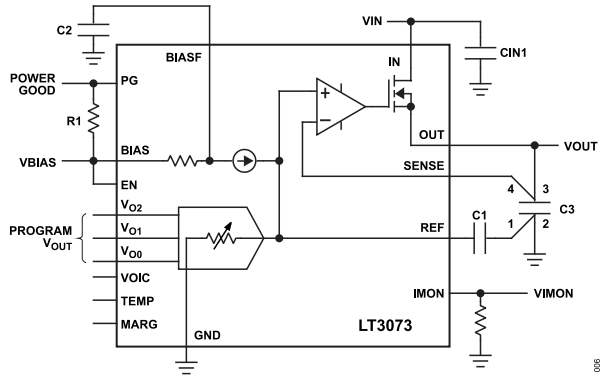

Figure 6. REF Capacitor C1 and Output Capacitor C3 Connections for Best Noise, PSRR, Load Transient, and Regulation Performance

PRINTED CIRCUIT BOARD (PCB) LAYOUT

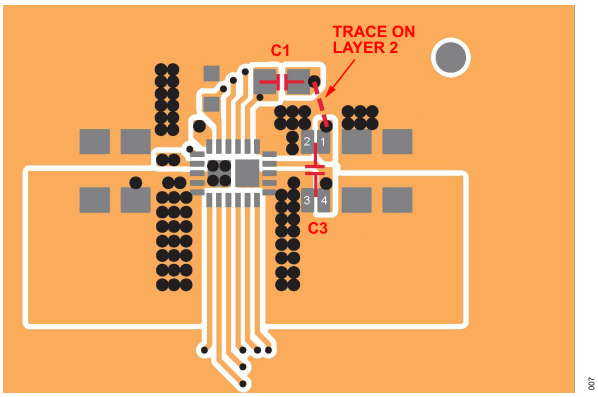

Figure 7. Split Pads for the C3 Output Capacitor on the Top Layer of EVAL-LT3073-AZ, Connect the Ground Terminal of the C1 REF Capacitor to the Ground Terminal of C3 and the SENSE Pin to the Positive Terminal of C3

EVALUATION BOARD SCHEMATIC

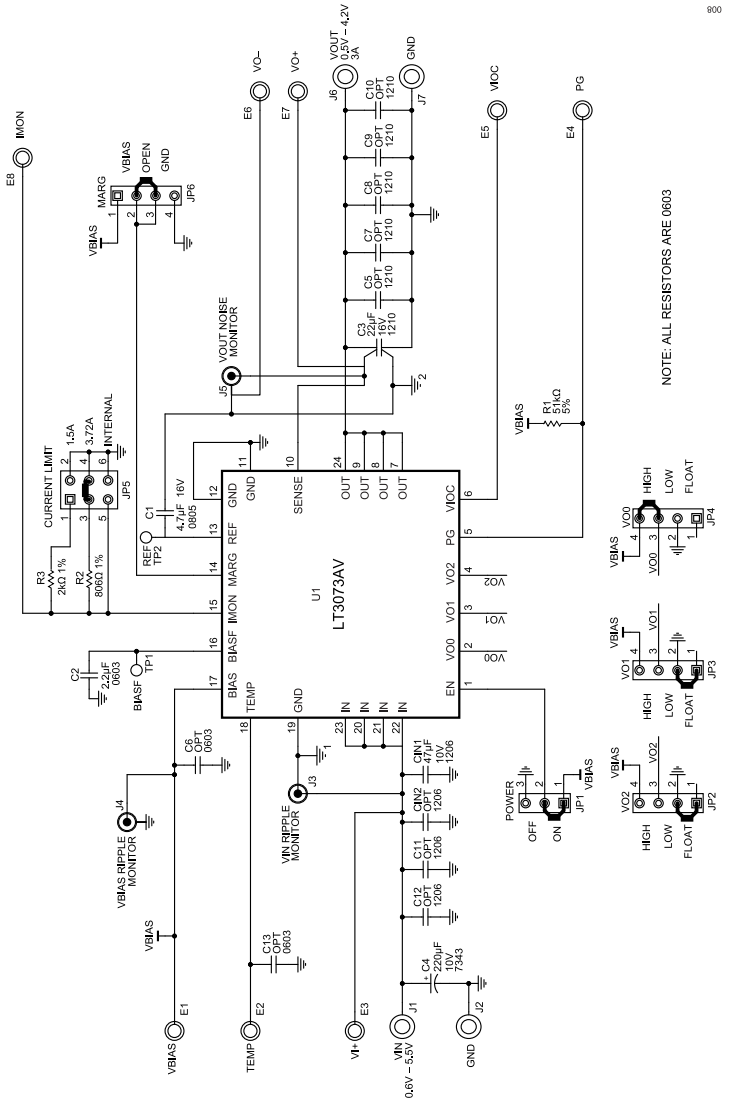

Figure 8. Evaluation Board Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. Bill of Materials

Item	Quantity[1]	Reference Designator	Part Description	Manufacturer, Part Number
Required Circuit Components				
1	1	C1	4.7 µF capacitor, X7R, 16 V, 10%, 0805, soft termination	Murata, GCJ21BR71C475KA01L
2	1	C2	2.2 µF capacitor, X7R, 10 V, 10%, 0603	Murata, GRM188R71A225KE15D
3	1	C3	22 µF capacitor, X7R, 16 V, 10%, 1210	Murata, GCM32ER71C226KE19L
4	1	CIN1	47 µF capacitor, X5R, 10 V, 10%, 1206	Murata, GRM31CR61A476KE15L
5	1	U1	3 A, ultra-low noise, high PSRR, 45 mV dropout, ultra-fast linear regulator	Analog Devices, Inc., LT3073AV#PBF
Optional Evaluation Board Components				
1	1	C4	220 µF capacitor, tantalum polymer, 10 V, 20%, 7343, 40 mΩ ESR	AVX, TCJD227M010R0040
2		C5, C7, C8, C9, C10	Capacitors, 1210, optional	Optional
3		C6, C13	Capacitors, 0603, optional	Optional
4		C11, C12, CIN2	Capacitors, 1206, optional	Optional
5	1	R1	51 kΩ resistor, 5%, 1/10 W, 0603, AEC-Q200	Vishay, CRCW060351K0JNEA
6	1	R2	806 Ω resistor, 1%, 1/10 W, 0603,AEC-Q200	Vishay, CRCW0603806RFKEA
7	1	R3	2 kΩ resistor, 1%, 1/10 W, 0603, AEC-Q200	Vishay, CRCW06032K00FKEA
Hardware				
1	8	E1 to E8	Test points, turret, 0.094" PBF	Mill-Max, 2501-2-00-80-00-00-07-0
2	4	J1, J2, J6, J7	Connectors, banana jack, female, through-hole, noninsulated, swage, 0.218"	Keystone, 575-4
3	3	J3 to J5	Connectors, RF, BNC, receptacle, jack, 5-pin, straight, through-hole, 50 Ω	Amphenol RF, 112404
4	1	JP1	Connector, header, male, 1 x 3, 2 mm, vertical, straight, through-hole	Wurth Elecktronik, 62000311121
5	4	JP2 to JP4, JP6	Connectors, header, male, 1 x 4, 2 mm, vertical, straight, through-hole	Wurth Elecktronik, 62000411121
6	1	JP5	Connector, header, male, 2 × 3, 2 mm, vertical, straight, through-hole	Wurth Elecktronik, 62000621121
7	4	MP1 to MP4	Standoffs, nylon, snap-on, ½ inch	Wurth Elecktronik, 702935000
8	6	XJP1 to XJP6	Connector shunt, female, 2-position, 2 mm	Wurth Elecktronik, 60800213421

[1] Blank cell is for optional components.

ORDERING INFORMATION

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.