

Inverter Grade Thyristors (Hockey PUK Version), 370 A


A-PUK (TO-200AB)

**RoHS
COMPLIANT**
FEATURES

- Metal case with ceramic insulator
- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- International standard case A-PUK (TO-200AB)
- Guaranteed high dI/dt
- High surge current capability
- Low thermal impedance
- High speed performance
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

TYPICAL APPLICATIONS

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

PRIMARY CHARACTERISTICS	
Package	A-PUK (TO-200AB)
Circuit configuration	Single SCR
$I_{T(AV)}$	370 A
V_{DRM}/V_{RRM}	1000 V, 1200 V
V_{TM}	1.72 V
I_{TSM} at 50 Hz	5260 A
I_{TSM} at 60 Hz	5510 A
I_{GT}	200 mA
T_C/T_{hs}	55 °C

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		370	A
	T_{hs}	55	°C
$I_{T(RMS)}$		700	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	5260	A
	60 Hz	5510	
I^2t	50 Hz	138	kA ² s
	60 Hz	126	
V_{DRM}/V_{RRM}		1000 to 1200	V
t_q	Range	20 to 30	µs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST203C..C	10	1000	1100	40
	12	1200	1300	



CURRENT CARRYING CAPABILITY							
FREQUENCY							UNITS
50 Hz	860	750	1340	1160	5620	5020	A
400 Hz	840	706	1400	1220	2940	2590	
1000 Hz	700	580	1350	1170	1750	1520	
2500 Hz	430	340	980	830	910	780	
Recovery voltage V_r	50		50		50		V
Voltage before turn-on V_d	V_{DRM}		V_{DRM}		V_{DRM}		
Rise of on-state current dI/dt	50		-		-		A/ μ s
Heatsink temperature	40	55	40	55	40	55	$^{\circ}$ C
Equivalent values for RC circuit	47/0.22		47/0.22		47/0.22		Ω/μ F

ON-STATE CONDUCTION							
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS		
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled		370 (140)	A		
				55 (85)	$^{\circ}$ C		
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled		700			
Maximum peak, one half cycle, non-repetitive surge current	I_{TSM}		Sinusoidal half wave, initial $T_J = T_J$ maximum	$t = 10$ ms	No voltage reapplied	5260	A
				$t = 8.3$ ms	No voltage reapplied	5510	
				$t = 10$ ms	100 % V_{RRM} reapplied	4420	
				$t = 8.3$ ms	100 % V_{RRM} reapplied	4630	
Maximum I^2t for fusing	I^2t		Sinusoidal half wave, initial $T_J = T_J$ maximum	$t = 10$ ms	No voltage reapplied	138	kA ² s
				$t = 8.3$ ms	No voltage reapplied	126	
				$t = 10$ ms	100 % V_{RRM} reapplied	98	
				$t = 8.3$ ms	100 % V_{RRM} reapplied	89	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1$ to 10 ms, no voltage reapplied		1380	kA ² \sqrt{s}		
Maximum peak on-state voltage	V_{TM}	$I_{TM} = 600$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine wave pulse		1.72	V		
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7 \% \times \pi \times I_{T(AV)}) < I < \pi \times I_{T(AV)}$, $T_J = T_J$ maximum		1.17			
High level value of threshold voltage	$V_{T(TO)2}$	$I > \pi \times I_{T(AV)}$, $T_J = T_J$ maximum		1.22			
Low level value of forward slope resistance	r_{t1}	$(16.7 \% \times \pi \times I_{T(AV)}) < I < \pi \times I_{T(AV)}$, $T_J = T_J$ maximum		0.92	m Ω		
High level value of forward slope resistance	r_{t2}	$I > \pi \times I_{T(AV)}$, $T_J = T_J$ maximum		0.83			
Maximum holding current	I_H	$T_J = 25$ °C, $I_T > 30$ A		600	mA		
Typical latching current	I_L	$T_J = 25$ °C, $V_A = 12$ V, $R_a = 6$ Ω , $I_G = 1$ A		1000			

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum non-repetitive rate of rise of turned on current	dI/dt	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$ $I_{TM} = 2 \times dI/dt$		1000	A/ μ s
Typical delay time	t_d	$T_J = 25$ °C, $V_{DM} = \text{Rated } V_{DRM}$, $I_{TM} = 50$ A DC, $t_p = 1$ μ s Resistive load, gate pulse: 10 V, 5 Ω source		0.8	μ s
Maximum turn-off time	t_q	$T_J = T_J$ maximum, $I_{TM} = 300$ A, commutating $dI/dt = 20$ A/ μ s		20	
		$V_R = 50$ V, $t_p = 500$ μ s, dV/dt : See table in device code		30	



BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % V_{DRM} , higher value available on request	500	V/ μ s
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	40	mA

TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, f = 50 Hz, d % = 50	60	W
Maximum average gate power	$P_{G(AV)}$		10	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	A
Maximum peak positive gate voltage	+ V_{GM}		20	
Maximum peak negative gate voltage	- V_{GM}		5	
Maximum DC gate current required to trigger	I_{GT}	$T_J = 25$ °C, $V_A = 12$ V, $R_a = 6$ Ω	200	mA
Maximum DC gate voltage required to trigger	V_{GT}		3	V
Maximum DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied	20	mA
Maximum DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T_J		- 40 to 125	°C
Maximum storage temperature range	T_{Stg}		- 40 to 150	
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled	0.17	K/W
		DC operation double side cooled	0.08	
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled	0.033	
		DC operation double side cooled	0.017	
Mounting force, ± 10 %			4900 (500)	N (kg)
Approximate weight			50	g
Case style		See dimensions - link at the end of datasheet	A-PUK (TO-200AB)	

ΔR_{thJ-hs} CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.015	0.017	0.011	0.011	$T_J = T_J$ maximum	K/W
120°	0.018	0.019	0.019	0.019		
90°	0.024	0.024	0.026	0.026		
60°	0.035	0.035	0.036	0.037		
30°	0.060	0.060	0.060	0.061		

Note

- The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

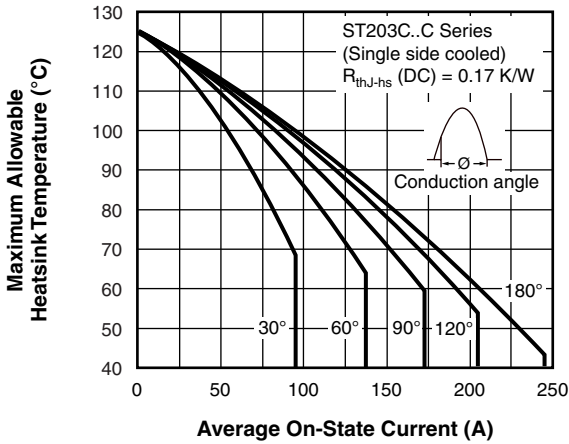


Fig. 1 - Current Ratings Characteristics

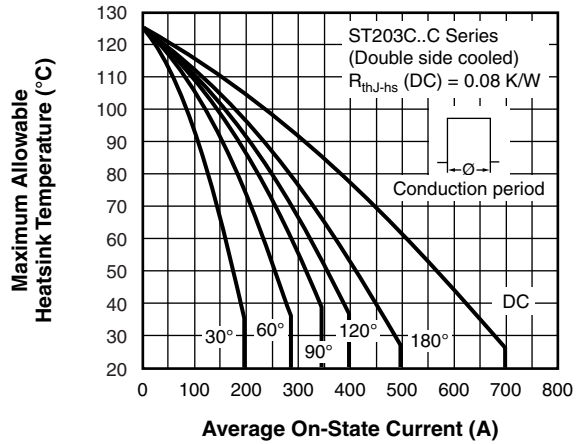


Fig. 4 - Current Ratings Characteristics

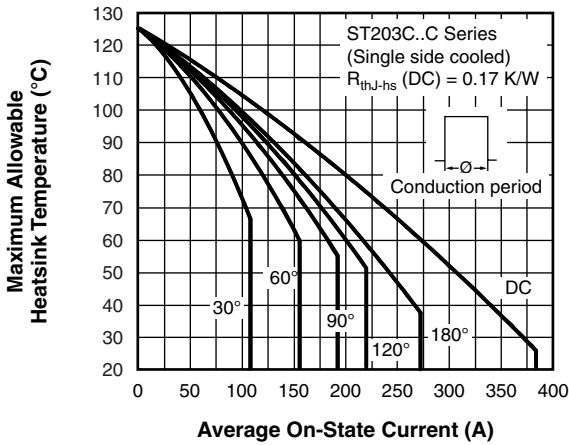


Fig. 2 - Current Ratings Characteristics

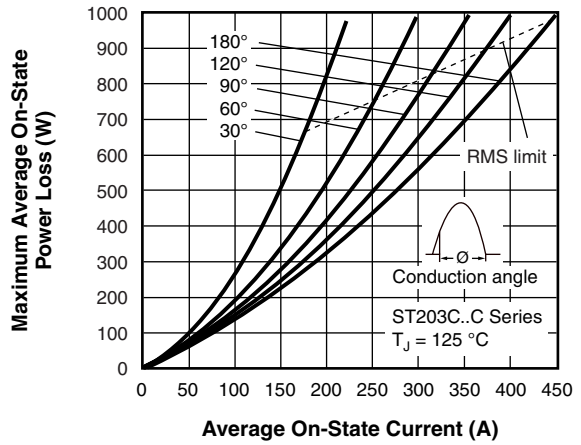


Fig. 5 - On-State Power Loss Characteristics

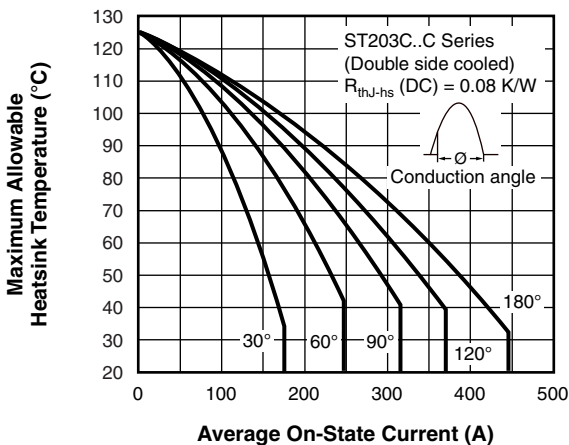


Fig. 3 - Current Ratings Characteristics

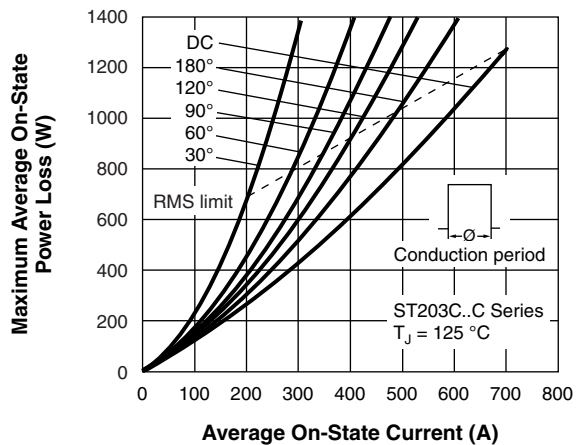


Fig. 6 - On-State Power Loss Characteristics

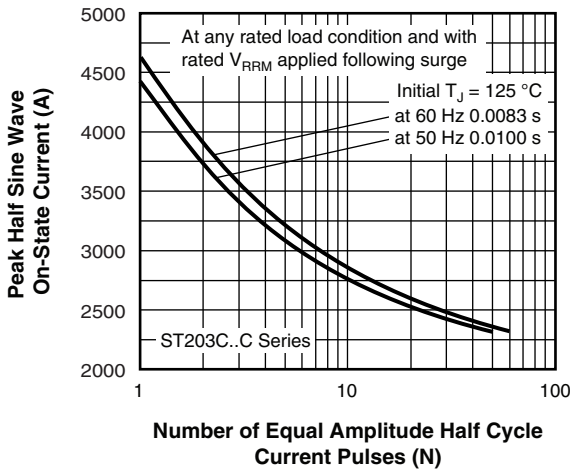


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

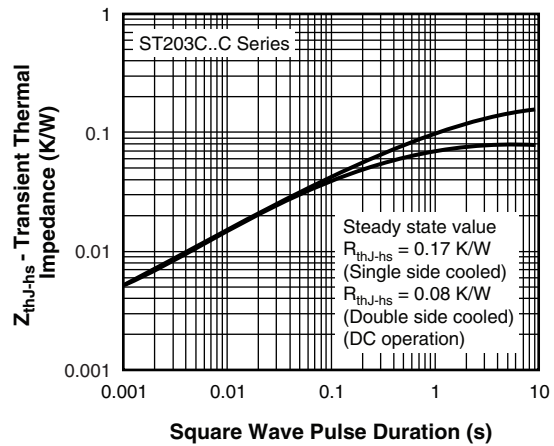


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

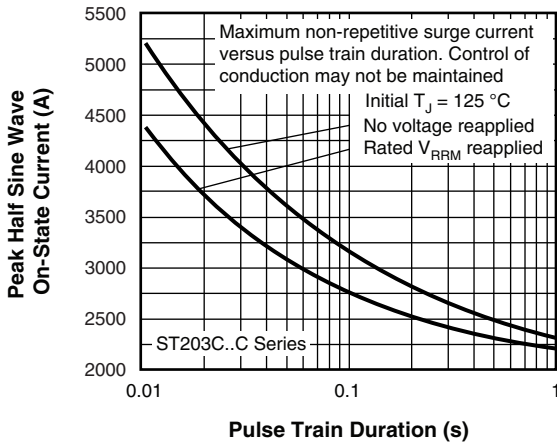


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

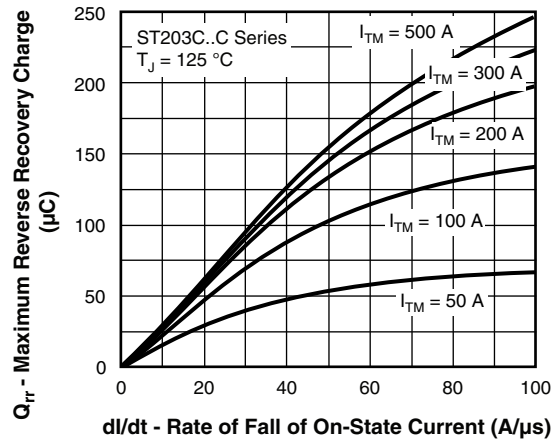


Fig. 11 - Reverse Recovered Charge Characteristics

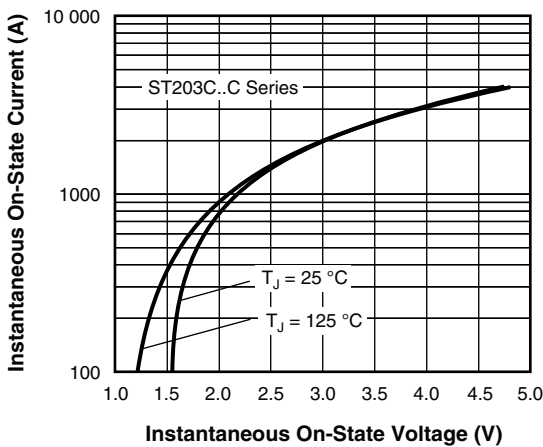


Fig. 9 - On-State Voltage Drop Characteristics

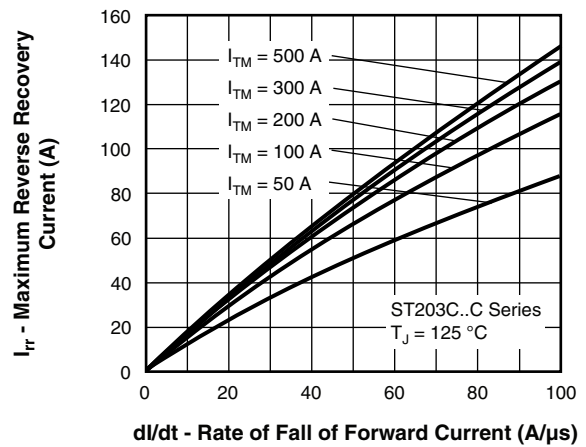


Fig. 12 - Reverse Recovery Current Characteristics

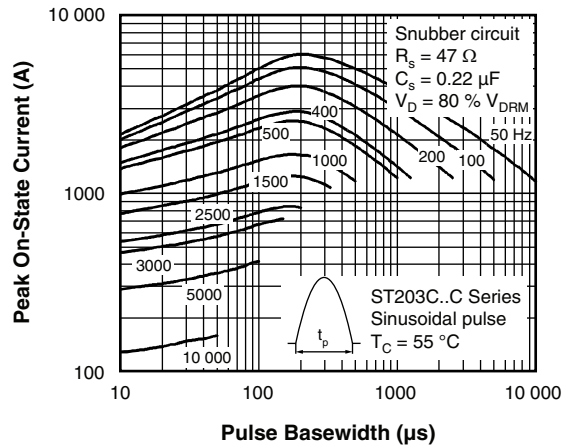
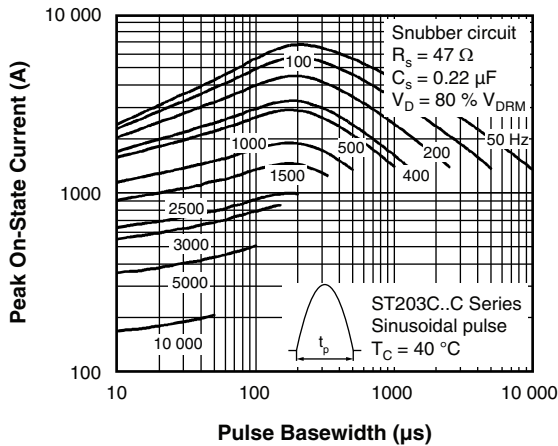


Fig. 13 - Frequency Characteristics

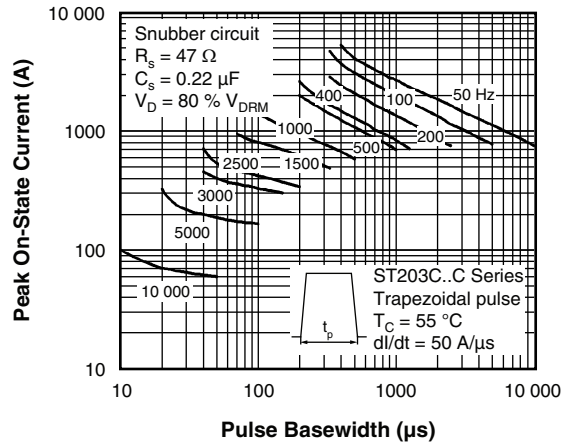
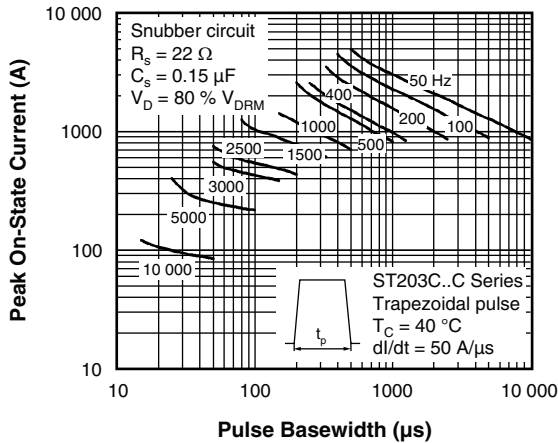


Fig. 14 - Frequency Characteristics

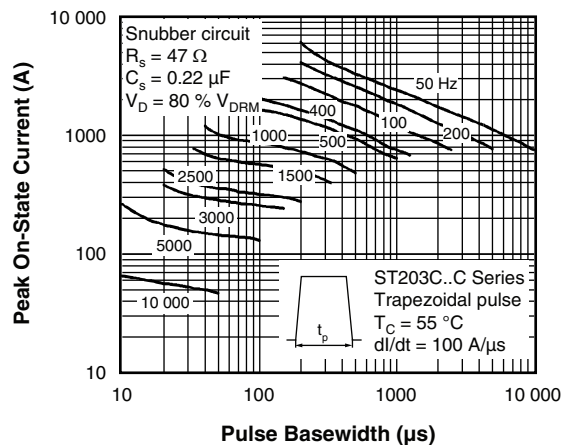
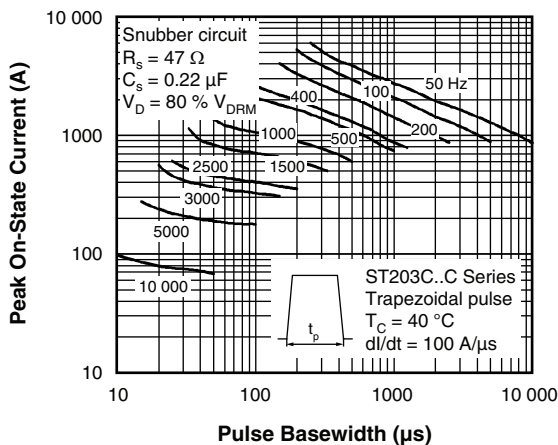


Fig. 15 - Frequency Characteristics

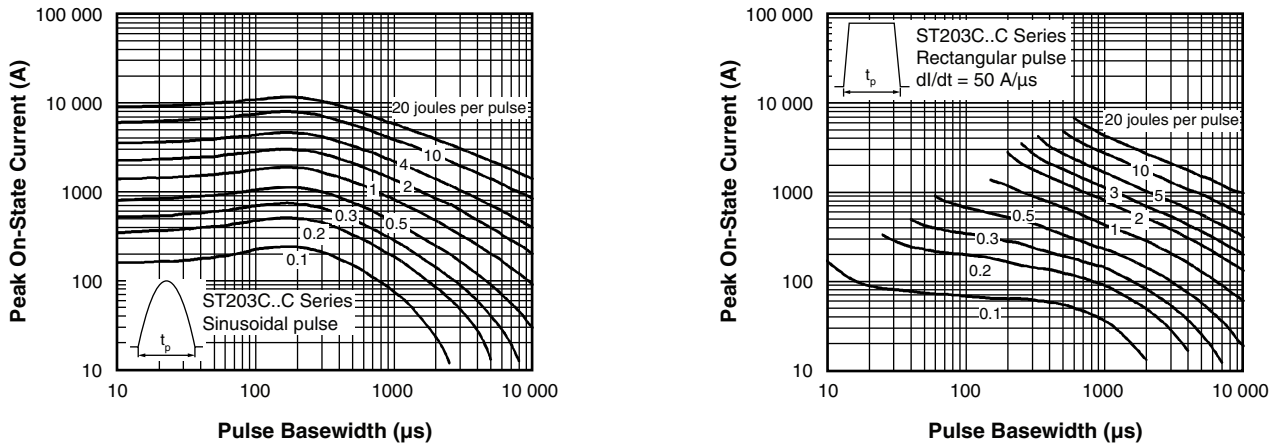


Fig. 16 - Maximum On-State Energy Power Loss Characteristics

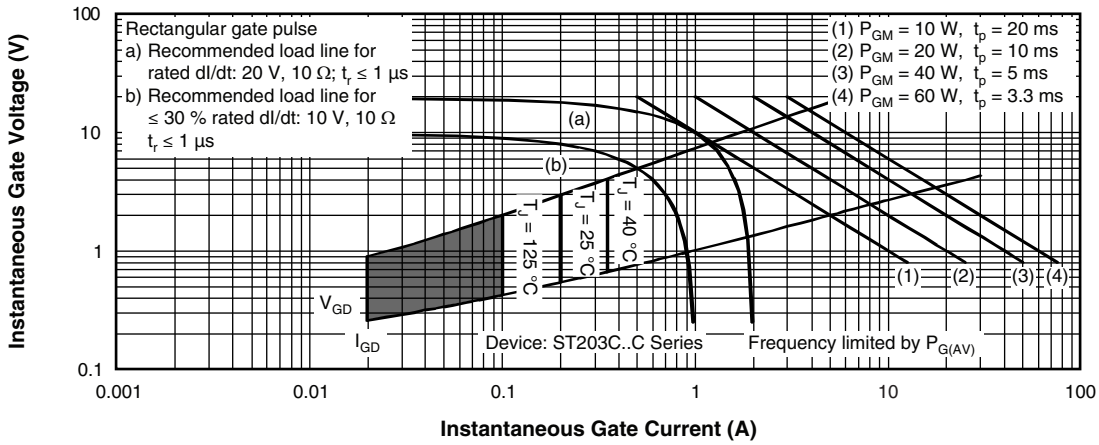
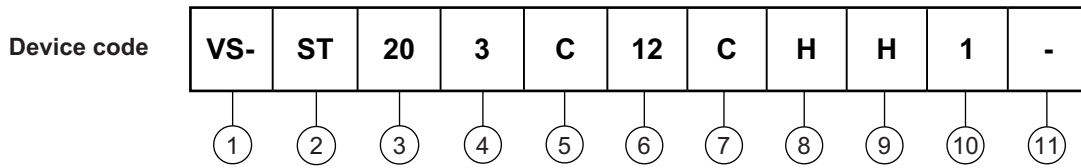


Fig. 17 - Gate Characteristics



ORDERING INFORMATION TABLE



- 1** - Vishay Semiconductors product
- 2** - Thyristor
- 3** - Essential part number
- 4** - 3 = fast turn-off
- 5** - C = ceramic PUK
- 6** - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
- 7** - C = PUK case A-PUK (TO-200AB)
- 8** - Reapplied dV/dt code (for t_q test condition)
- 9** - t_q code
- 10** - 0 = eyelet terminals

dV/dt - t_q combinations available						
dV/dt (V/μs)		20	50	100	200	400
t_q (μs)	20	CK	DK	EK	-	-
	25	CJ	DJ	EJ	FJ*	-
	30	CH	DH	EH	FH	HH

- 10** - 0 = eyelet terminals
(gate and auxiliary cathode unsoldered leads)
- 1 = fast-on terminals
(gate and auxiliary cathode unsoldered leads)
- 2 = eyelet terminals
(gate and auxiliary cathode soldered leads)
- 3 = fast-on terminals
(gate and auxiliary cathode soldered leads)
- 11** - Critical dV/dt:
 - None = 500 V/ μ s (standard value)
 - L = 1000 V/ μ s (special selection)

* Standard part number.
All other types available only on request.

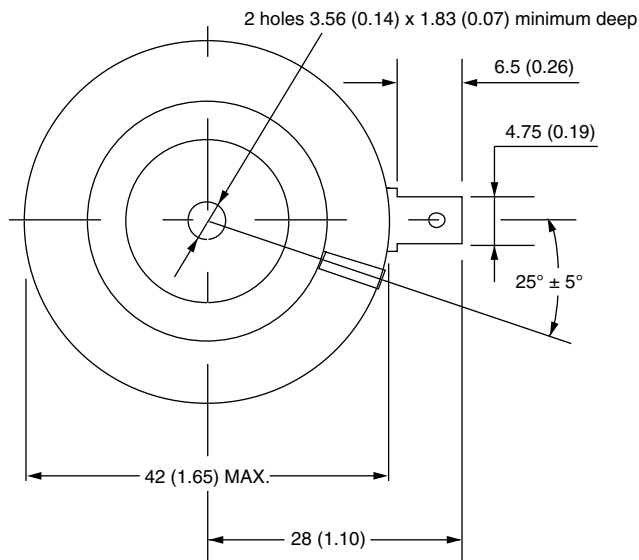
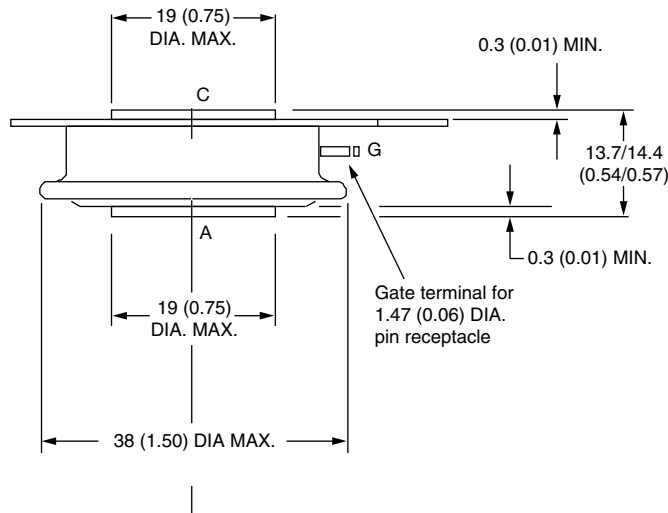
LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95074



A-PUK (TO-200AB)

DIMENSIONS in millimeters (inches)

Anode to gate
Creepage distance: 7.62 (0.30) minimum
Strike distance: 7.12 (0.28) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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