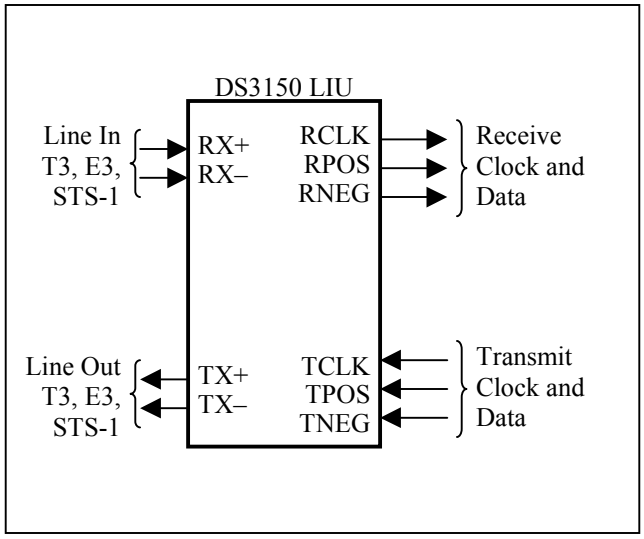
DALLAS SEMICONDUCTOR

DS3150
3.3V T3 / E3 / STS-1 Line Interface

FEATURES

- Integrated transmit and receive for T3, E3 and STS-1 line interfaces
- Performs clock/data recovery and wave shaping
- Requires no special external components other than 1:2 transformers
- Interfaces to 75Ω coaxial cable at lengths up to 380 meters (T3), 440 meters (E3), or 360 meters (STS-1)
- Adaptive receive equalizer handles from 0 dB to 15 dB of cable loss
- Interfaces directly to a DSX monitor signal (20 dB flat loss)
- On-chip jitter attenuator can be placed either in the receive path or the transmit path
- Built-in B3ZS and HDB3 coder/decoder
- Bipolar and NRZ interfaces
- Analog and digital loopbacks
- Onboard $2^{15} - 1$ and $2^{23} - 1$ Pseudo Random Bit Sequence (PRBS) generator and detector
- Transmit line driver monitor checks for a faulty transmitter or a shorted output
- Complete T3 AIS generator (ANSI T1.107)
- Unframed all ones generator (E3 AIS)
- Digital clock inversion capability
- Tri-state line driver for low-power mode
- Loss of signal detector (ANSI T1.231-1999 and ITU G.775)
- Pin compatible to the TDK 78P7200 and 78P2241 footprint
- Low power 3.3V operation (5V tolerant I/O)
- Industrial temperature range: -40°C to +85°C
- Small packaging: 28-lead PLCC, 48-lead TQFP and 49-lead CSBGA (7 x 7 mm)

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

DS3150QN	28-lead PLCC	(-40°C to +85°C)
DS3150Q	28-lead PLCC	(0°C to 70°C)
DS3150TN	48-lead TQFP	(-40°C to +85°C)
DS3150T	48-lead TQFP	(0°C to 70°C)
DS3150GN	49-lead CSBGA	(-40°C to +85°C)
DS3150G	49-lead CSBGA	(0°C to 70°C)

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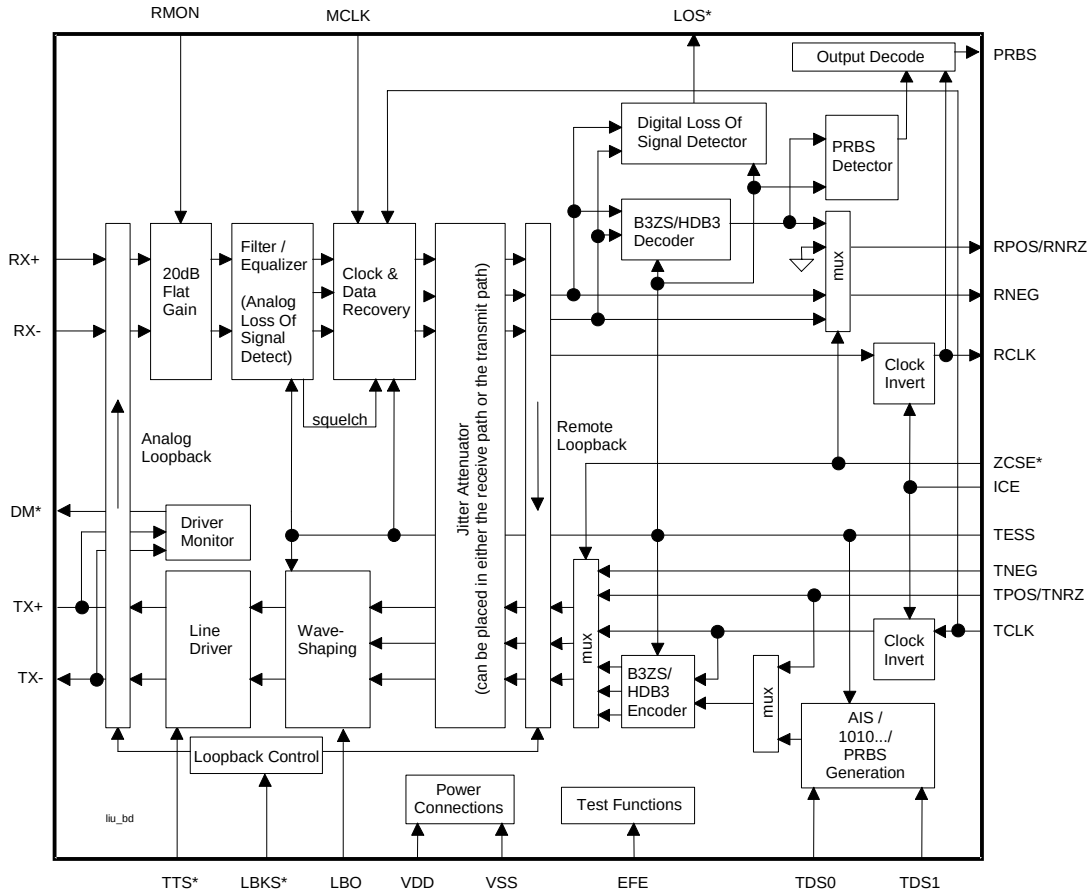
SECTION 1: FUNCTIONAL DESCRIPTION

The DS3150 performs all of the functions necessary for interfacing at the physical layer to T3, E3, and STS-1 lines. The device has independent receive and transmit paths. See Figure 1A. The receiver performs clock and data recovery from a B8ZS- or HDB3-code AMI signal and monitors for loss of the incoming signal. The recovered data optionally can be B8ZS/HDB3 decoded and output in NRZ format. The transmitter accepts either NRZ or bipolar data and drives standard pulse-shape waveforms onto 75 ohm coaxial cable. The receiver and transmitter sections will be discussed separately below. Table 1A lists the telecommunications standards that the DS3150 was designed to meet.

DS3150 Block Diagram Figure 1A



Applicable Standards Table 1A

T1.102-1993	(ANSI) "Digital Hierarchy – Electrical Interfaces"
T1.107-1995	(ANSI) "Digital Hierarchy - Formats Specification"
T1.231-1997	(ANSI) Draft "Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring"
T1.231-1993	(ANSI) "Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring"
T1.404-1994	(ANSI) "Network-to-Customer Installation - DS3 Metallic Interface Specification"
GR-499-CORE	(Bellcore) Issue 1, December1995 "Transport Systems Generic Requirements (TSGR): Common Requirements"
GR-253-CORE	(Bellcore) Issue 2, December 1995 "SONET Transport Systems: Common Generic Criteria"
G.703, 1991	(ITU) "Physical/Electrical Characteristics of Hierarchical Digital Interfaces
G.751, 1993	(ITU) "Digital Multiplex Equipment Operating at the Third Order Bit Rate of 34,368 kbit/s and the Fourth Order bit Rate of 139,264 kbit/s and Using Postive Justification"
G.823, 1993	(ITU) "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy"
G.775, 1994	(ITU) "Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria"
O.151, 1992	(ITU)"Error Performance Measuring Equipment Operating at the Primary Rate and Above"
TBR 24, 1997	(ETSI) "Business TeleCommunications; 34Mbit/s digital unstructured and structured lease lines; attachment requirements for terminal equipment interface
ETS 300 687, 1996	(ETSI) "Business TeleCommunications; 34Mbit/s digital leased lines (D34U and D34S); Connection characteristics
ETS 300 686, 1996	(ETSI) "Business TeleCommunications; 34Mbit/s and 140Mbits/s digital leased lines (D34U, D34S, D140U and D140S); Network interface presentation

RECEIVER

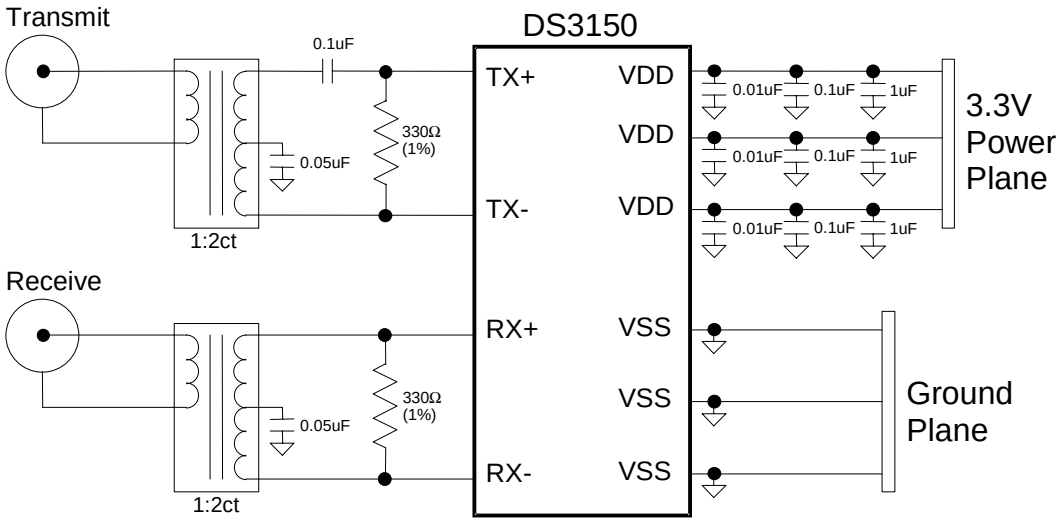
The DS3150 interfaces to the receive T3/E3/STS-1 coax line via a 1:2 step up transformer. See Figure 1B. The receiver automatically adapts to coax cable loses from 0 to 15 dB which translates into 0 to 380 meters (T3) or 440 meters (E3) or 360 meters (STS-1) of coax cable (AT&T 734A or equivalent). The receiver has the ability to interface to monitor jacks as well. Via the RMON input (see Table 2A), the device can be configured to insert a 20 dB flat boost into the incoming signal. Monitor jacks typically have series resistors that result in a resistive loss of 20 dB. The receiver has excellent jitter tolerance characteristics. See Figure 1C.

The receiver contains both analog and digital loss-of-signal detectors. The analog loss of signal detector resides in the equalizer. If the incoming signal drops below –24 dB of the nominal signal level, the analog loss-of-signal detector will activate and it will step on the recovered data and force all zeros out of the data recovery circuitry. The analog loss-of-signal detector will not clear until the signal level is above -18 dB of the nominal signal level. The digital Loss of Signal (LOS) detector is activated when it detects 192±1 consecutive zeros. LOS is cleared when there are no Excessive Zero occurrences over a span of 192±1 clock periods. An Excessive Zero occurrence is defined as 3 or more consecutive zeros in the T3 and STS-1 modes and 4 or more zeros in the E3 mode. The status of the digital LOS is reflected at the LOS* output (see Table 2A). There is no status output available for the analog loss-of-signal detector. While the device is in a loss-of-signal state, the RCLK output will be referenced to the MCLK input (or the TCLK input if MCLK is high/floating or to the internal oscillator if MCLK is tied low). The analog

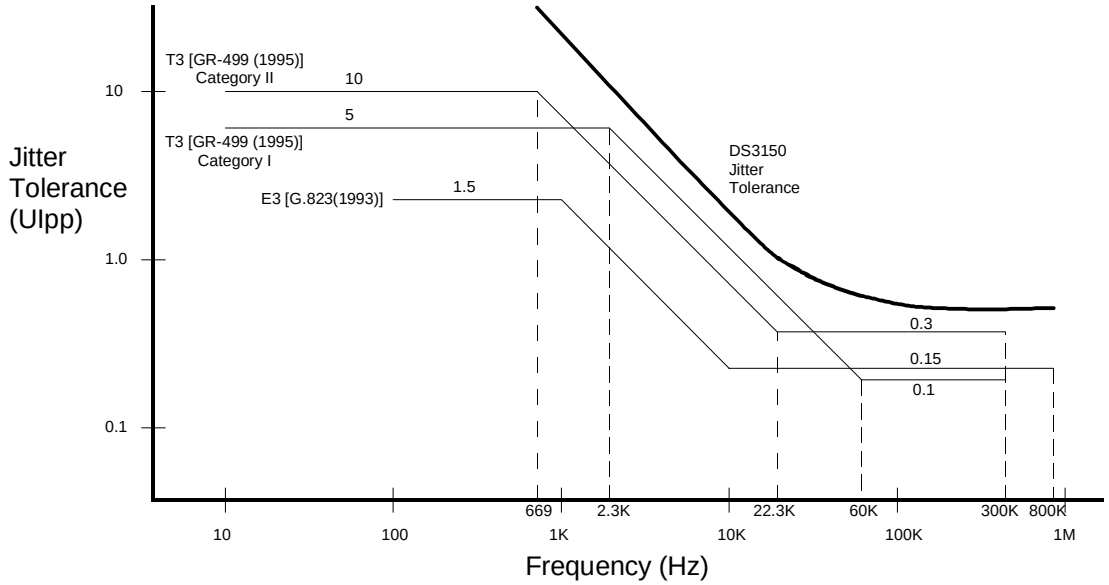
loss-of-signal detector has a longer time constant than the digital LOS. Hence when the incoming signal is lost, the digital LOS will activate first followed by the analog loss-of-signal detector. When a signal is restored, the digital LOS will not be allowed to qualify a signal for no Excessive Zero violations until the analog loss-of-signal detector has seen the signal rise above –18 dB. Governing specifications for the loss-of-signal detectors are ANSI T1.231 and ITU G.775.

The recovered data from the receiver can be output in either bipolar format or a Non Return to Zero (NRZ) format. To select the bipolar format, the ZCSE* input is tied high. In this format, the B3ZS/HDB3 decoder is disabled and the received data is buffered and then output on the RPOS and RNEG outputs. To select the NRZ format, the ZCSE* input is tied low. In this format, the B3ZS/HBD3 decoder is enabled and the recovered data is B3ZS/HDB3 decoded and then logically OR'ed together and output at the RPOS output while the RNEG output is forced low.

DS3150 EXTERNAL CONNECTION Figure 1B



DS3150 RECEIVER JITTER TOLERANCE Figure 1C



TRANSMITTER

Via the ZCSE* input, the device is configured to accept either bipolar data or NRZ data to be input to the transmitter. When the ZCSE* input is tied high, bipolar data must be applied at the TPOS and TNEG inputs. In this mode, the device will not perform B3ZS/HDB3-encoding on the outgoing data stream. When the ZCSE* input is tied low, an NRZ data stream must be applied at the TPOS input (TNEG is ignored). In this mode, the device will perform B3ZS/HDB3-encoding on the outgoing data stream.

The clock applied at the TCLK input is used to transmit data onto the T3/E3/STS-1 line. Hence TCLK must be of transmission quality (i.e. accurate to ±20 ppm). The duty cycle of TCLK is not a key parameter as long as the clock high and low times listed in Section 3 are met.

The DS3150 also has the ability to generate a number of different patterns, including an unframed all ones pattern (which is also the E3 AIS signal), a 101010… pattern, or a T3 Alarm Indication Signal (AIS). See Figure 1E for a description of the T3 AIS. The TDS0 and TDS1 inputs are used to select these onboard patterns. See Tables 2A and 2B.

The DS3150 interfaces to the transmit T3/E3/STS-1 coax cable via a 1:2 step up transformer. See Figure 1B. It will drive the 75 ohm cable and create the proper waveforms required for interfacing to T3/E3/STS-1 lines. In T3 and STS-1 modes, the LBO (Line Build-Out) pin controls waveform shape. For cable lengths less than 225 feet, LBO should be pulled high. For 225 feet or more of cable, LBO should be pulled low. Tables 1C through 1G and Figure 1D detail the waveform template specifications and testing parameters.

The transmitter can be disabled and the TX+ and TX– outputs tri-stated via the TTS* input. See Table 2A for details.

The transmit driver monitor constantly checks the analog signal output at TX+ and TX–. If the output fails, then the DM* output will be pulled low. See Figures 1F and 1G. When the transmitter is disabled (TTS* = 0) or enhanced features are disabled (EFE=0), the driver monitor is also disabled.

T3 TRANSMIT WAVEFORM TEMPLATE Table 1C

Time Axis Range	Normalized Amplitude Equations
Upper Curve	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.36$	$0.5\ \{1 + \sin[(\pi/2)(1 + T/0.34)]\} + 0.03$
$0.36 \le T \le 1.4$	$0.08 + 0.407e^{-1.84(T - 0.36)}$
Lower Curve	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le 0.36$	$0.5\ \{1 + \sin[(\pi/2)(1 + T/0.18)]\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

Governing Specifications: ANSI T1.102-1993 and Bellcore GR-499.

T3 TRANSMIT WAVEFORM TEST PARAMETERS AND LIMITS Table 1D

Parameter	Specification
Rate	44.736 Mbit/s (± 20 ppm)
Line code	B3ZS
Transmission medium	coax cable (AT&T 734A or equivalent)
Test measurement point	At the end of 0 to 450 feet of coax cable
Test termination	75Ω (± 1%) resistive
Pulse amplitude	Between 0.36V and 0.85V
Pulse shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the curved listed in Table 1C
Unframed All Ones Power level @ 22.368 MHz	Between –1.8 dBm and +5.7 dBm
Unframed All Ones Power level @ 44.736 MHz	At least 20 dB less than the power measured at 22.368 MHz
Pulse imbalance of isolated pulses	Ratio of positive and negative pulses must be between 0.90 and 1.10

STS-1 TRANSMIT WAVEFORM TEMPLATE Table 1E

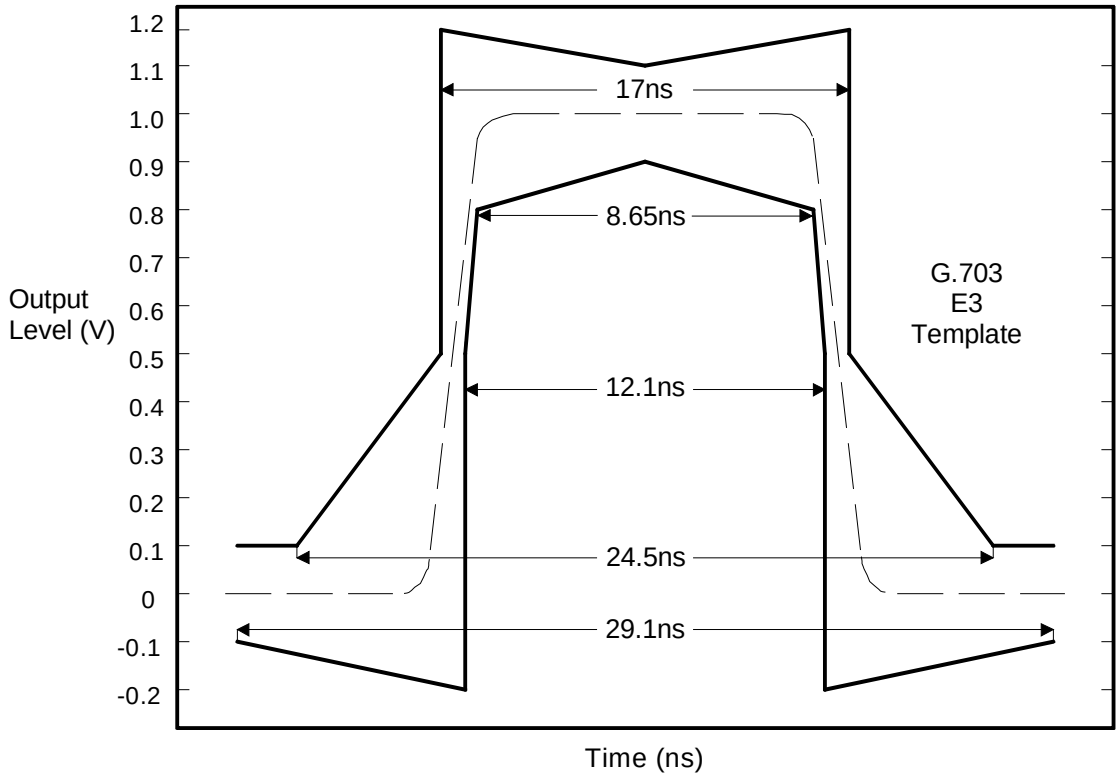
Time Axis Range	Normalized Amplitude Equations
Upper Curve	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.26$	$0.5\ \{1 + \sin[(\pi/2)(1 + T/0.34)]\} + 0.03$
$0.26 \le T \le 1.4$	$0.1 + 0.61e^{-2.4(T - 0.26)}$
Lower Curve	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le 0.36$	$0.5\ \{1 + \sin[(\pi/2)(1 + T/0.18)]\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

Governing Specifications: Bellcore GR-253 and Bellcore GR-499.

STS-1 TRANSMIT WAVEFORM TEST PARAMETERS AND LIMITS Table 1F

Parameter	Specification
Rate	51.840 Mbit/s (± 20 ppm)
Line code	B3ZS
Transmission medium	coax cable (AT&T 734A or equivalent)
Test measurement point	At the end of 0 to 450 feet of coax cable
Test termination	75Ω (± 1%) resistive
Pulse shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the curved listed in Table 1E
Unframed All Ones Power level @ 25.92 MHz	Between –1.8 dBm and +5.7 dBm
Unframed All Ones Power level @51.84 MHz	At least 20 dB less than the power measured at 25.92 MHz

E3 TRANSMIT WAVEFORM TEMPLATE Figure 1D



E3 TRANSMIT WAVEFORM TEST PARAMETERS AND LIMITS Table 1G

Parameter	**Specification**
Rate	34.368 Mbit/s (± 20 ppm)
Line code	HDB3
Transmission medium	coax cable (AT&T 734A or equivalent)
Test measurement point	At the transmitter
Test termination	75Ω (± 1%) resistive
Pulse amplitude	1.0V (nominal)
Pulse shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the template shown in Figure 1D
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05

T3 AIS STRUCTURE Figure 1E

M1 Subframe

X1 (1)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M2 Subframe

X2 (1)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M3 Subframe

P1 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M4 Subframe

P2 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M5 Subframe

M1 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M6 Subframe

M2 (1)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M7 Subframe

M3 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

NOTES:

X1 is transmitted first.

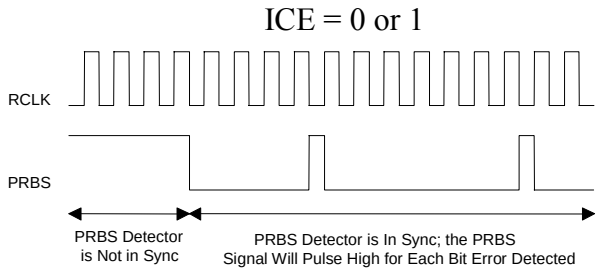
The 84 Info Bits are the sequence 101010… where the one (“1”) starts after each X, P, F, C, or M bit.

DIAGNOSTICS

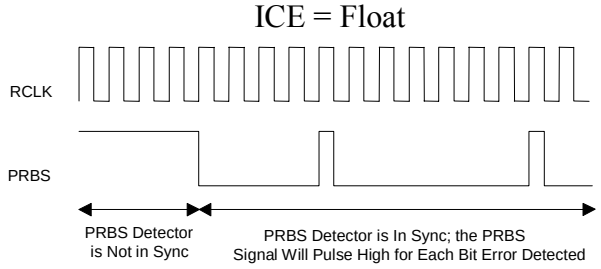
The DS3150 contains an onboard Pseudo Random Binary Sequence (PRBS) generator and detector. This function is useful in testing the device at the physical layer. It will generate and detect either a $2^{15} - 1$ (T3 or STS-1) or $2^{23} - 1$ PRBS according to the ITU O.151 specification. The PRBS pattern generated and detected by the DS3150 is an unframed pattern. In other words, no T3, E3, or STS-1 framing patterns are inserted in the transmit data stream nor expected in the received data stream. The PRBS generator is enabled via the TDS0 and TDS1 inputs. See Tables 2A and 2B for details. The PRBS detector is always enabled and will report it's status via the PRBS output if signal EFE = 1. When the PRBS detector is out of synchronization, the PRBS output will be forced high. When the PRBS detector synchronizes to the incoming pseudorandom pattern, the PRBS output will go low and then pulse high for each bit detected in error. See Figures 1F and 1G. On the receive side, the recovered data is B3ZS/HDB3 decoded before it is routed to the PRBS decoder.

The DS3150 also has two internal loopbacks that can be used for testing. See Figure 1A. The Analog Loopback loops the outgoing transmit waveform back to the receiver. When this loopback is enabled, data will be transmitted as it normally would be and the incoming data at RX+ and RX– is ignored. The Remote Loopback loops data from the receive side to the transmit side. When this loopback is enabled, data will continue to pass through the receive side as it normally would and data at the TPOS and TNEG inputs is ignored. These two loopbacks are invoked via the LBKS* input. See Table 2A.

PRBS OUTPUT WITH NORMAL RCLK OPERATION Figure 1F



PRBS OUTPUT WITH INVERTED RCLK OPERATION Figure 1G



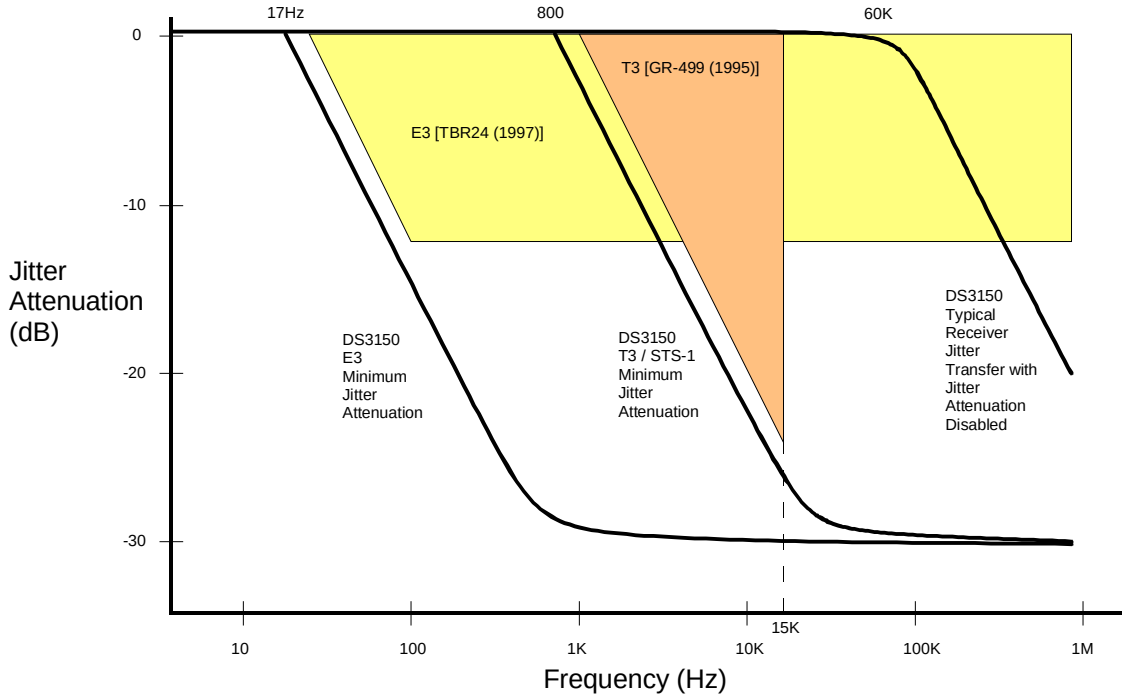
JITTER ATTENUATOR

The DS3150 contains an onboard jitter attenuator that can be placed in either the receive path or the transmit path or disabled. This selection is made via the RMON and TTS* input signals. See Table 1H below for details. Figure 1H shows the minimum jitter attenuation for the device when the jitter attenuator is enabled. Figure 1H also shows the receive jitter transfer when the jitter attenuator is disabled. Depending on whether the device is in the T3/STS-1 or E3 mode, the jitter attenuation will be adjusted. Note that for best results, a highly accurate clock source should be present at MCLK (or at TCLK if MCLK is tied high or left floating).

RMON & TTS* SIGNAL DECODE Table 1H

RMON	TTS*	Receive 20 dB Flat Gain	Transmit Line Driver	Jitter Attenuator
0	0	disabled	tri-stated	disabled
0	1	disabled	enabled	disabled
0	Float	disabled	enabled	enabled in TX path
1	0	enabled	tri-stated	disabled
1	1	enabled	enabled	disabled
1	Float	enabled	enabled	enabled in TX path
Float	0	disabled	tri-stated	enabled in RX path
Float	1	disabled	enabled	enabled in RX path
Float	Float	disabled	enabled	enabled in RX path

DS3150 JITTER ATTENUATION / JITTER TRANSFER Figure 1H



SECTION 2: SIGNAL DESCRIPTIONS

Table 2A below lists all of the signals on the DS3150 and their function. The signals are listed in alphabetical order. Section 4 shows the signal pin assignments for each package option.

SIGNAL DESCRIPTIONS Table 2A

Signal Name	I/O	Description
DM*	O	Driver Monitor (active low, open drain). This signal reports the status of the transmit driver monitor. When the transmit driver monitor detects a faulty transmitter, this pin is pulled low. This pin should have an external pull-up to V_{DD}. This signal is not bonded out in the PLCC package.
EFE	I3	Enhanced Feature Enable. This signal enables the enhanced DS3150 features (PRBS generation/detection; transmit driver monitor; and transmission of all ones, T3 AIS or the 1010… pattern). 0 = Enhanced Features Disabled: TDS0 and TDS1 ignored, PRBS/DM tri-stated 1 = Enhanced Features Enabled: TDS0, TDS1 and PRBS/DM active Float = Test Mode Enabled: TDS0, TDS1, LBO, LOS* redefined as test pins
ICE	I3	Invert Clock Enable. This signal determines on which RCLK edge RPOS and RNEG are updated and on which TCLK edge TPOS and TNEG are sampled. 0 = Normal RCLK / Normal TCLK: update RPOS/RNRZ and RNEG on falling edge of RCLK and sample TPOS/TNRZ and TNEG on rising edge of TCLK 1 = Normal RCLK / Inverted TCLK: update RPOS/RNRZ and RNEG on falling edge of RCLK and sample TPOS/TNRZ and TNEG on falling edge of TCLK Float = Inverted RCLK / Inverted TCLK: update RPOS/RNRZ & RNEG on rising edge of RCLK and sample TPOS/TNRZ and TNEG on falling edge of TCLK
LBKS*	I3	Loopback Select. This input determines if either the Analog Loopback or the Remote Loopback is enabled. See the Block Diagram in Section 1 for details. 0 = Analog Loopback Enabled 1 = No Loopback Enabled Float = Remote Loopback Enabled
LBO	I	Line Build-Out. This input indicates cable length for waveform shaping in DS3 and STS-1 modes. LBO is ignored for E3 mode. 0 = Cable length less than 225 feet. 1 = Cable length greater than or equal to 225 feet.
LOS*	O	Loss Of Signal (active low). This signal will be asserted upon detection of 192±1 consecutive zeros. Signals lower than 21dB below nominal are squelched. LOS* is deasserted when there are no Excessive Zero occurrences over a span of 192±1 clock periods. An Excessive Zero occurrence is defined as 3 or more consecutive zeros in the T3 and STS-1 modes or 4 or more zeros in the E3 mode. Governing Specifications are ANSI T1.231 and ITU G.775.
MCLK	I	Master Clock. The clock input at this signal is used by the clock and data recovery machine. A T3 (44.736 MHz ± 20 ppm), E3 (34.368 MHz ± 20 ppm), or STS-1 (51.840 MHz ± 20 ppm) clock should be applied at this signal. Tying this pin high or leaving it floating forces the device to use the clock applied at the TCLK input for the receive side clock and data recovery. Tying this pin low enables an internal oscillator. The frequency of this oscillator is determined by a resistor placed between OFSEL and VSS. MCLK has an internal 15 kΩ pull-up resistor to V_{DD}.

SIGNAL DESCRIPTIONS Table 2A (cont.)

PRBS	O3	PRBS Detector. This signal reports the status of the PRBS Detector. The PRBS detector will constantly search for either a $2^{15} - 1$ (T3 or STS-1) or $2^{23} - 1$ (E3) psuedo random bit sequence. This signal will remain high when the PRBS detector is out of synchronization. When the PRBS detector syncs to the PRBS, this signal will go low and will create a high pulse (synchronous with RCLK) for each bit error detected. See Figures 1F and 1G for more details. If EFE = 0, then this signal is tri-stated. This signal is not bonded out in the PLCC package.
RCLK	O	Receive Clock. The recovered clock is output at this pin. When the DS3150 experiences a Loss Of Signal (LOS* = 0), the clock applied at MCLK (or TCLK if MCLK is high/floating or the internal oscillator if MCLK is tied low) appears at this signal. The recovered data is updated at the RPOS and RNEG outputs on either the falling edge of RCLK (ICE = 0 or 1) or the rising edge of RCLK (ICE = FLOAT).
RMON	I3	Receive Monitor Mode. This input determines whether or not a 20 dB flat gain will be applied to the incoming signal before it is fed to the receive equalizer. This mode is invoked when the device is being used to monitor signals that have been resistively attenuated by a monitor jack. In this mode, the maximum input signal allowed at RX+ and RX– is reduced by 20 dB. This input also controls the jitter attenuator. See Table 2C. 0 = disable the 20 dB gain, disable RX jitter attenuation 1 = enable the 20 dB gain, disable RX jitter attenuation Float = disable the 20 dB gain, enable RX jitter attenuation
RNEG	O	Receive Negative Data. When the B3ZS/HBD3 encoder/decoder is disabled (ZCSE* = 1), this signal indicates reception of a negative AMI pulse. When the B3ZS/HDB3 encoder/decoder is enabled (ZCSE* = 0), this signal will be forced low and the NRZ data stream will be output at RPOS. This signal will be updated either on the rising edge of RCLK (ICE = Float) or the falling edge of RCLK (ICE = 0 or 1) with the recovered data stream.
RPOS/ RNRZ	O	Receive Positive or NRZ Data. When the B3ZS/HBD3 encoder/decoder is disabled (ZCSE* = 1), this signal indicates reception of a positive AMI pulse. When the B3ZS/HDB3 encoder/decoder is enabled (ZCSE* = 0), this signal will contain the recovered NRZ data stream. This signal will be updated either on the rising edge of RCLK (ICE = Float) or the falling edge of RCLK (ICE = 0 or 1) with the recovered data stream.
RX+ RX–	I	Receive Analog Inputs. These differential AMI inputs are coupled to the T3, STS-1, or E3 75Ω coax line via a 1:2 step-up transformer. See Figure 1B for details.
TCLK	I	Transmit Clock. A T3 (44.736 MHz ± 20 ppm), E3 (34.368 MHz ± 20 ppm) or STS-1 (51.840 ± 20 ppm) clock should be applied at this signal. Data to be transmitted will be clocked into the device at TPOS/TNRZ and TNEG either on a rising edge of TCLK (ICE = 0) or falling edge of TCLK (ICE = 1 or FLOAT). The duty cycle on TCLK is not restricted as long it meets the high and low times listed in Section 3.
TDS0	I	Transmit Data Select Bit 0. If EFE = 1, this signal and signals TDS1 and TESS select the source of the transmit data (see Table 2B). If EFE = 0, this signal is ignored.

SIGNAL DESCRIPTIONS Table 2A (cont.)

TDS1/ OFSEL	I	Transmit Data Select Bit 1 / Oscillator Frequency Select. If EFE = 1, this pin (TDS1) and signals TDS0 and TESS select the source of the transmit data (see Table 2B). If MCLK is tied low, TDS1 is internally pulled low and a resistor connected between this pin (OFSEL) and ground determines the frequency of an internal oscillator. The following resistor values should be used for specific applications. E3: 6.81 kΩ T3: 5.23 kΩ STS1: 4.53 kΩ If EFE = 0, this signal is ignored.
TESS	I3	T3 / E3 / STS-1 Select. This input determines the mode of operation for the device. 0 = E3 1 = T3 Float = STS-1
TNEG	I	Transmit Negative Data. For bipolar data, the B3ZS/HDB3 encoder/decoder should be disabled (ZCSE* = 1) and TNEG should be driven high to generate a negative AMI pulse on the coax. For NRZ data, the B3ZS/HDB3 encoder/decoder should be enabled (ZCSE* = 0), the NRZ data stream should be applied to TNRZ, and TNEG is ignored and can be tied either high or low. TNEG is sampled either on the falling edge of TCLK (ICE = 1 or Float) or the rising edge of TCLK (ICE = 0).
TPOS/ TNRZ	I	Transmit Positive Data. For bipolar data, the B3ZS/HDB3 encoder/decoder should be disabled (ZCSE* = 1) and TPOS should be driven high to generate a positive AMI pulse on the coax. For NRZ data, the B3ZS/HDB3 encoder/decoder should be enabled (ZCSE* = 0), the NRZ data stream should be applied to TNRZ, and TNEG is ignored and can be tied either high or low. TPOS/TNRZ is sampled either on the falling edge of TCLK (ICE = 1 or Float) or the rising edge of TCLK (ICE = 0).
TTS*	I3	Transmit Tri-State. This input determines whether the TX+ and TX– analog output signals are forced into tri-state or are active. This input also controls the jitter attenuator. See Table 2C. 0 = tri-state the transmit output driver, disable TX jitter attenuation 1 = enable the transmit driver, disable TX jitter attenuation Float = enable the transmit driver, enable TX jitter attenuation
TX+ TX–	O3	Transmit Analog Outputs. These differential AMI outputs drive the T3, STS-1, or E3 signal into the 75Ω coax line. They are coupled to the coax line via a 2:1 step-down transformer. See Section 1 for details. These outputs can be tri-stated via the TTS* input signal.
V_{DD}	-	Positive Supply. 3.3V ± 5%. All V_{DD} signals should be tied together.
VSS	-	Ground Reference. All VSS signals should be tied together.
ZCSE*	I	Zero Code Suppression Enable. 0 = B3ZS/HDB3 encoder/decoder enabled (NRZ interface enabled) 1 = B3ZS/HDB3 encoder/decoder disabled (NRZ interface disabled)

NOTES:

- I3 indicates an input capable of detecting 3 states, high, low and float. All I3 input have a 10 kΩ pull-up to 1.5V.
- O3 indicates an output that is tri-state capable.
- Symbols appended with an asterisks (*) are active low signals.

TRANSMIT DATA MODE SELECT PIN DESCRIPTIONS Table 2B

TDS1	TDS0	TESS	Transmit Mode Selected
0	0	X	Transmit data normally as input at TPOS and TNEG
0	1	X	Transmit Unframed All Ones
1	0	0 or float	Transmit an Unframed 101010… pattern
1	0	1	Transmit T3 AIS as per ANSI T1.107 (see Figure 1E)
1	1	0	Transmit a $2^{23} – 1$ PRBS pattern as per ITU O.151
1	1	1 or float	Transmit a $2^{15} – 1$ PRBS pattern as per ITU O.151

NOTES:

TDS0 and TDS1 are ignored when EFE is tied low and the device will transmit TPOS / TNEG data

RMON & TTS* SIGNAL DECODE Table 2C

RMON	TTS*	Receive 20 dB Flat Gain	Transmit Line Driver	Jitter Attenuator
0	0	disabled	tri-stated	disabled
0	1	disabled	enabled	disabled
0	Float	disabled	enabled	enabled in TX path
1	0	enabled	tri-stated	disabled
1	1	enabled	enabled	disabled
1	Float	enabled	enabled	enabled in TX path
Float	0	disabled	tri-stated	enabled in RX path
Float	1	disabled	enabled	enabled in RX path
Float	Float	disabled	enabled	enabled in RX path

SECTION 3: AC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Lead with Respect to VSS (except V_{DD})	-0.3V to 5.5V
Supply Voltage (V_{DD}) with Respect to VSS	-0.3V to 3.63V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

NOTE:

The typical values listed below are not production tested.

RECOMMEND DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.4		5.5	V	
Logic 0	V_{IL}	-0.3		0.8	V	
Supply (V_{DD})	V_{DD}	3.135		3.465	V	

DC CHARACTERISTICS (-40°C to +85°C; VDD = 3.3V±5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current (V_{DD} = 3.465V)	I_{DD}		TBD		mA	1
Power Down Current (V_{DD} = 3.465V)	I_{PD}		TBD		mA	2
Lead Capacitance	C_{IO}		7		pF	
Input Leakage	I_{IL}	-10		+10	uA	3
Input Leakage (w/ pull-ups or float)	IILP	-500		+500	uA	3
Output Current (2.4V)	I_{OH}	-4.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. TCLK = MCLK = 44.736 MHz & TX+ and TX– driving all ones into a 75Ω load / other inputs at V_{DD} or grounded / other outputs left open circuited
2. MCLK = 44.736 MHz & TTS* = 0 / other inputs at V_{DD} or grounded / other outputs left open circuited
3. $0V < V_{IN} < V_{DD}$
4. Outputs in Tri-State

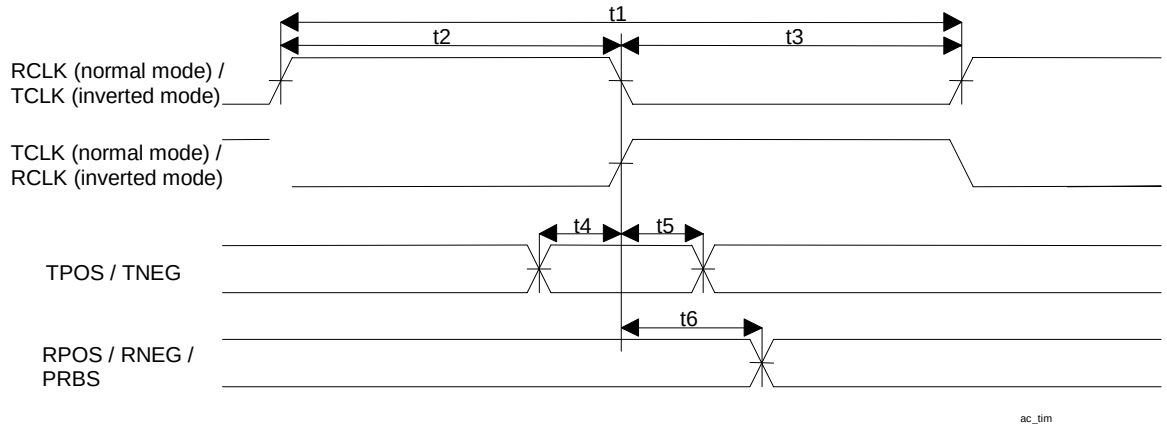
AC CHARACTERISTICS – DIGITAL (-40°C to +85°C; VDD = 3.3V±5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK / TCLK Clock Period	t1		22.4		ns	1
	t1		29.1		ns	2
	t1		19.3		ns	3
RCLK Clock High / Low Time	t2 / t3	9.0	11.2	13.4	ns	1
	t2 / t3	11.6	14.5	17.4	ns	2
	t2 / t3	7.7	9.6	11.5	ns	3
TCLK Clock High / Low Time	t2 / t3	7			ns	
TPOS / TNEG to TCLK Setup Time	t4	2			ns	
TPOS / TNEG Hold Time	t5	2			ns	
RCLK to RPOS / RNEG Valid, Signal Change on PRBS	t6	2		6	ns	4, 5

NOTES:

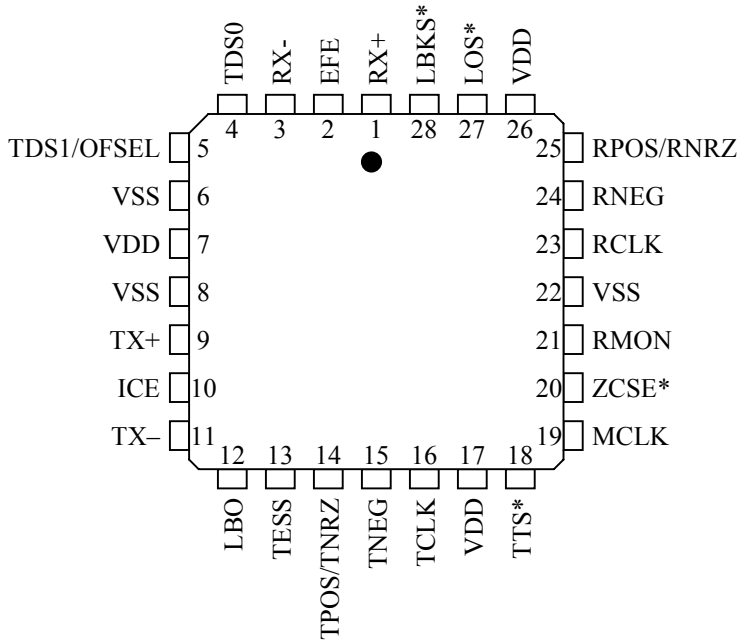
1. T3 Mode
2. E3 Mode
3. STS-1 Mode
4. In Normal Mode, TPOS and TNEG are sampled on the rising edge of TCLK and RPOS and RNEG are updated on the falling edge of RCLK
5. In Inverted Mode, TPOS and TNEG are sampled on the falling edge of TCLK and RPOS and RNEG are updated on the rising edge of RCLK

AC TIMING DIAGRAM Figure 3A

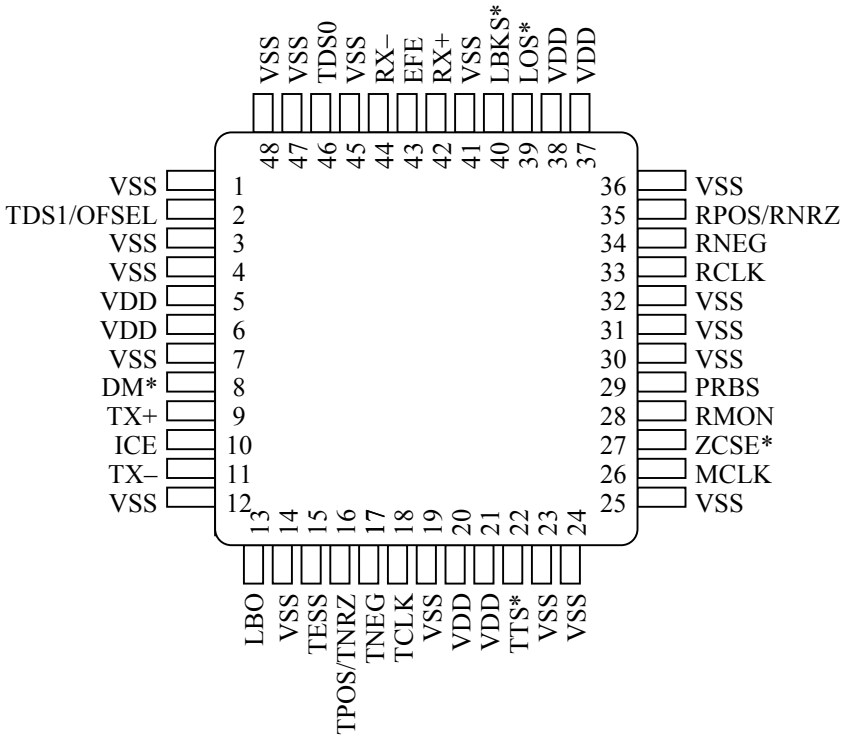


SECTION 4: PIN ASSIGNMENTS

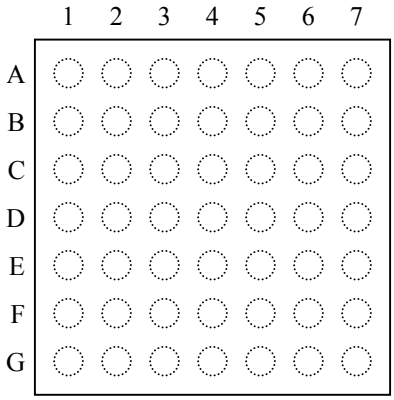
28-LEAD PLCC PIN ASSIGNMENT Figure 4A



48-LEAD TQFP PIN ASSIGNMENT Figure 4B



49-LEAD CSBGA PIN ASSIGNMENT Figure 4C

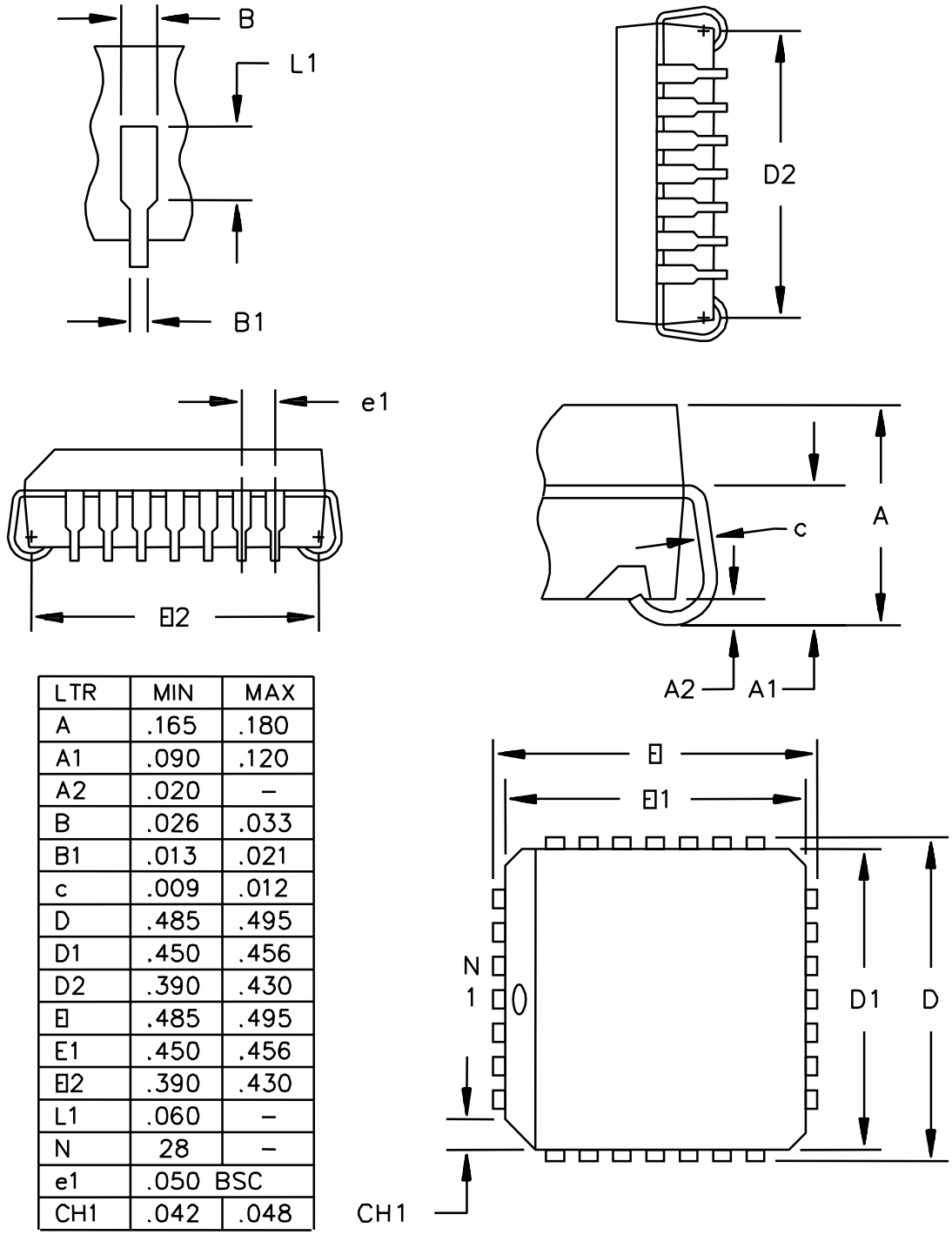


TOP VIEW

	1	2	3	4	5	6	7
A	NC	TDS0	RX-	RX+	LBKS*	NC	RPOS/ RNRZ
B	VSS	NC	EFE	LOS*	VDD	RNEG	NC
C	VSS	NC	TDS1	NC	NC	NC	RCLK
D	DM*	VDD	NC	NC	PRBS	NC	VSS
E	TX+	NC	NC	NC	NC	MCLK	RMON
F	TX-	ICE	LBO	TESS	TCLK	NC	ZCSE*
G	NC	NC	TPOS/ TNRZ	TNEG	VDD	TTS*	NC

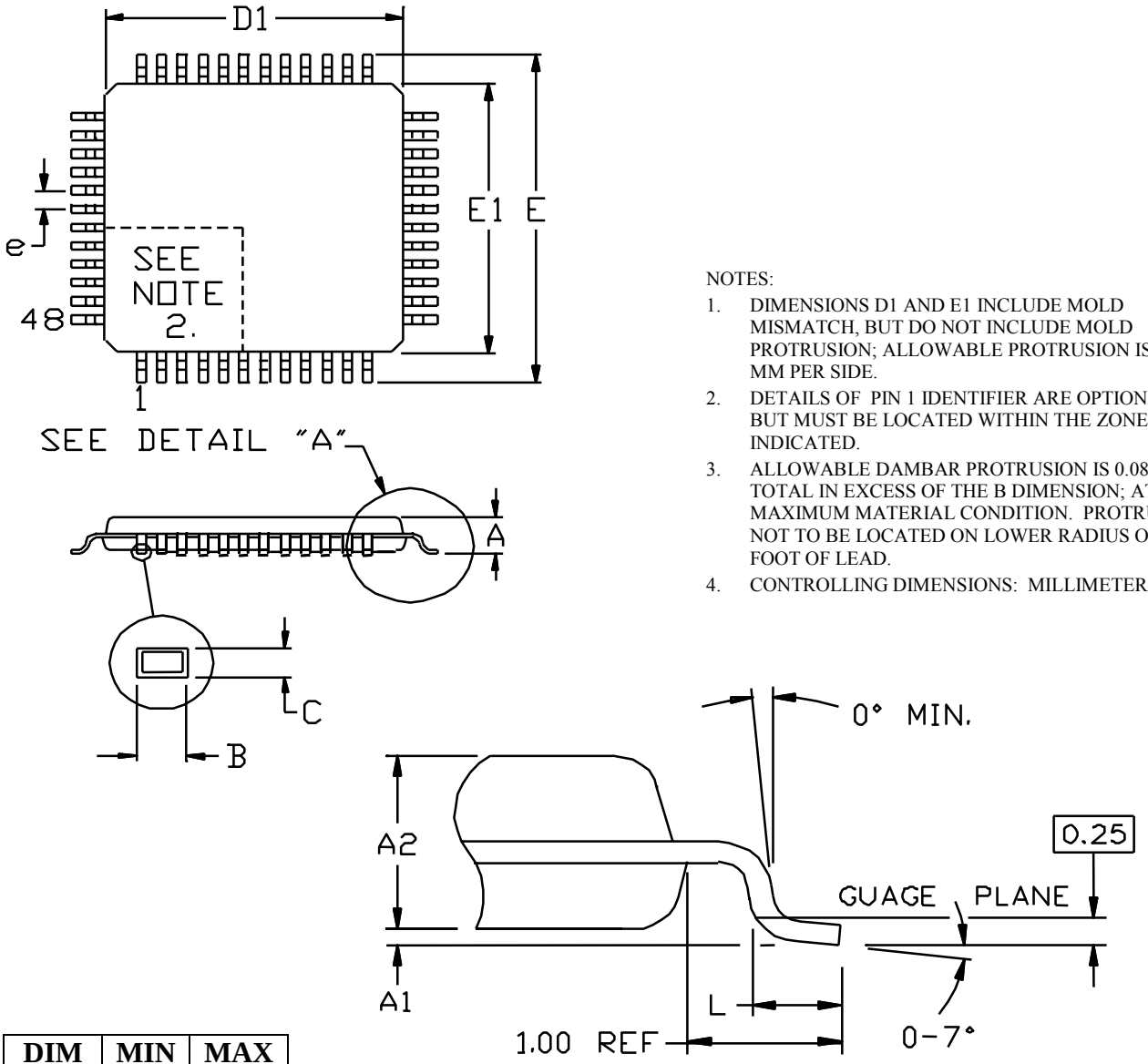
SECTION 5: MECHANICAL DIMENSIONS

28-LEAD PLCC PACKAGE Figure 5A



LTR	MIN	MAX
A	.165	.180
A1	.090	.120
A2	.020	–
B	.026	.033
B1	.013	.021
c	.009	.012
D	.485	.495
D1	.450	.456
D2	.390	.430
E	.485	.495
E1	.450	.456
E2	.390	.430
L1	.060	–
N	28	–
e1	.050 BSC	
CH1	.042	.048

48-LEAD TQFP PACKAGE Figure 5B

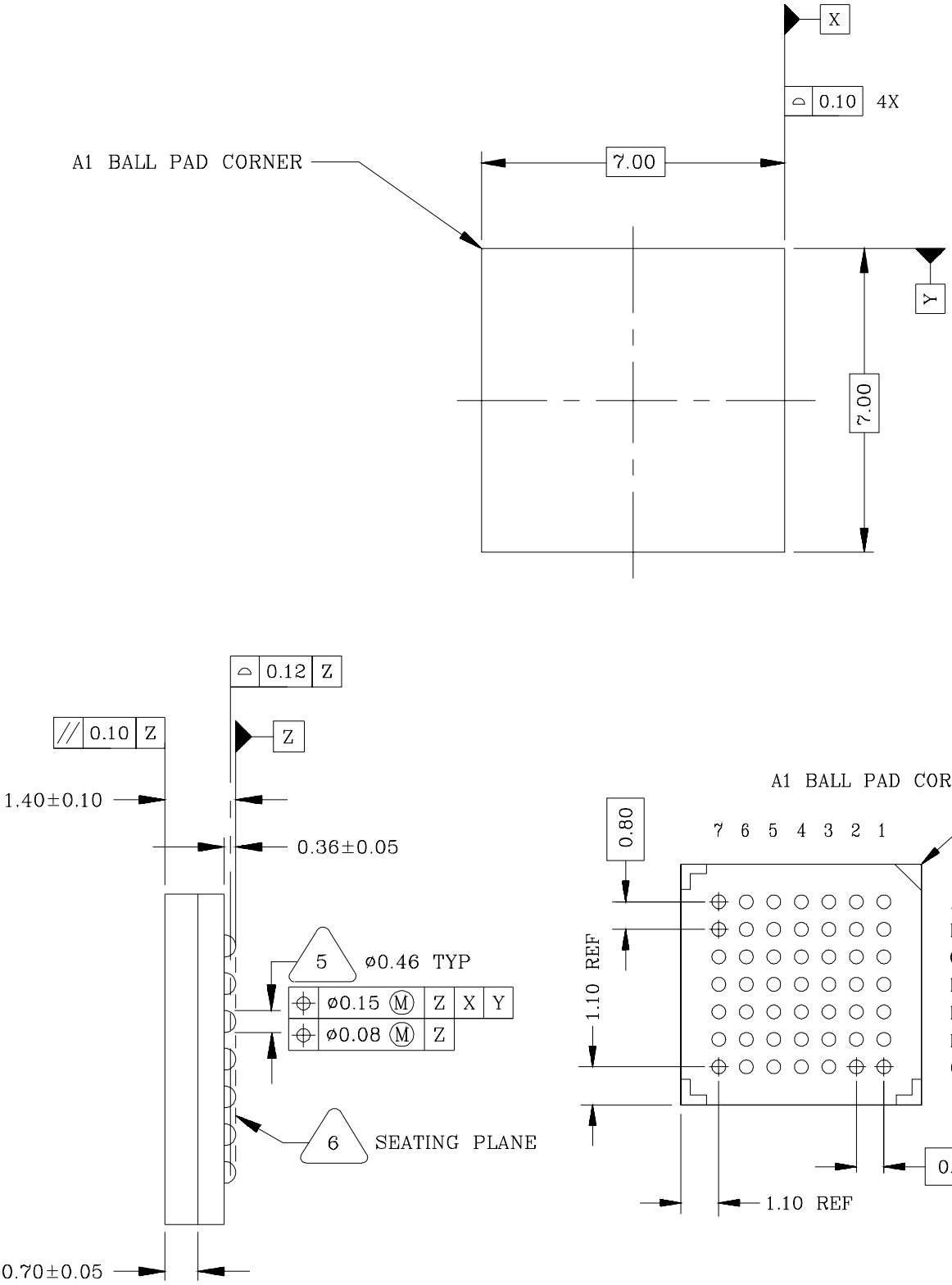


NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. CONTROLLING DIMENSIONS: MILLIMETERS.

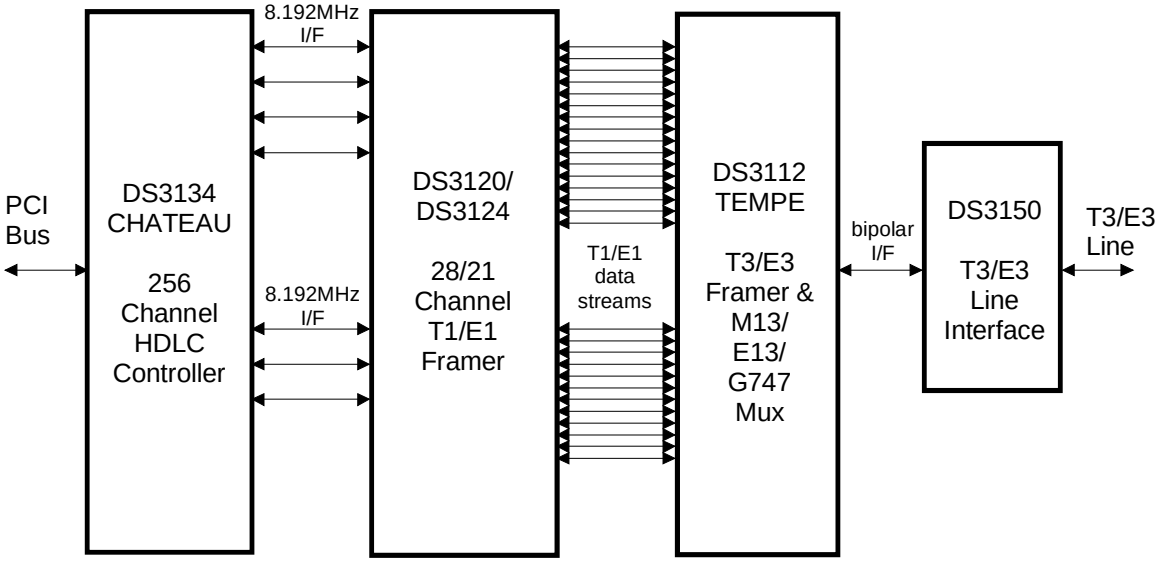
DIM	MIN	MAX
A	-	1.20
A1	0.05	0.15
A2	0.95	1.05
D	8.80	9.20
D1	7.00 BSC	
E	8.80	9.20
E1	7.00 BSC	
L	0.45	0.75
e	0.50 BSC	
B	0.17	0.27
C	0.09	0.20

49-LEAD CSBGA PACKAGE Figure 5C



SECTION 6: APPLICATIONS

CHANNELIZED T3/E3 APPLICATION Figure 6A



DUAL UNCHANNELIZED T3/E3 APPLICATION Figure 6B