



MAX3677 Evaluation Kit

General Description

The MAX3677 evaluation kit (EV kit) is an assembled demonstration board that provides convenient evaluation of the MAX3677 low-jitter, precision clock generator. The EV kit includes an on-board 25MHz crystal to allow for immediate testing.

The EV kit includes switches to allow easy selection of different modes of operation. The clock outputs use SMA connectors and are AC-coupled to simplify connection to test equipment.

Features

- ◆ AC-Coupled I/Os for Ease of Testing
- ◆ Fully Assembled and Tested
- ◆ +3.3V Power-Supply Operation
- ◆ On-Board 25MHz Crystal

Ordering Information

| PART | TYPE |
|---------------|--------|
| MAX3677EVKIT+ | EV Kit |

+Denotes lead(Pb)-free and RoHS compliant.

Component List

| DESIGNATION | QTY | DESCRIPTION |
|--|-----|--|
| C1 | 1 | 2.2 μ F \pm 10% ceramic capacitor (0805) |
| C2, C4, C5, C9, C11–C15, C20, C44, C54–C64, C66, C67 | 24 | 0.1 μ F \pm 10% ceramic capacitor (0402) |
| C3 | 1 | 33 μ F \pm 10% Tantalum capacitor (B case) |
| C6, C21 | 2 | 0.01 μ F \pm 5% ceramic capacitor (0402) |
| C7 | 1 | 10 μ F \pm 20% ceramic capacitor (0603) |
| C17 | 1 | 3pF \pm 5% ceramic capacitor (0402) |
| C45 | 1 | 27pF \pm 5% ceramic capacitor (0402) |
| C46 | 1 | 33pF \pm 5% ceramic capacitor (0402) |
| J4, J8, J10 | 3 | 2-pin header, 0.1in centers |
| J13 | 1 | SMA right-angle connector |
| J14 | 1 | SPDT switch |
| J15, J16, J35, J36, J44, J51, J52, J55, J56, J59–J62, J65, J66 | 15 | SMA connectors |

| DESIGNATION | QTY | DESCRIPTION |
|---|-----|--|
| L1 | 1 | 4.7 μ H inductor (DS1608) |
| R1, R89 | 2 | 49.9 Ω \pm 1% resistor (0402) |
| R2 | 1 | Do not install (0402) |
| R3 | 1 | 0 Ω \pm 5% resistor (0402) |
| R34 | 1 | 10.5 Ω \pm 1% resistor (0402) |
| R87, R90 | 2 | 806 Ω \pm 1% resistor (0402) |
| R88 | 1 | 33.2 Ω \pm 1% resistor (0402) |
| SW3 | 1 | SP3T switch |
| TP1, TP2, TP3, TP5, TP26, TP28, J2, J48 | 8 | Test points |
| U6 | 1 | +3.3V, low-jitter, precision clock generator (32 TQFN-EP*) MAX3677CTJ+ |
| Y1 | 1 | 25MHz crystal NDK America EXS00A-AT00429 |
| — | 3 | Shunts |
| — | 1 | MAX3677 EVKIT BOARD + REV A |

*EP = Exposed pad.

Component Suppliers

| SUPPLIER | PHONE | WEBSITE |
|-------------|--------------|----------------|
| NDK America | 815-544-7900 | www.ndk.com/en |

Note: Indicate that you are using the MAX3677 when contacting these component suppliers.

Evaluates: MAX3677

MAX3677 Evaluation Kit

Quick Start

For evaluation of the MAX3677, configure the EV kit as follows:

- 1) Determine which output is going to be evaluated and connect to the test equipment through SMA cables. Be sure not to leave any outputs unterminated, i.e., place 50Ω terminators on all unused outputs.
- 2) Set $\overline{\text{PLL_BP}}$ high so that the on-board crystal is used.
- 3) Place a shunt on J8 (VDD_DIFF) and J10 (VDD_SE) to connect the power supply for the differential and single ended outputs.
- 4) Connect a +3.3V power supply to J48 (VCC) and J2 (GND). Set the current limit to 200mA.

Adjustment and Control Descriptions (see Quick Start first)

| COMPONENT | NAME | FUNCTION |
|-----------|-----------------------------|---|
| J4 | INDUCTOR SHUNT | J4 shunts the power-supply inductor. Normal operation is J4 not shunted. |
| J8 | VDD_DIFF | Connects the power supply for the Q0, Q1, Q2, Q3, Q4, Q5, and Q6 clock outputs to the VCC supply. |
| J10 | VDD_SE | Connects the power supply for the Q7 clock output to the VCC supply. |
| J14 | OE | When set to HIGH, the Q4, Q5, and Q6 outputs are enabled. When set to LOW, the Q4, Q5, and Q6 outputs are disabled. |
| SW3 | $\overline{\text{PLL_BP}}$ | When set to HIGH, the PLL locks to the crystal interface (25MHz at X_IN and X_OUT). When set to OPEN, the PLL locks to the OSC_IN input (25MHz typical). When set LOW, the PLL is bypassed and the OSC_IN input is selected. When bypass mode is selected, the VCO/PLL is disabled to save power and eliminate intermodulation spurs. |

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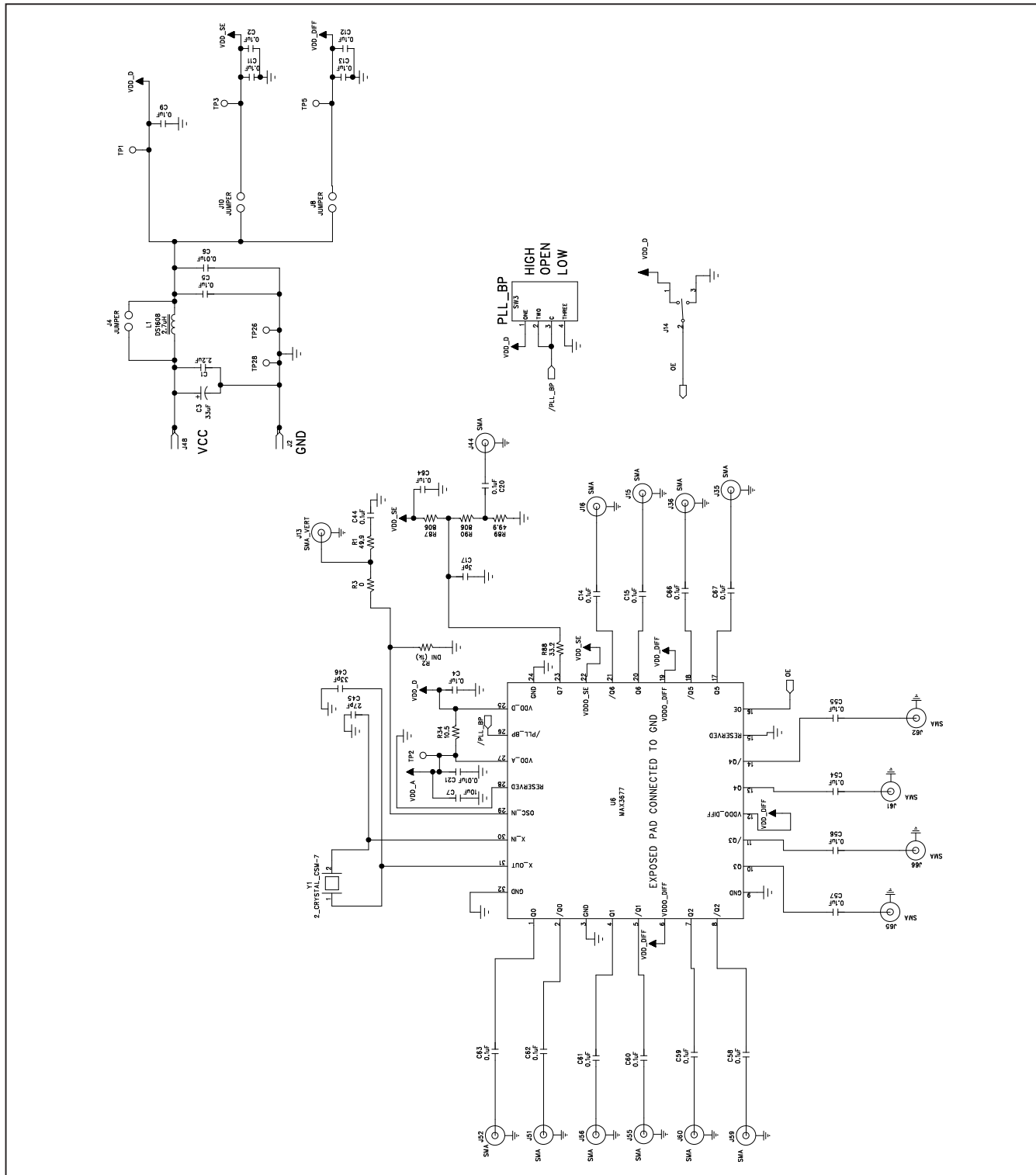


Figure 1. MAX3677 EV Kit Schematic

MAX3677 Evaluation Kit

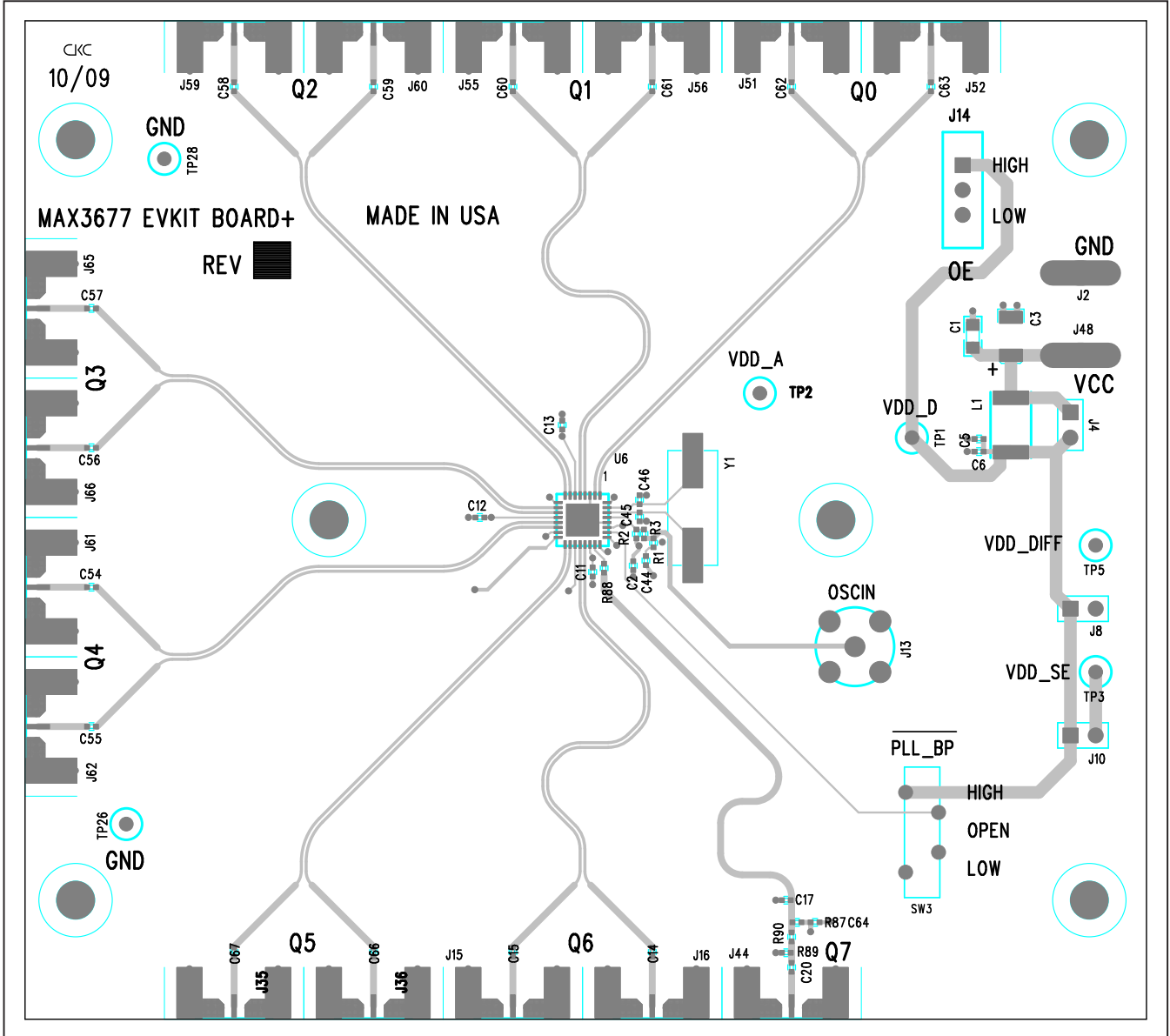


Figure 2. MAX3677 EV Kit Component Placement Guide—Component Side

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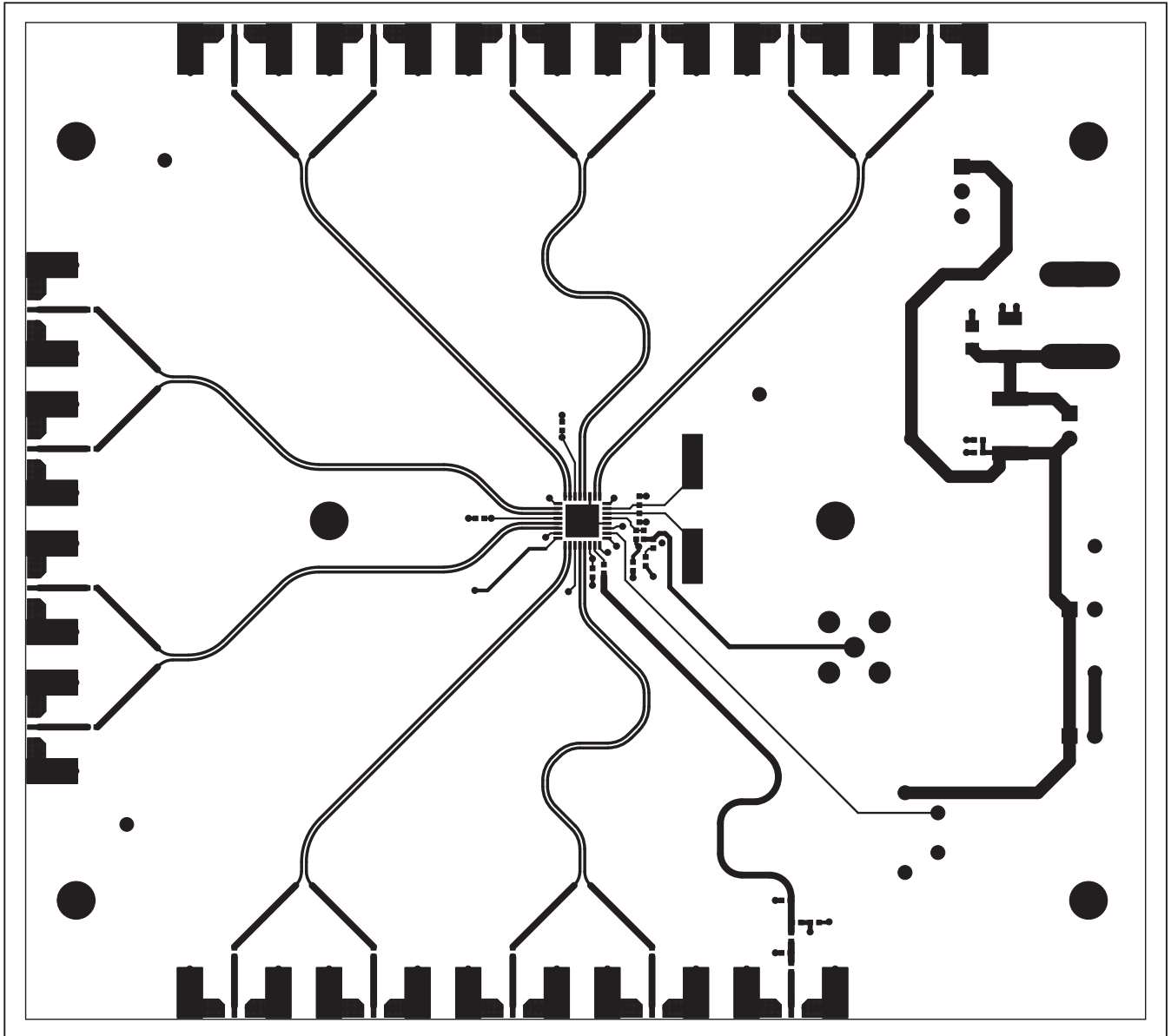


Figure 3. MAX3677 EV Kit PCB Layout—Component Side

MAX3677 Evaluation Kit

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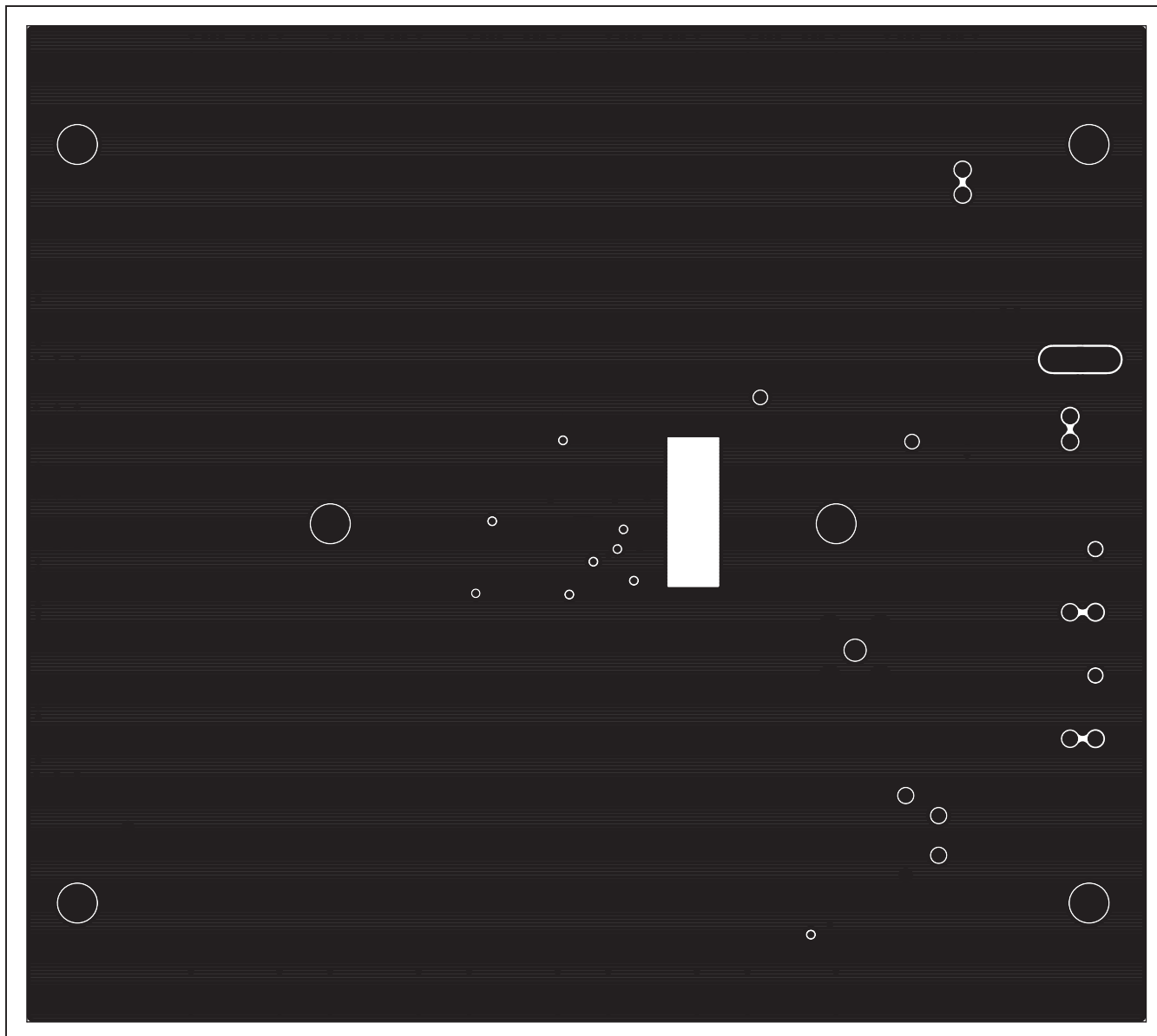


Figure 4. MAX3677 EV Kit PCB Layout—Ground Plane

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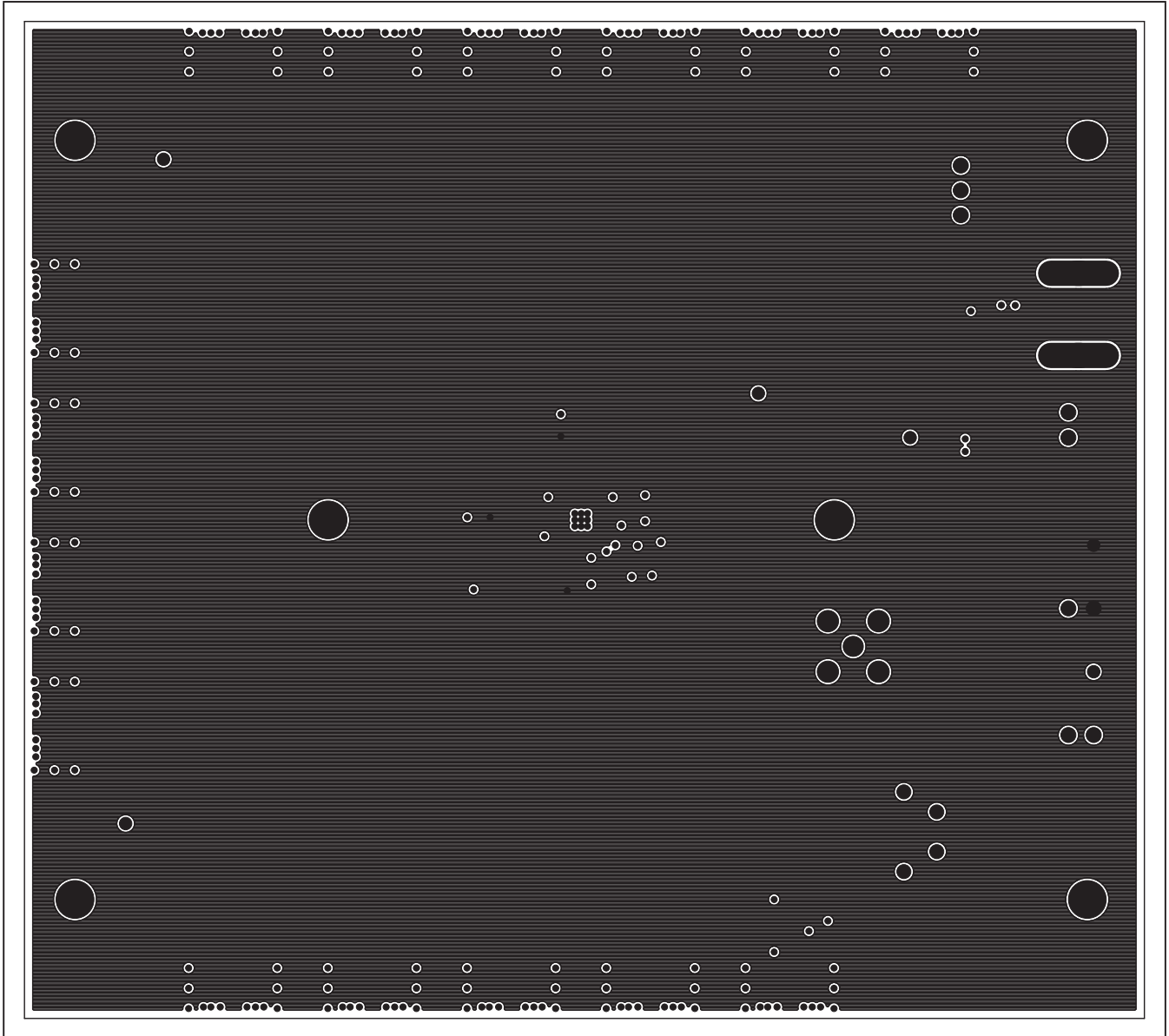


Figure 5. MAX3677 EV Kit PCB Layout—Power Plane

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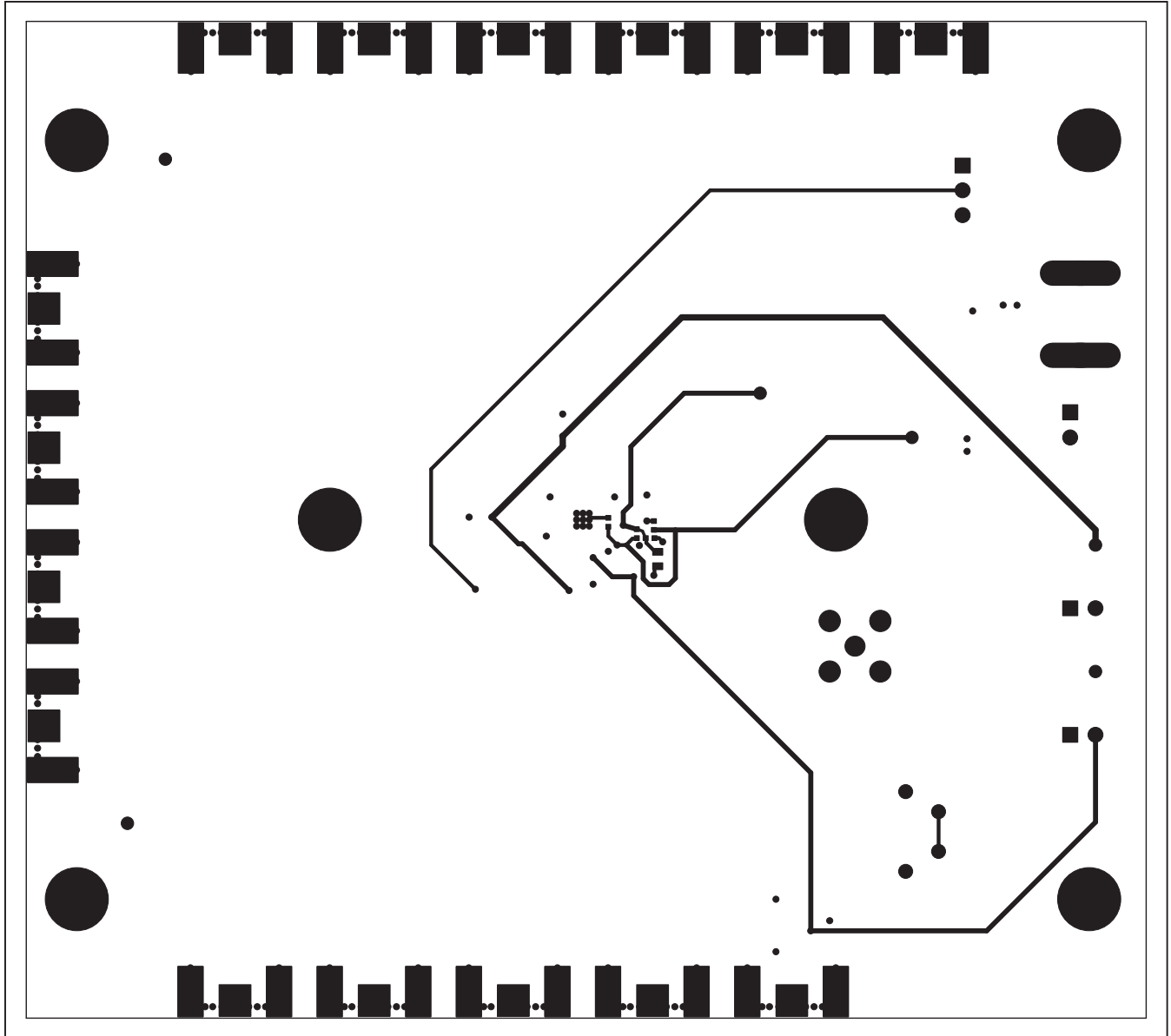


Figure 6. MAX3677 EV Kit PCB Layout—Solder Side



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