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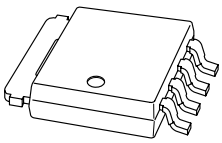


# PH4830L

## N-channel TrenchMOS logic level FET

**Rev. 01 — 6 September 2007** **Product data sheet**

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Logic level threshold
- Optimized for use in DC-to-DC converters
- 100 % $R_G$ tested
- Lead-free package
- Very low switching and conduction losses
- 100 % ruggedness tested

### 1.3 Applications

- DC-to-DC converters
- Voltage regulators
- Switched-mode power supplies
- PC Motherboards

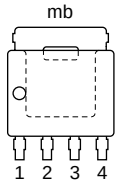
### 1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $R_{DSon} \leq 4.8$ mΩ
- $I_D \leq 84$ A
- $Q_{GD} = 5.4$ nC (typ)

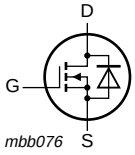
## 2. Pinning information

**Table 1. Pinning**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1, 2, 3 | source (S) | | |
| 4 | gate (G) | | |
| mb | mounting base; connected to drain (D) | | |




**SOT669 (LFPAK)**



## 3. Ordering information

**Table 2. Ordering information**

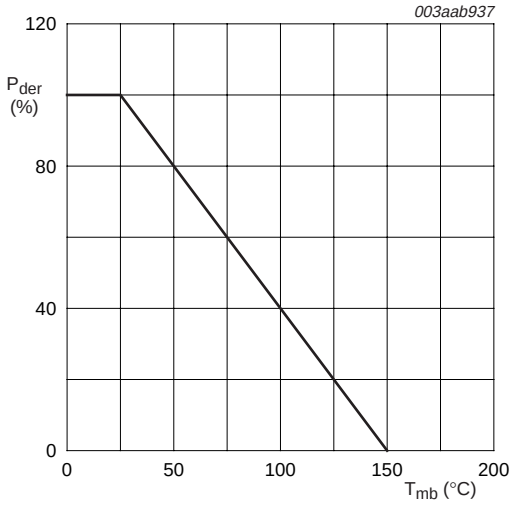
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PH4830L | LFPAK | plastic single-ended surface-mounted package (lfpak); 4 leads | SOT669 |

## 4. Limiting values

**Table 3. Limiting values**

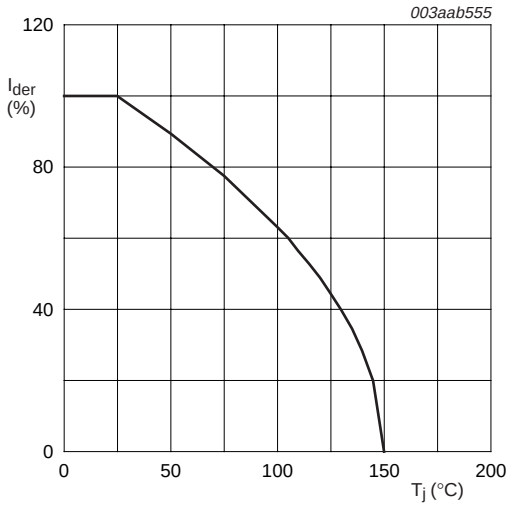
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 150 °C | - | 30 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C; $R_{GS}$ = 20 kΩ | - | 30 | V |
| $V_{GS}$ | gate-source voltage | | - | ±20 | V |
| $I_D$ | drain current | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see Figure 2 and 3 | - | 84 | A |
| | | $T_{mb}$ = 100 °C; $V_{GS}$ = 10 V; see Figure 2 | - | 63 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; see Figure 3 | - | 240 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; see Figure 1 | - | 62.5 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –55 | +150 | °C |
| **Source-drain diode** | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | - | 52 | A |
| $I_{SM}$ | peak source current | $T_{mb}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs | - | 208 | A |
| **Avalanche ruggedness** | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | unclamped inductive load; $I_D$ = 49 A; $t_p$ = 0.12 ms; $V_{DS}$ ≤ 25 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; starting at $T_j$ = 25 °C | - | 121 | mJ |



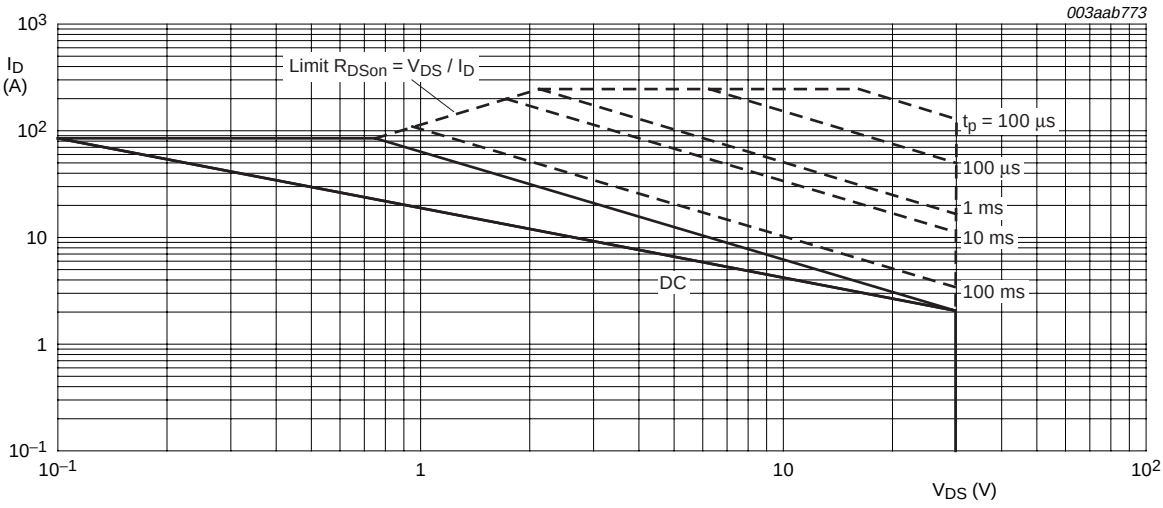

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature**




$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

**Fig 2. Normalized continuous drain current as a function of mounting base temperature**




$T_{mb}$ = 25 °C; $I_{DM}$ is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | - | 2 | K/W |

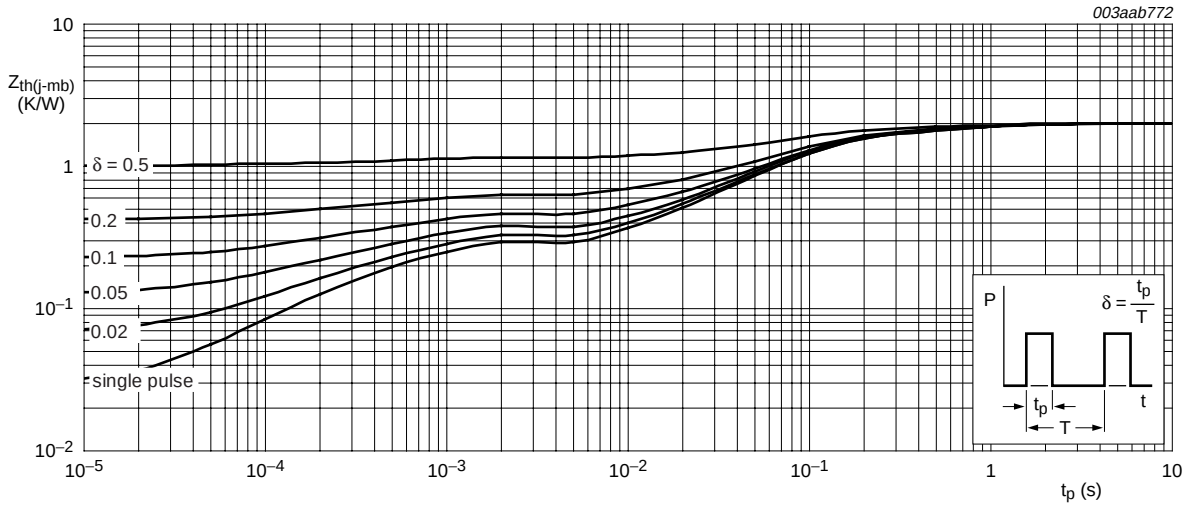


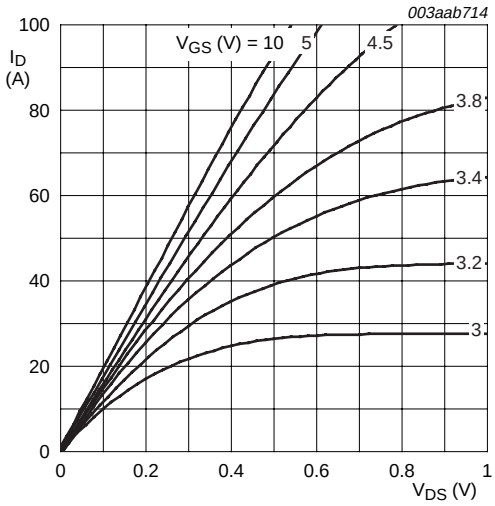

**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

**Table 5. Characteristics**

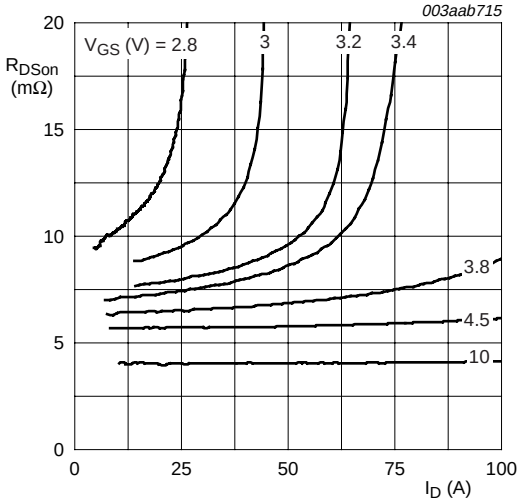
*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | 30 | - | - | V |
| | | $T_j$ = −55 °C | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; see Figure 9 and 10 | | | | |
| | | $T_j$ = 25 °C | 1.3 | 1.7 | 2.15 | V |
| | | $T_j$ = 150 °C | 0.8 | - | - | V |
| | | $T_j$ = −55 °C | - | - | 2.6 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | - | 1.0 | µA |
| | | $T_j$ = 150 °C | - | - | 100 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = ±20 V; $V_{DS}$ = 0 V | - | - | 100 | nA |
| $R_G$ | gate resistance | f = 1 MHz | - | 0.51 | - | Ω |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; see Figure 6 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 3.8 | 4.8 | mΩ |
| | | $T_j$ = 150 °C | - | 6.3 | 7.7 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; see Figure 6 and 8 | - | 5.6 | 7.0 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 12 V; $V_{GS}$ = 4.5 V; see Figure 11 and 12 | - | 22.9 | - | nC |
| $Q_{GS}$ | gate-source charge | | - | 9.0 | - | nC |
| $Q_{GS1}$ | pre-$V_{GS(th)}$ gate-source charge | | - | 5.5 | - | nC |
| $Q_{GS2}$ | post-$V_{GS(th)}$ gate-source charge | | - | 3.5 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 5.4 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | | - | 2.8 | - | V |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 12 V; f = 1 MHz; see Figure 14 | - | 2786 | - | pF |
| $C_{oss}$ | output capacitance | | - | 579 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 297 | - | pF |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 0 V; f = 1 MHz | - | 3300 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 12 V; $R_L$ = 0.5 Ω; $V_{GS}$ = 4.5 V; $R_G$ = 5.6 Ω | - | 28 | - | ns |
| $t_r$ | rise time | | - | 43 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 35 | - | ns |
| $t_f$ | fall time | | - | 19 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; see Figure 13 | - | 0.85 | - | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = −100 A/µs; $V_{GS}$ = 0 V; $V_R$ = 30 V | - | 47 | - | ns |
| $Q_r$ | recovered charge | | - | 17 | - | nC |



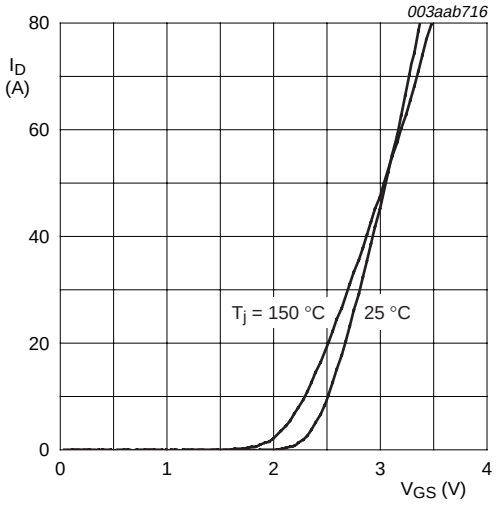

$T_j$ = 25 °C

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



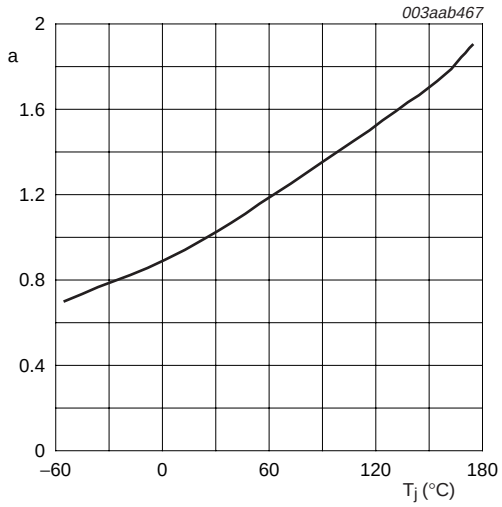

$T_j$ = 25 °C

**Fig 6. Drain-source on-state resistance as a function of drain current; typical values**



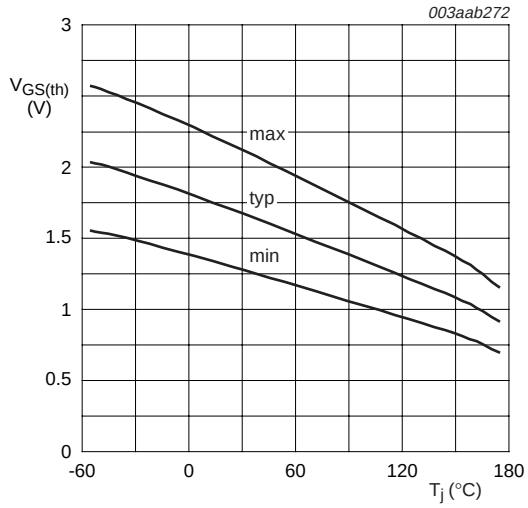

$T_j$ = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



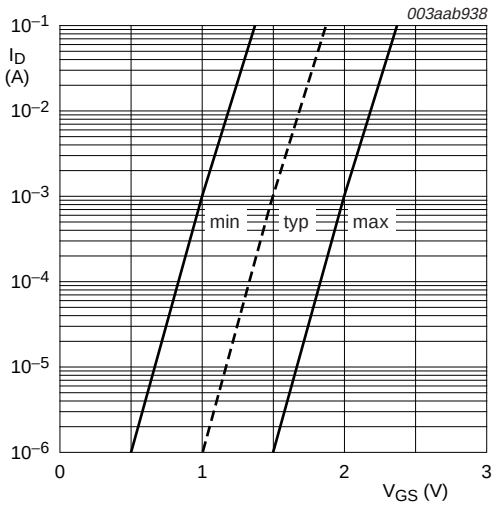

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**



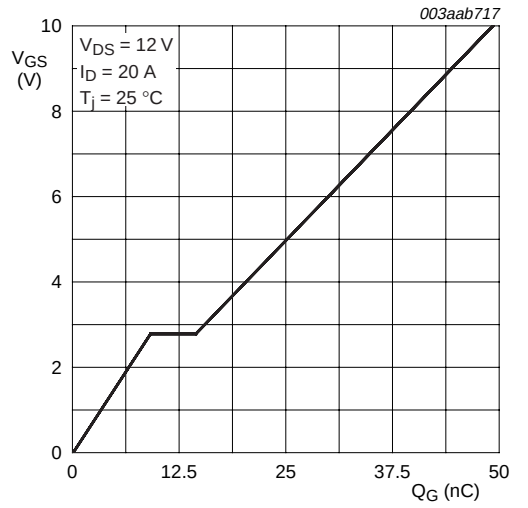

$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**




$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**




$I_D$ = 20 A; $V_{DS}$ = 12 V

**Fig 11. Gate-source voltage as a function of gate charge; typical values**

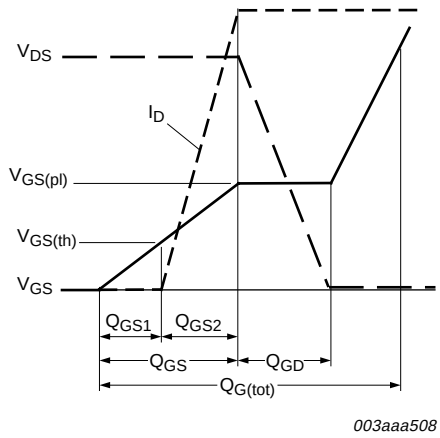
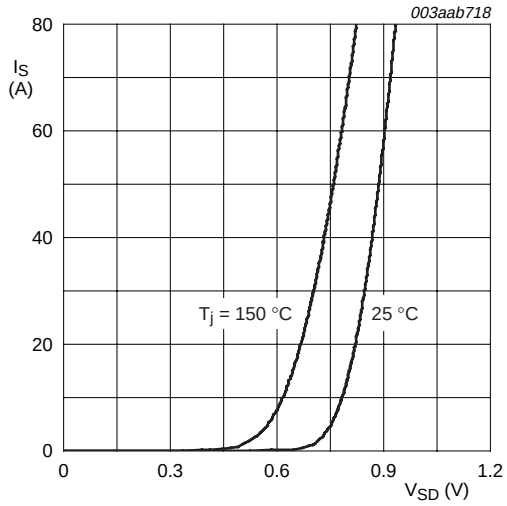
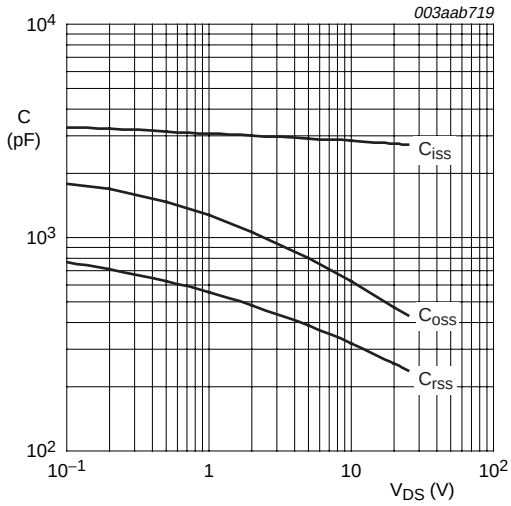



**Fig 12. Gate charge waveform definitions**




$T_j$ = 25 °C and 150 °C; $V_{GS}$ = 0 V

**Fig 13. Source current as a function of source-drain voltage; typical values**

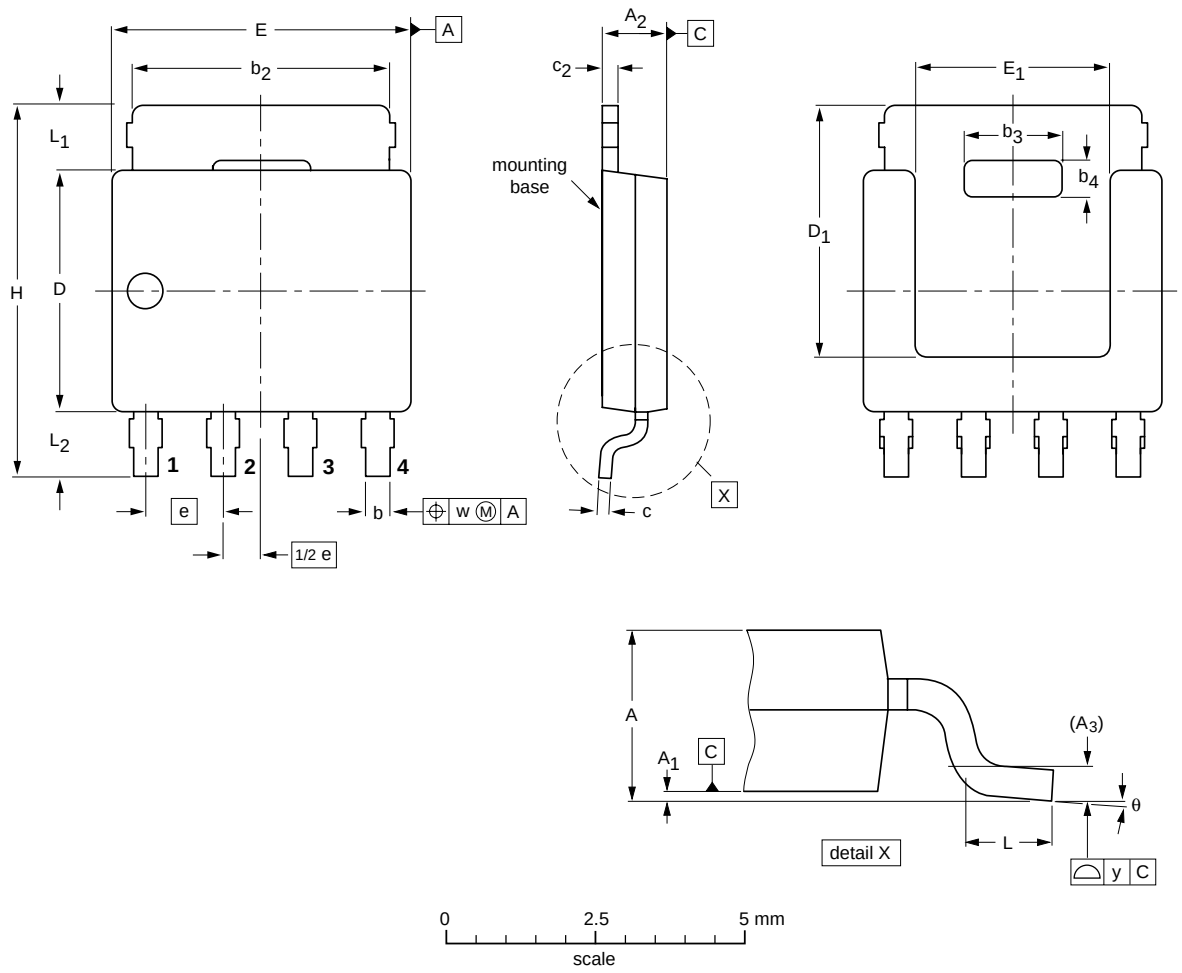



$V_{GS}$ = 0 V; f = 1 MHz

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

## 7. Package outline

**Plastic single-ended surface-mounted package (LFPAK); 4 leads** **SOT669**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | $b_3$ | $b_4$ | c | $c_2$ | $D^{(1)}$ | $D_1^{(1)}$ max | $E^{(1)}$ | $E_1^{(1)}$ | e | H | L | $L_1$ | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.20<br>1.01 | 0.15<br>0.00 | 1.10<br>0.95 | 0.25 | 0.50<br>0.35 | 4.41<br>3.62 | 2.2<br>2.0 | 0.9<br>0.7 | 0.25<br>0.19 | 0.30<br>0.24 | 4.10<br>3.80 | 4.20 | 5.0<br>4.8 | 3.3<br>3.1 | 1.27 | 6.2<br>5.8 | 0.85<br>0.40 | 1.3<br>0.8 | 1.3<br>0.8 | 0.25 | 0.1 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | ~~04-10-13~~<br>06-03-16 |

**Fig 15. Package outline SOT669 (LFPAK)**

## 8. Revision history

**Table 6. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PH4830L_1 | 20070906 | Product data sheet | - | - |

# 9. Legal information

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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contents


| | | |
|---|---|---|
| **1** | **Product profile** | **1** |
| 1.1 | General description | 1 |
| 1.2 | Features | 1 |
| 1.3 | Applications | 1 |
| 1.4 | Quick reference data | 1 |
| **2** | **Pinning information** | **1** |
| **3** | **Ordering information** | **2** |
| **4** | **Limiting values** | **2** |
| **5** | **Thermal characteristics** | **4** |
| **6** | **Characteristics** | **5** |
| **7** | **Package outline** | **9** |
| **8** | **Revision history** | **10** |
| **9** | **Legal information** | **11** |
| 9.1 | Data sheet status | 11 |
| 9.2 | Definitions | 11 |
| 9.3 | Disclaimers | 11 |
| 9.4 | Trademarks | 11 |
| **10** | **Contact information** | **11** |
| **11** | **Contents** | **12** |




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