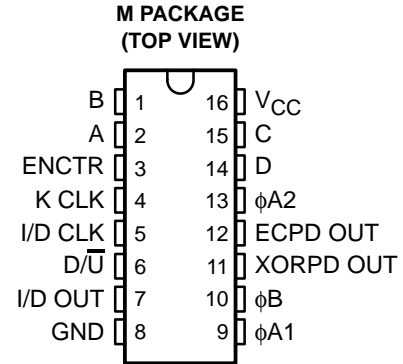- **Speed of Bipolar FCT, AS, and S, With Significantly Reduced Power Consumption**
- **Digital Design Avoids Analog Compensation Errors**
- **Easily Cascadable for Higher-Order Loops**
- **Useful Frequency Range**
  - **DC to 110 MHz Typical (K CLK)**
  - **DC to 70 MHz Typical (I/D CLK)**
- **Dynamically Variable Bandwidth**
- **Very Narrow Bandwidth Attainable**
- **Power-On Reset**
- **Output Capability**
  - **Standard: XORPD OUT, ECPD OUT**
  - **Bus Driver: I/D OUT**
- **SCR Latch-Up-Resistant CMOS Process and Circuit Design**
- **Balanced Propagation Delays**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**

M PACKAGE
(TOP VIEW)

B	1	16	V_{CC}
A	2	15	C
ENCTR	3	14	D
K CLK	4	13	ϕA2
I/D CLK	5	12	ECPD OUT
D/$\overline{U}$	6	11	XORPD OUT
I/D OUT	7	10	ϕB
GND	8	9	ϕA1

description/ordering information

The CD74ACT297 provides a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. This device contains all the necessary circuits, with the exception of the divide-by-N counter, to build first-order phase-locked loops as shown in Figure 1.

Both exclusive-OR phase detectors (XORPDs) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation or to cascade to higher-order phase-locked loops.

The length of the up/down K counter is digitally programmable according to the K-counter function table. With A, B, C, and D all low, the K counter is disabled. With A high and B, C, and D low, the K counter is only three stages long, which widens the bandwidth, or capture range, and shortens the lock time of the loop. When A, B, C, and D are programmed high, the K counter becomes 17 stages long, which narrows the bandwidth, or capture range, and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A-through-D inputs can maximize the overall performance of the digital phase-locked loop.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	SOIC – M	Tube	CD74ACT297M	ACT297M
		Tape and reel	CD74ACT297M96	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering information (continued)

This device performs the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked loop (DPLL) is not affected by V_{CC} and temperature variations, but depends solely on accuracies of the K clock (K CLK), increment/decrement clock (I/D CLK), and loop propagation delays. The I/D clock frequency and the divide-by-N modulos determine the center frequency of the DPLL. The center frequency is defined by the relationship $f_C = $ I/D clock/2N (Hz).
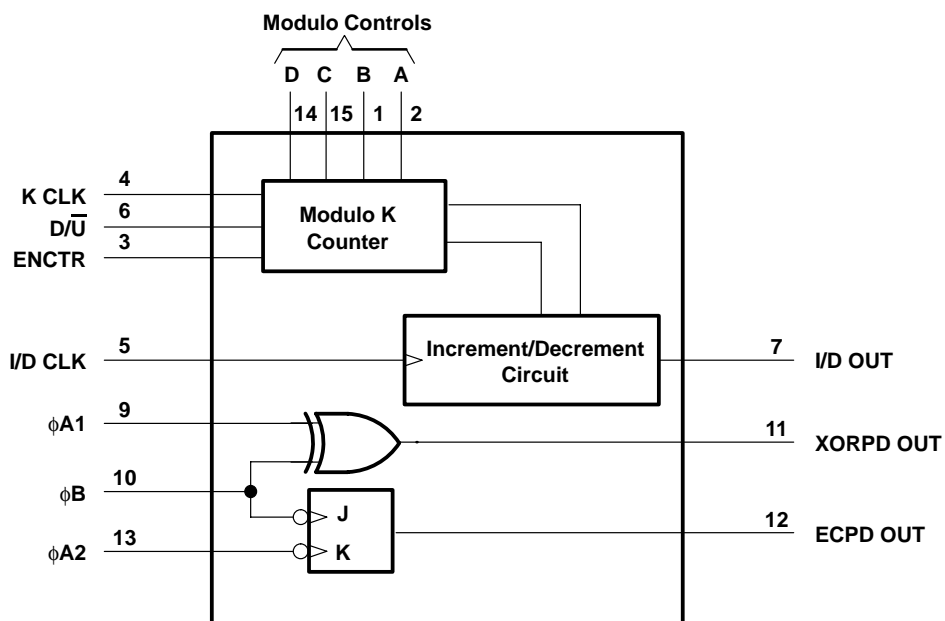

Figure 1. Simplified Block Diagram

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Function Tables

K COUNTER
(digital control)

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2^3
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	21^3
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

EXCLUSIVE-OR PHASE DETECTOR

ϕA1	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

EDGE-CONTROLLED PHASE DETECTOR

ϕA2	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No change
↑	H or L	No change

H = steady-state high level
L = steady-state low level
↓ = transition from high to low
↑ = transition from low to high

TEXAS INSTRUMENTS

CD74ACT297
DIGITAL PHASE-LOCKED LOOP

functional block diagram
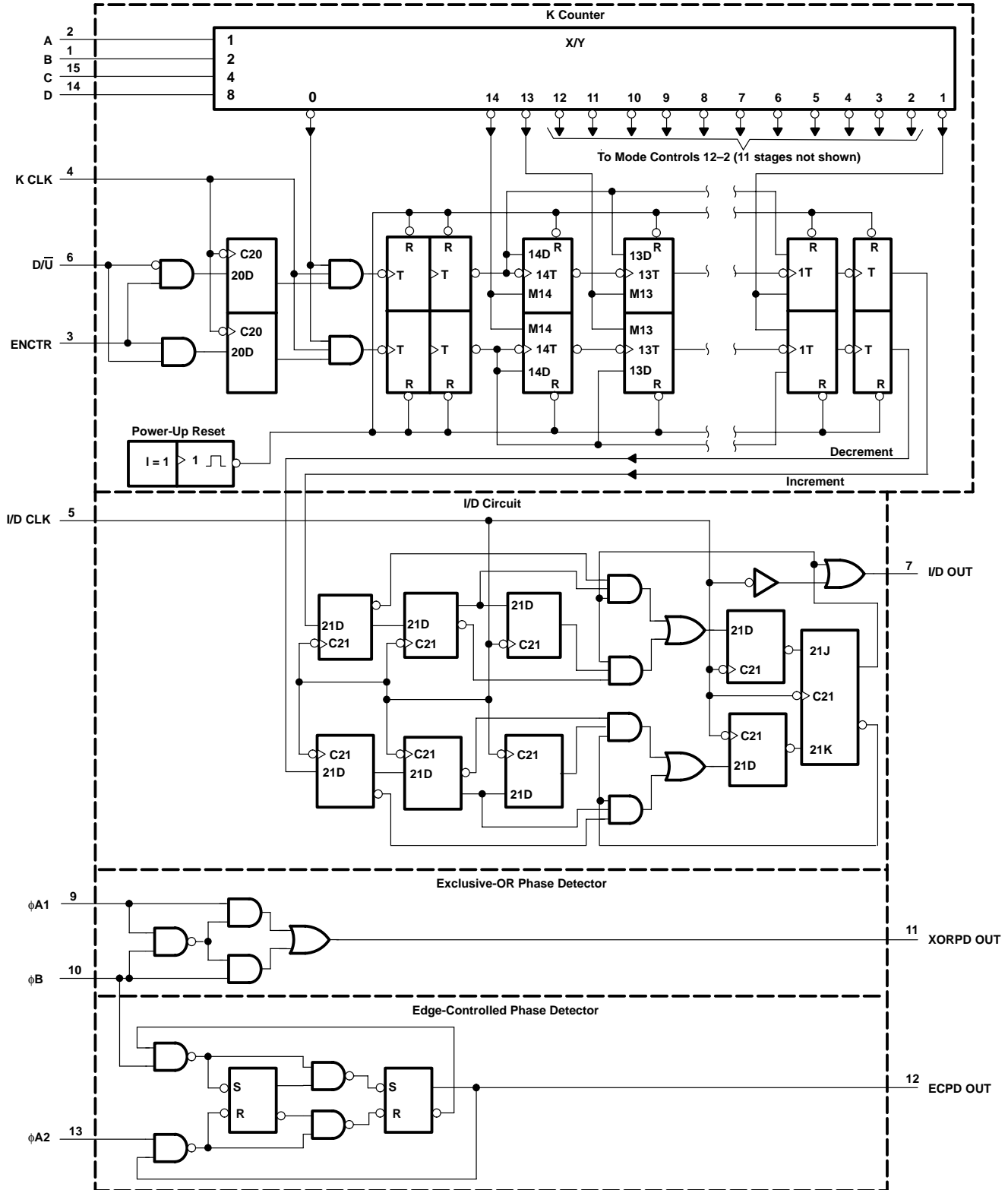
detailed description

The phase detector generates an error-signal waveform that, at zero phase error, is a 50% duty-cycle square wave. At the limits of linear operation, the phase-detector output is either high or low all of the time, depending on the direction of the phase error ($\phi_{in} - \phi_{out}$). Within these limits, the phase-detector output varies linearly with the input phase error according to the gain k_d, which is expressed in terms of phase-detector output per cycle of phase error. The phase-detector output can be varied between ± 1 according to the relation:

$$\text{Phase-detector output} = \frac{\%\ \text{high} - \%\ \text{low}}{100} \tag{1}$$

The output of the phase detector is $k_d \phi_e$, where the phase error $\phi_e = \phi_{in} - \phi_{out}$.

XORPD and ECPD are commonly used digital types. The ECPD is more complex than the XORPD, but can be described generally as a circuit that changes states on one of the transitions of its inputs. For an XORPD, $k_d = 4$, because its output remains high (PD output = 1) for a phase error of one-fourth cycle. Similarly, for the ECPD, $k_d = 2$, because its output remains high for a phase error of one-half cycle. The type of phase detector determines the zero-phase-error point, i.e., the phase separation of the phase-detector inputs for ϕ_e is defined to be zero. For the basic DPLL system of Figure 2, $\phi_e = 0$ when the phase-detector output is a square wave. The XORPD inputs are one-fourth cycle out of phase for zero phase error. For the ECPD, $\phi_e = 0$ when the inputs are one-half cycle out of phase.
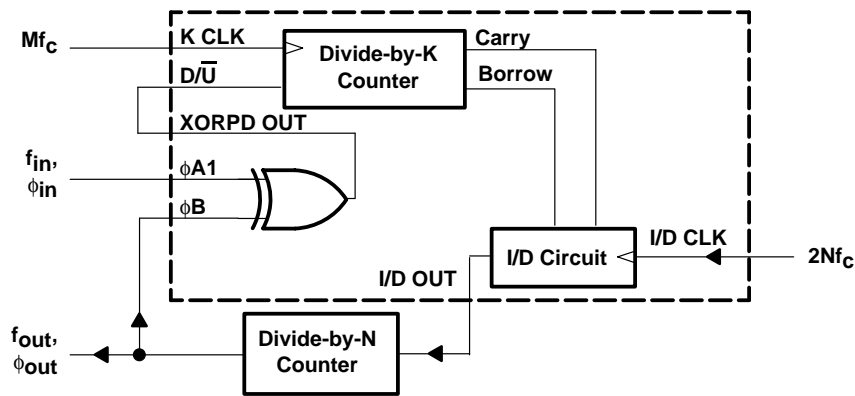

Figure 2. DPLL Using Exclusive-OR Phase Detection

The phase-detector output controls the up/down input to the K counter. The counter is clocked by input frequency Mf_C, which is a multiple M of the loop center frequency f_C. When the K counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K counter is considered as a frequency divider with the ratio Mf_C/K, the output of the K counter equals the input frequency multiplied by the division ratio. Thus, the output from the K counter is $k_d \phi_e Mf_C/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit, which, in the absence of any carry or borrow pulse, has an output that is one-half of the input clock (I/D CLK). The input clock is just a multiple (2N) of the loop center frequency. In response to a carry or borrow pulse, the I/D circuit either adds or deletes a pulse at I/D OUT. Thus, the output of the I/D circuit is $Nf_C + (k_d \phi_e Mf_C)/2K$.

The output of the N counter (or the output of the phase-locked loop) is:

$$f_O = f_C + (k_d \phi_e Mf_C)/2KN \tag{2}$$

When this result is compared to the equation for a first-order analog phase-locked loop, the digital equivalent of the gain of the VCO is $Mf_C/2KN$, or f_C/K for M = 2N.

TEXAS INSTRUMENTS

detailed description (continued)

Thus, the simple first-order phase-locked loop with an adjustable K counter is the equivalent of an analog phase-locked loop with a programmable VCO gain.
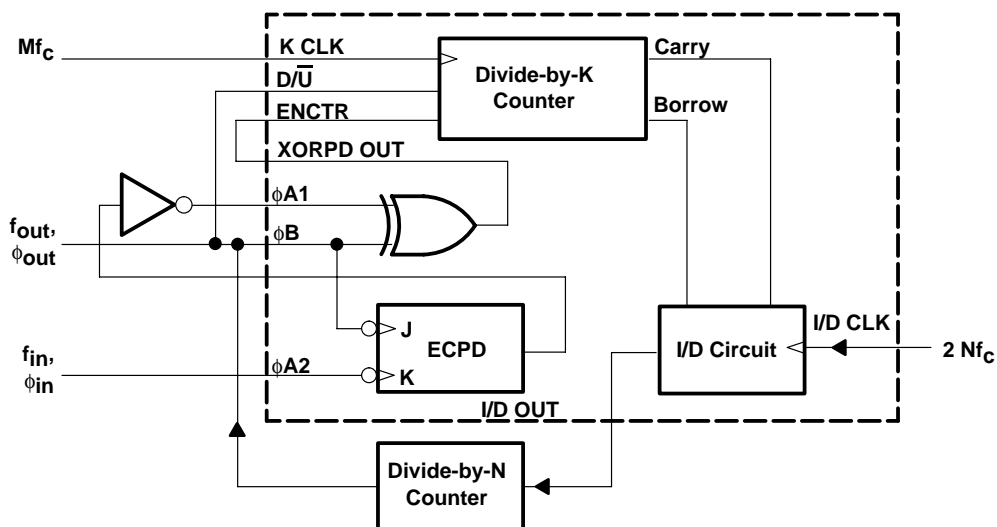

Figure 3. DPLL Using Both Phase Detectors in a Ripple-Cancellation Scheme

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 6 V
DC input diode current, I_{IK} ($V_I < −0.5$ V or $V_I > V_{CC} + 0.5$ V) .... ±20 mA
DC input diode current, I_{OK} ($V_O < −0.5$ V or $V_O > V_{CC} + 0.5$ V) .... ±50 mA
DC output source or sink current per output pin, I_O ($V_O > −0.5$ V or $V_O < V_{CC} + 0.5$ V) .... ±50 mA
Continuous current through V_{CC} or GND (see Note 1) .... ±100 mA
Package thermal impedance, θ_{JA} (see Note 2) .... 73°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. For up to four outputs per device, add ±25 mA for each additional output.
         2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
$\Delta t/\Delta v$	Input rise and fall slew rate		10	ns
T_A	Operating free-air temperature range	−55	125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V$_{CC}$	T$_A$ = 25°C		MIN MAX	UNIT
				MIN	MAX		
V$_{OH}$	V$_I$ = V$_{IH}$ or V$_{IL}$	I$_O$ = −50 μA	4.5 V	4.4		4.4	V
		I$_O$ = −24 mA	4.5 V	3.4		3.1	
		I$_O$ = −75 mA	5.5 V			3.3	
V$_{OL}$	V$_I$ = V$_{IH}$ or V$_{IL}$	I$_O$ = 50 μA	4.5 V		0.1	0.1	V
		I$_O$ = 24 mA	4.5 V		0.9	1.1	
		I$_O$ = 75 mA†	5.5 V			2.9	
I$_I$	V$_I$ = V$_{CC}$ or GND		5.5 V		±0.1	±1	μA
I$_{CC}$ (MSI)	V$_I$ = V$_{CC}$ or GND		5.5 V		8	80	μA
I$_{CC}$ (SSI/FF)	V$_I$ = V$_{CC}$ or GND		5.5 V		4	40	μA
ΔI$_{CC}$	V$_I$ = V$_{CC}$ −2.1 V		4.5 V to 5.5 V		2.4	2.8	mA

† Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C.

ACT INPUT LOAD

INPUT	UNIT LOAD†
ENCTR, D/$\overline{U}$	0.1
A, B, C, D, K CLK, φA2	0.2
I/D CLK, φA1, φB	0.5

† Unit Load is ΔI$_{CC}$ limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

timing requirements over recommended supply-voltage range and recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			T$_A$ = 25°C		MIN MAX	UNIT
			MIN	MAX		
f$_{clock}$	Clock frequency	K CLK		55	45	MHz
		I/D CLK		40	35	
t$_w$	Pulse duration	K CLK	6		8	ns
		I/D CLK	7		9	
t$_{su}$	Setup time before K CLK↑	D/$\overline{U}$	13		17	ns
		ENCTR	12		16	
t$_h$	Hold time after K CLK↑	D/$\overline{U}$	3		7	ns
		ENCTR	2		6	

TEXAS INSTRUMENTS

Carry Pulse
(internal signal)

Borrow Pulse
(internal signal)

I/D CLK

I/D OUT

Figure 4. I/D OUT in Lock Condition

φB

φA2

ECPD OUT
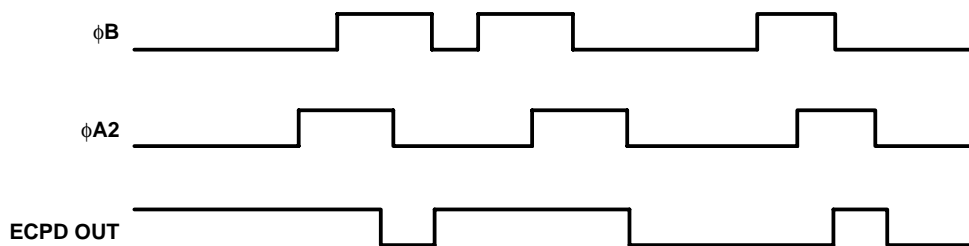
Figure 5. Edge-Controlled Phase-Comparator Waveforms

φB

φA1
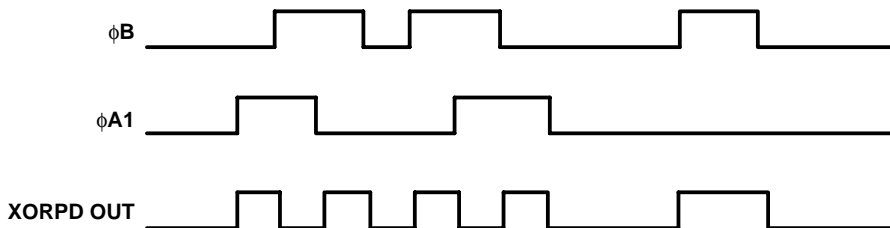
XORPD OUT

Figure 6. Exclusive-OR Phase-Detector Waveforms

1/F max

t_W

I/D CLK   1.5 V   1.5 V   3 V   0 V

t_{PHL} t_{PHL}

90%   ≈V_{CC}

I/D OUT   50% V_{CC} 50% V_{CC}

10% V_{OL}

t_{TLH} t_{THL}
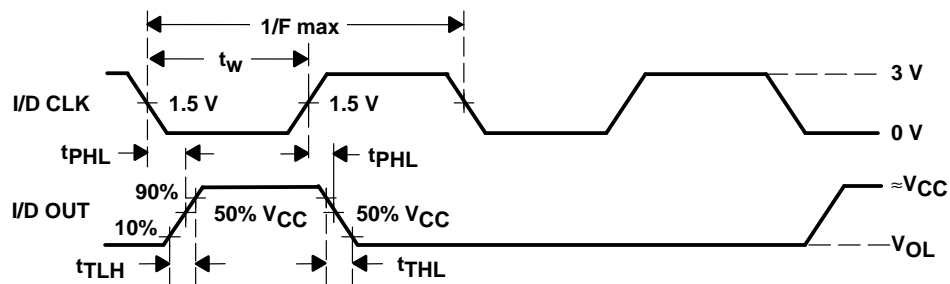
**Figure 7. Clock (ID CLK) to Output (ID OUT) Propagation Delays,
Clock Pulse Duration, and Maximum Clock-Pulse Frequency**

**TEXAS
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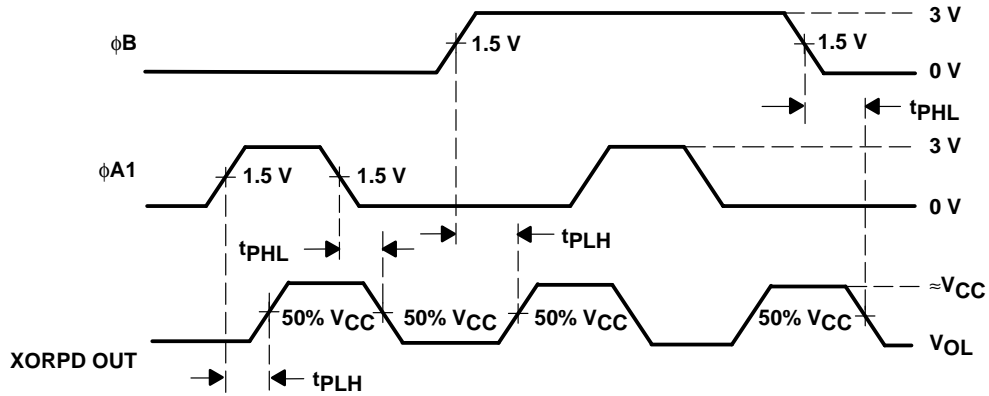
Figure 8. Phase Input (φB, φA2) to Output (XORPD OUT) Propagation Delays
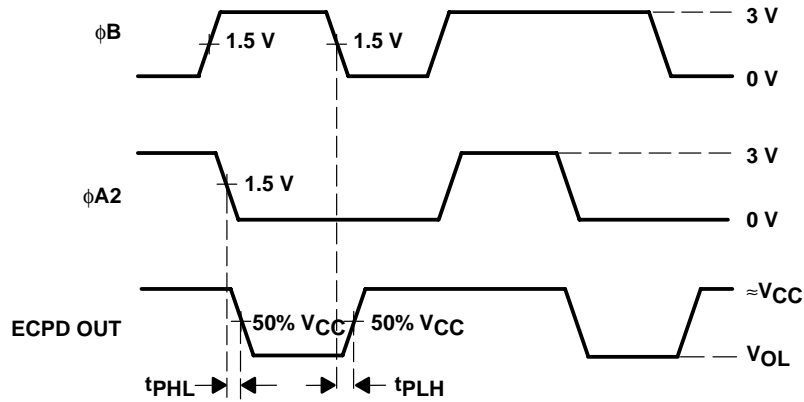
Figure 9. Phase Input (φB, φA2) to Output (ECPD OUT) Propagation Delays
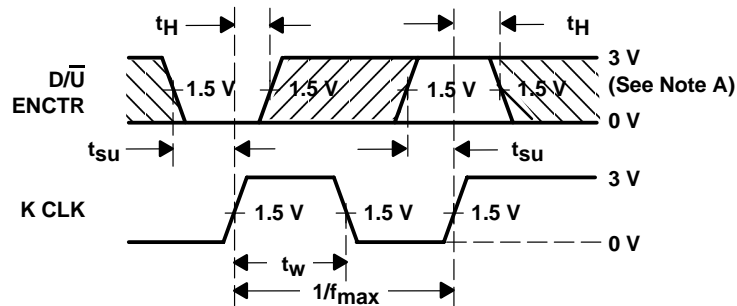
NOTE A: Shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 10. Clock (K CLK) Pulse Duration and Maximum Clock-Pulse Frequency,
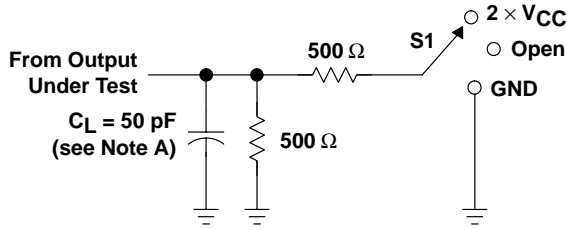**and Inputs (D/U, ENCTR) to Clock (K CLK) Setup and Hold Times**

SCHS297D – AUGUST 1998 – REVISED JUNE 2002

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	K CLK	I/D OUT	55			45		MHz
	I/D CLK		40			35		
t_{PLH}	I/D CLK	I/D OUT			19		24	ns
t_{PHL}					19		24	
t_{PHL}	φA2	ECPD OUT			24		30	ns
t_{PLH}	φA1	XORPD OUT			17		22	ns
t_{PHL}					17		22	
t_{PLH}	φB	XORPD OUT			17		22	ns
t_{PHL}					17		22	
t_{PLH}	φB	ECPD OUT			24		30	ns

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

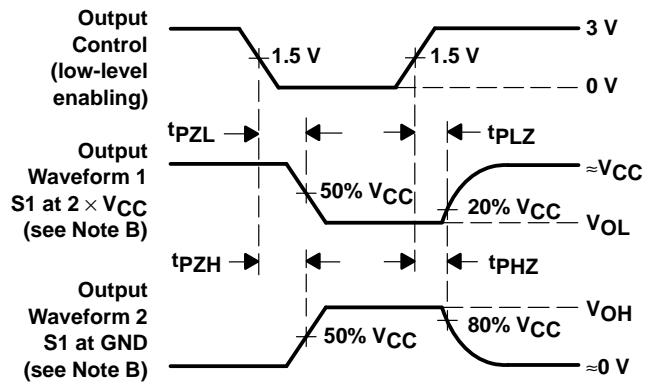| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND
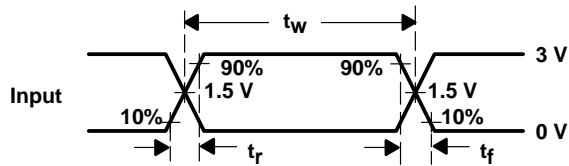
VOLTAGE WAVEFORMS
INPUT RISE AND FALL TIMES AND PULSE DURATION
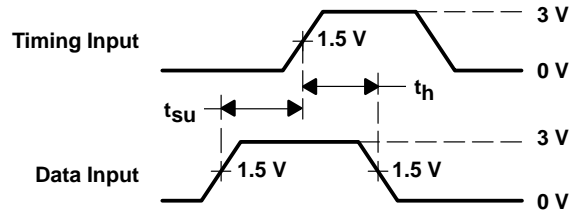
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
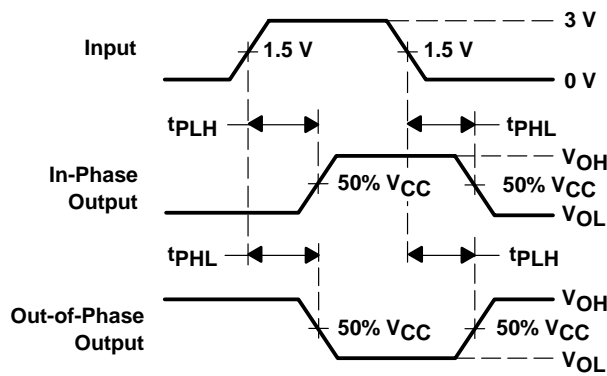
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
       B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
          Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
       C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
       D. The outputs are measured one at a time with one input transition per measurement.

Figure 11. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74ACT297M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT297M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74ACT297M	D	SOIC	16	40	507	8	3940	4.32

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
△C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
       △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
       △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

←14x1,27

16x0,55

←14x1,27

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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