TEXAS INSTRUMENTS

TPS7H2201-SP

SLVSDO0B – SEPTEMBER 2018 – REVISED MAY 2019

TPS7H2201-SP Radiation Hardened 1.5-V to 7-V, 6-A Load Switch

1 Features

- Radiation performance:
  - Radiation hardness assurance (RHA) up to TID 100 krad(Si)
  - Single event latchup (SEL), single event burnout (SEB), and single event gate rupture (SEGR) immune to LET = 75 MeV-cm^2/mg
  - SEFI/SET characterized to LET = 75 MeV-cm^2/mg
- Integrated single channel load switch
- Input voltage range: 1.5 V to 7 V
- Low on-resistance (R_{ON}) of 35-mΩ maximum at 25°C and VIN = 5 V
- 6-A maximum continuous switch current
- Low control input threshold enables use of 1.2-, 1.8-, 2.5-, and 3.3-V logic
- Configurable rise time (soft start)
- Reverse current protection
- Programmable and internal current limiting (fast-trip)
- Programmable fault timer (current limit and retry modes)
- Thermal shutdown
- Ceramic package with thermal pad

2 Applications

- Space satellite power management and distribution
- Radiation hardened and tolerant power tree applications
- Available in military (–55°C to 125°C) temperature range

3 Description

The TPS7H2201-SP is a single channel load switch that provides configurable rise time to minimize inrush current and reverse current protection. The device contains a P-channel MOSFET that can operate over an input voltage range of 1.5 V to 7 V and can support a maximum continuous current of 6 A. The switch is controlled by an on and off input (EN), which is capable of interfacing directly with low-voltage control signals.

The TPS7H2201-SP is available in a ceramic package with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –55°C to 125°C.

Device Information[1]

PART NUMBER	GRADE	PACKAGE
5962R1722001VXC	Flight Grade RHA 100 krad(Si)	16-Pin CDFP 11.00 × 9.60 mm Weight: 1.56 g[3]
5962-1722001VXC	Flight Grade QMLV	
TPS7H2201HKR/EM	Engineering Samples[2]	
TPS7H2201EVM-CVAL	Ceramic Evaluation Board	EVM

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

(3) Weight is accurate to ±10%.

Simplified Schematic

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4 Revision History

Changes from Revision A (January 2019) to Revision B   **Page**

Changes from Original (September 2018) to Revision A   **Page**

5 Pin Configuration and Functions

HKR Package
16-Pin CFP With Thermal Pad
Top View

VIN	1	16 VOUT
VIN	2	15 VOUT
VIN	3	14 VOUT
VIN	4	13 VOUT
CS	5	12 SS
EN	6	11 ILTIMER
OVP	7	10 IL
GND	8	9 RTIMER

Thermal Pad

Not to scale
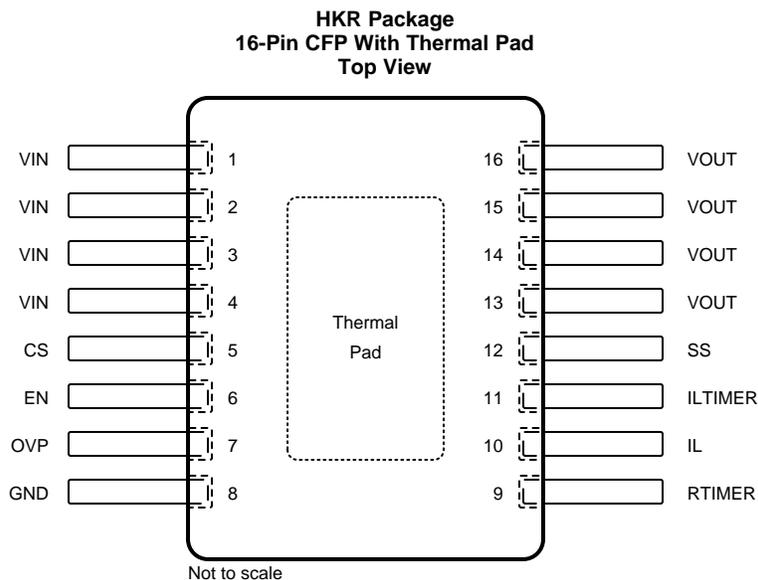
Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip.
2			
3			
4			
5	CS	O	Current sense pin proportional to output current. Connect a resistor to GND.
6	EN	I	Active high switch control input. Do not leave floating.
7	OVP	I	Overvoltage protection. Programmable using an external resistor divider. If no OVP is desired, this pin should be connected to GND.
8	GND	—	Device ground.[1]
9	RTIMER	I/O	Capacitor programmed fault timer control during disabled and retry mode. Connecting this pin to GND holds the switch disabled until the EN pin is cycled. Do not float this pin or connect it to VIN.
10	IL	I/O	Current limiter control. Programmable using an external resistor to GND. Do not float this pin.
11	ILTIMER	I	Capacitor programmed fault timer control during current limiting mode. Connecting this pin to VIN uses the internal current limit timer and connecting this pin to GND disables the internal timer functionality for the ILTIMER as well as retry mode. In this case, the device will remain at programmed current limit indefinitely in the event of a short without going intro retry mode. Do not float this pin.
12	SS	I/O	Switch slew rate control. See the *Adjustable Rise Time* section for more information.
13	VOUT	O	Switch output. A minimum 10-µF output capacitor is recommended.
14			
15			
16			
—	Thermal Pad	—	Thermal pad (exposed center pad) for heat dissipation purposes. Thermal pad is internally connected to seal ring and GND.

(1) Thermal pad is internally connected to the seal ring and GND.

Table 1. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Ground	ALCU	1050 nm
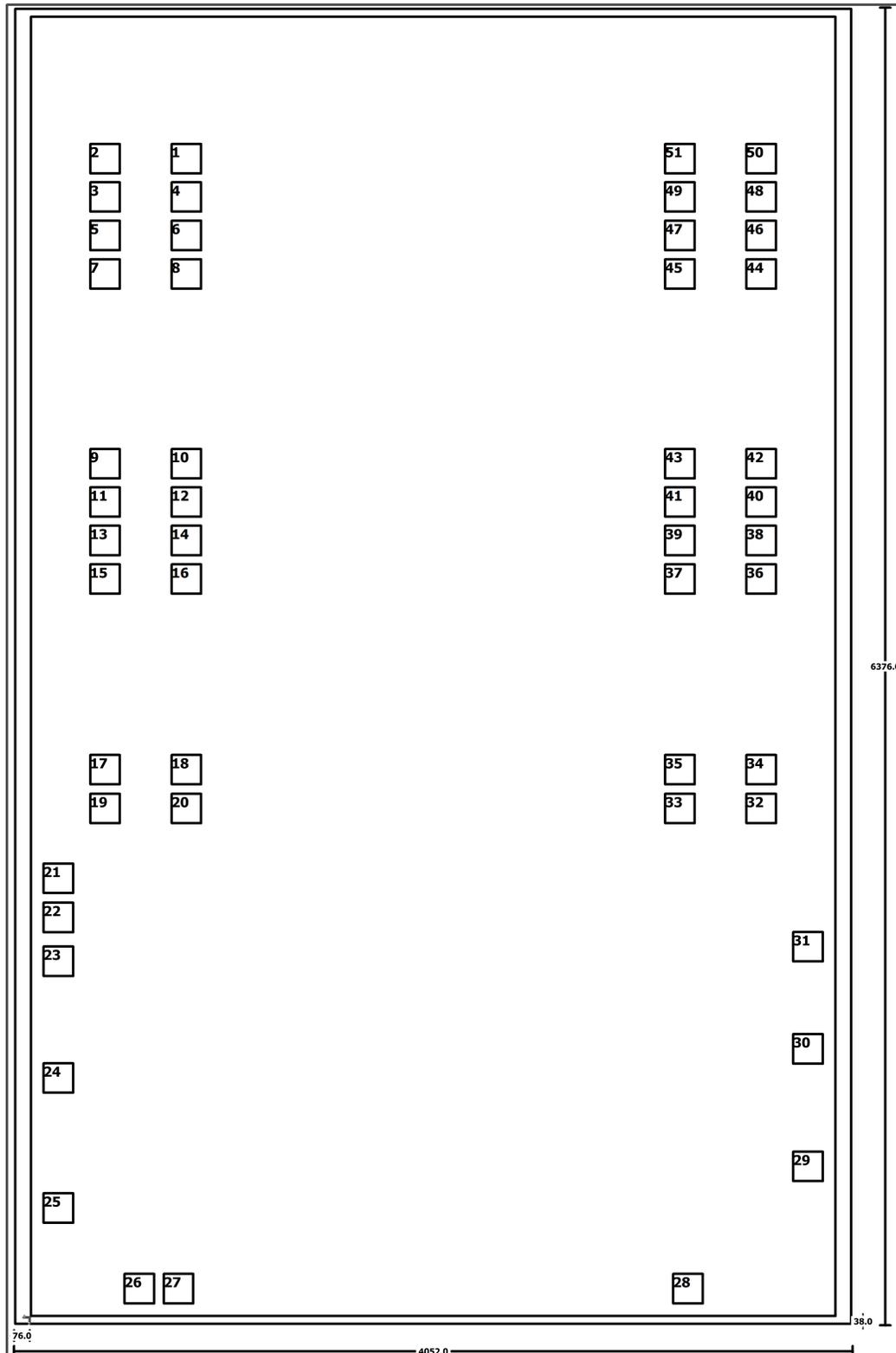
Table 2. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VIN	1	679.75	5529	835.25	5684.5
VIN	2	286.85	5529	442.35	5684.5
VIN	3	286.85	5343.5	442.35	5499
VIN	4	679.75	5343.5	835.25	5499
VIN	5	286.85	5157.1	442.35	5312.6
VIN	6	679.75	5157.1	835.25	5312.6
VIN	7	286.85	4970.65	442.35	5126.15
VIN	8	679.75	4970.65	835.25	5126.15
VIN	9	286.85	4053	442.35	4208.5
VIN	10	679.75	4053	835.25	4208.5
VIN	11	286.85	3867.5	442.35	4023
VIN	12	679.75	3867.5	835.25	4023
VIN	13	286.85	3681.1	442.35	3836.6
VIN	14	679.75	3681.1	835.25	3836.6
VIN	15	286.85	3494.65	442.35	3650.15
VIN	16	679.75	3494.65	835.25	3650.15
VIN	17	286.85	2572.85	442.35	2728.35
VIN	18	679.75	2572.85	835.25	2728.35
VIN	19	286.85	2384.85	442.35	2540.35
VIN	20	679.75	2384.85	835.25	2540.35
AVDD	21	61.1	2046.7	216.6	2202.2
AVDD	22	61.1	1857.2	216.6	2012.7
CS	23	61.1	1645.3	216.6	1800.8
EN	24	61.1	1080.75	216.6	1236.25
OVP	25	61.1	451.4	216.6	606.9
GND	26	452.45	61.1	607.95	216.6
GND	27	641.95	61.1	797.45	216.6
RTIMER	28	3103.2	61.1	3258.7	216.6
IL	29	3683.4	652.7	3838.9	808.2
ILTIMER	30	3683.4	1221.4	3838.9	1376.9
SS	31	3683.4	1715.65	3838.9	1871.15
VOUT	32	3457.4	2384.85	3612.9	2540.35
VOUT	33	3064.5	2384.85	3220	2540.35
VOUT	34	3457.4	2572.85	3612.9	2728.35
VOUT	35	3064.5	2572.85	3220	2728.35
VOUT	36	3457.4	3494.65	3612.9	3650.15
VOUT	37	3064.5	3494.65	3220	3650.15
VOUT	38	3457.4	3681.1	3612.9	3836.6
VOUT	39	3064.5	3681.1	3220	3836.6
VOUT	40	3457.4	3867.5	3612.9	4023
VOUT	41	3064.5	3867.5	3220	4023
VOUT	42	3457.4	4053	3612.9	4208.5
VOUT	43	3064.5	4053	3220	4208.5
VOUT	44	3457.4	4970.65	3612.9	5126.15
VOUT	45	3064.5	4970.65	3220	5126.15
VOUT	46	3457.4	5157.1	3612.9	5312.6
VOUT	47	3064.5	5157.1	3220	5312.6

Product Folder Links: *TPS7H2201-SP*

Table 2. Bond Pad Coordinates in Microns (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VOUT	48	3457.4	5343.5	3612.9	5499
VOUT	49	3064.5	5343.5	3220	5499
VOUT	50	3457.4	5529	3612.9	5684.5
VOUT	51	3064.5	5529	3220	5684.5

Product Folder Links: *TPS7H2201-SP*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)(2)]

		MIN	MAX	UNIT
VIN	Input voltage	−0.3	7.5	V
VOUT	Output voltage	−0.3	7.5	V
EN, OVP	Enable and over voltage protection pins	−0.3	7.5	V
CS, ILTIMER, RTIMER, IL, SS	Current sense, current limit timer, retry timer, current limit and soft start pins	−0.3	VIN + 0.3	V
I_{MAX}	Maximum continuous switch current		9	A
I_{PLS}	Maximum pulsed switch current (t≤5µs)		45	A
T_J	Maximum junction temperature	−55	150	°C
T_{stg}	Storage temperature	−65	150	°C

(1)   Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±750	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VIN	Input voltage	1.5	7	V
SR_{VIN}	Input voltage slew rate		0.01	V/µs
VOUT	Output voltage	0	VIN	V
I_{MAX}	Maximum continuous switch current		6	A
T_J	Operating junction temperature[(1)]	−55	125	°C

(1)   In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the equation: $T_{A(max)} = T_{J(max)} − (\theta_{JA} \times P_{D(max)})$.

Product Folder Links: *TPS7H2201-SP*

6.4 Thermal Information

THERMAL METRIC		TPS7H2201-SP	UNIT
		HKR (CFP)	
		16 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SUBGROUP[1]	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
VIN_{HUVLO}	Internal VIN UVLO voltage, rising				1.32		V
VIN_{LUVLO}	Internal VIN UVLO voltage, falling				1.23		V
$HYST_{VIN-UVLO}$	Internal VIN UVLO hysteresis				92		mV
I_Q	Quiescent current	I_{OUT} = 0 mA, V_{IN} = EN = 5 V, CS resistor of 20 kΩ to GND	1, 2, 3		2.4	6.5	mA
I_F	VIN to VOUT forward leakage current	EN = VOUT = GND, measured VOUT current	1, 2, 3			3	mA
I_{SD} VIN	VIN off-state supply current	EN = GND, I_{OUT} = 0 mA, measured VIN current	VIN = 5 V	1, 2, 3		0.4	3	mA
			VIN = 3.3 V	1, 2, 3		0.3	3	
			VIN = 1.8 V	1, 2, 3		0.2	3	
			After TID = 100 krad, VIN = 1.8, 3.3, and 5 V	1			3.1	
I_{RCP}	Reverse current protection leakage current	EN = 0 V, VIN = 0 to 7 V, VOUT = 0 to 7 V for VOUT > VIN	1, 2, 3		0.45	2.5	mA
		EN = 7 V, VIN = 0 V, VOUT = 0 to 7 V					
SOFT START							
I_{SS}	Soft start charge current	1 V on SS pin	1, 2, 3		65	83	µA
SR_{SS}	Soft start slew rate	SS pin floating, COUT = 10 µF			295		mV/µs
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT							
V_{IHEN}	EN/UVLO threshold voltage, rising		1, 2, 3	0.56	0.61	0.65	V
V_{ILEN}	EN/UVLO threshold voltage, falling		1, 2, 3	0.47	0.51	0.55	V
$HYST_{EN}$	EN/UVLO hysteresis voltage		1, 2, 3		93	124	mV
t_{LOW}	EN signal low time during cycling	RTIMER = GND, IL = 1 A, I_{VOUT} = 2 A	9, 10, 11	20			µs
VIN_{EN}	VIN percentage for enable		4, 5, 6	75%			
I_{EN}	EN pin input leakage current	EN = VIN = 5 V	1, 2, 3			12	nA
OVERVOLTAGE PROTECTION (OVP)							
V_{OVPR}	OVPR thresld voltage, rising		1, 2, 3	0.52	0.57	0.63	V
V_{OVPF}	OVPF threshold voltage, falling		1, 2, 3	0.5	0.55	0.59	V
$HYST_{OVP}$	OVP hysteresis voltage	1.6 V < VIN < 7 V	1, 2, 3		20	55	mV
I_{OVP}	OVP pin input leakage current		1, 2, 3			15	nA
CURRENT LIMIT AND CURRENT SENSE							
t_{CSEN}	Time for valid CS output after enable	C_{SS} = 120 nF	9, 10, 11			5	ms
	Minimum VOUT current for valid CS output		1, 2, 3	750			mA
	VOUT current change to CS change delay time	0.5-A rising step, 100 mA/µs, 1.5 V ≤ VIN ≤ 7 V	9, 10, 11		16	74	µs
	VOUT current change to CS change delay time	0.5-A falling step, 100 mA/µs, 1.5 V ≤ VIN ≤ 7 V	9, 10, 11		16	73	µs
	CS pin accuracy	0.75 A ≤ I_{VOUT} ≤ 7.5 A	4, 5, 6	−10%		10%	
	CS pin voltage	0.75 A ≤ I_{VOUT} ≤ 7.5 A, no OCP	1, 2, 3			VIN – 0.4	V

(1) For subgroup definitions, see Quality Conformance Inspection table.

Product Folder Links: *TPS7H2201-SP*

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP[1]	MIN	TYP	MAX	UNIT
Current limit setting, I_{IL}		$I_{VOUT} \leq 1$ A		1, 2, 3	I_{VOUT} + 0.5			A
		1A < $I_{VOUT} \leq 3$ A		1, 2, 3	I_{VOUT} + 1			
		I_{VOUT} > 3 A		1, 2, 3	I_{VOUT} + 1.5			
Programmable current limit accuracy		1.5 V ≤ VIN ≤ 7 V		4, 5, 6	−20%		20%	
Fast trip off current limit		VIN = 5 V, 10-mΩ short in 10 µs				22		A
Fast trip off off-time		VIN = 5 V, C_{SS} = 2.7 nF		9, 10, 11		61	158	µs
Internal current limit timer (fast trip off current limit)		VIN = 5 V, I_{VOUT} = 3 A, IL = 6 A, ILTIMER = VIN, 10-mΩ short in 10 µs		9, 10, 11		15	35	µs
TIMERS								
$I_{ILTIMER}$	ILTIMER charge current			1, 2, 3	0.7	1	1.38	µA
$PD_{ILTIMER}$	ILTIMER internal pull-down resistance	40 mV on ILTIMER pin		1, 2, 3		38	153	Ω
I_{RTIMER}	RTIMER charge current			1, 2, 3	0.7	1	1.38	µA
PD_{RTIMER}	RTIMER internal pull-down resistance	40 mV on RTIMER pin		1, 2, 3		38	153	Ω
THERMAL SHUTDOWN								
Thermal shutdown		VIN = 5 V				175		°C
Thermal shutdown hysteresis		VIN = 5 V				20		°C
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance, lead length = 2.5 mm	VIN = 7 V, I_{IL} = 7.5 A	−55°C	1, 2, 3			24	mΩ
			−40°C				26	
			25°C			31	34	
			85°C			37	40	
			125°C			41	45	
		VIN = 5 V, I_{IL} = 7.5 A	−55°C	1, 2, 3			26	
			−40°C				27	
			25°C			32	35	
			85°C			39	42	
			125°C			43	47	
		VIN = 3.3 V, I_{IL} = 7.5 A	−55°C	1, 2, 3			28	
			−40°C				30	
			25°C			35	38	
			85°C			42	46	
			125°C			47	52	
		VIN = 1.8 V, I_{IL} = 7.5 A	−55°C	1, 2, 3			36	
			−40°C				39	
			25°C			45	51	
			85°C			55	62	
			125°C			61	70	
		VIN = 1.5 V, I_{IL} = 7.5 A	−55°C	1, 2, 3			44	
			−40°C				48	
			25°C			52	63	
			85°C			63	77	
			125°C			70	87	

Product Folder Links: *TPS7H2201-SP*

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN = EN = 5 V, T$_A$ = 25°C (unless otherwise noted)						
t$_{ON}$	Turn-on time	R$_L$ = 10 Ω, C$_L$ = 10 µF, C$_{SS}$ = 1000 pF		208		µs
t$_{OFF}$	Turn-off time	R$_L$ = 10 Ω, C$_L$ = 10 µF, C$_{SS}$ = 1000 pF		60		µs
t$_F$	VOUT fall time	R$_L$ = 10 Ω, C$_L$ = 10 µF, C$_{SS}$ = 1000 pF		90		µs
t$_{ASSERT}$	OVP assert time	R$_L$ = 10 Ω, C$_L$ = 10 µF, C$_{SS}$ = 1000 pF		4.5		µs
t$_{DEASSERT}$	OVP deassert time	R$_L$ = 10 Ω, C$_L$ = 10 µF, C$_{SS}$ = 1000 pF		9.6		µs
VIN = EN = 1.5 V, T$_A$ = 25°C (unless otherwise noted)						
t$_{ON}$	Turn-on time	R$_L$ = 10 Ω, C$_L$ = 10 µF, C$_{SS}$ = 1000 pF		173		µs
t$_{OFF}$	Turn-off time	R$_L$ = 10 Ω, C$_L$ = 10 µF, C$_{SS}$ = 1000 pF		64		µs
t$_F$	VOUT fall time	R$_L$ = 10 Ω, C$_L$ = 10 µF, C$_{SS}$ = 1000 pF		70		µs
t$_{ASSERT}$	OVP assert time	R$_L$ = 10 Ω, C$_L$ = 10 µF, C$_{SS}$ = 1000 pF		2.65		µs
t$_{DEASSERT}$	OVP deassert time	R$_L$ = 10 Ω, C$_L$ = 10 µF, C$_{SS}$ = 1000 pF		6.56		µs

6.7 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	−55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	−55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	−55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	−55

Product Folder Links: *TPS7H2201-SP*

6.8 Typical Characteristics
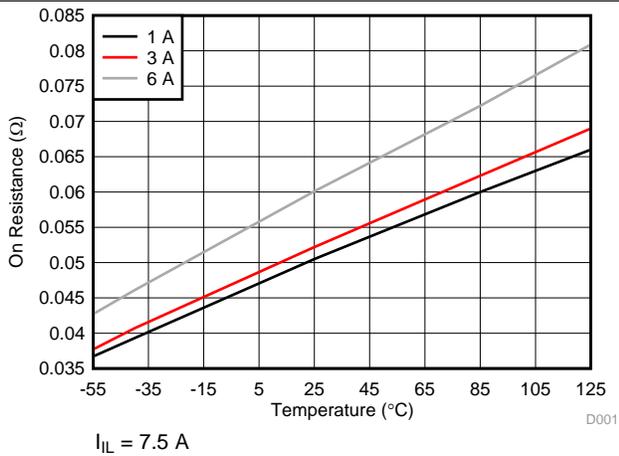
Figure 1. On-Resistance vs Temperature Across Loads at VIN = 1.5 V

I_{IL} = 7.5 A
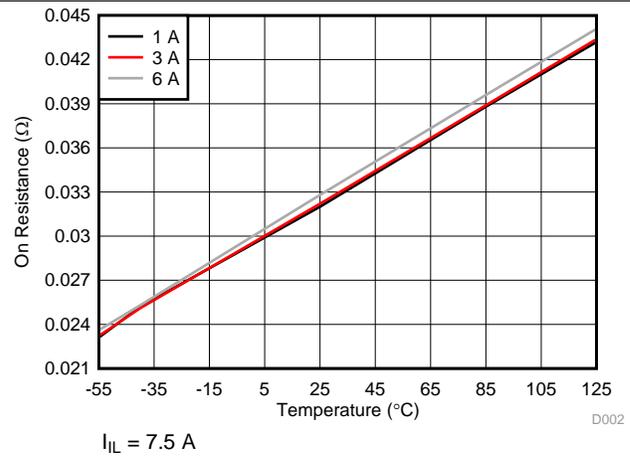
Figure 2. On-Resistance vs Temperature Across Loads at VIN = 5 V

I_{IL} = 7.5 A
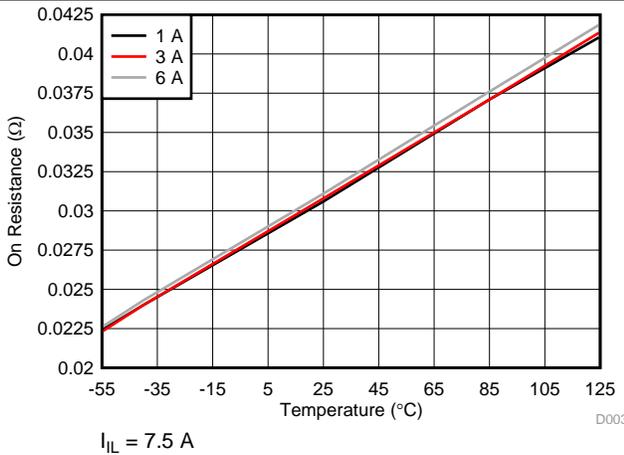
Figure 3. On-Resistance vs Temperature Across Loads at VIN = 7 V

I_{IL} = 7.5 A
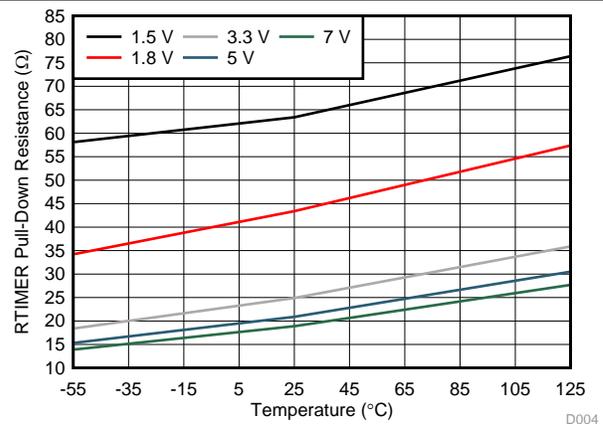
Figure 4. RTIMER Pull-Down Resistance vs Temperature Across VIN
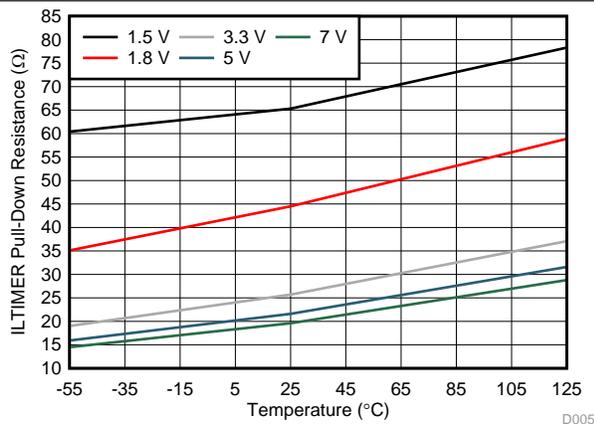
Figure 5. ILTIMER Pull-Down Resistance vs Temperature Across VIN
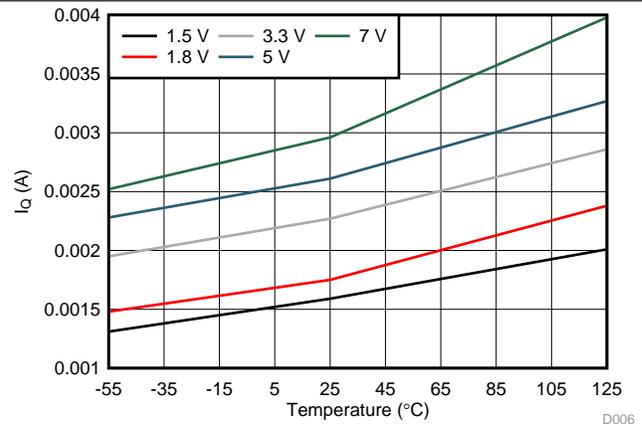
Figure 6. I_Q vs Temperature Across VIN

Product Folder Links: *TPS7H2201-SP*

Typical Characteristics (continued)

Figure 7. I$_{RCP}$ vs Temperature With EN = 7 V

Figure 8. I$_{RCP}$ vs Temperature With EN = GND

Figure 9. I$_{SD}$ VIN vs Temperature Across VIN

Figure 10. ILTIMER Charge Current vs Temperature Across VIN

Figure 11. RTIMER Charge Current vs Temperature Across VIN

Figure 12. SS Charge Current vs Temperature Across VIN

Product Folder Links: *TPS7H2201-SP*
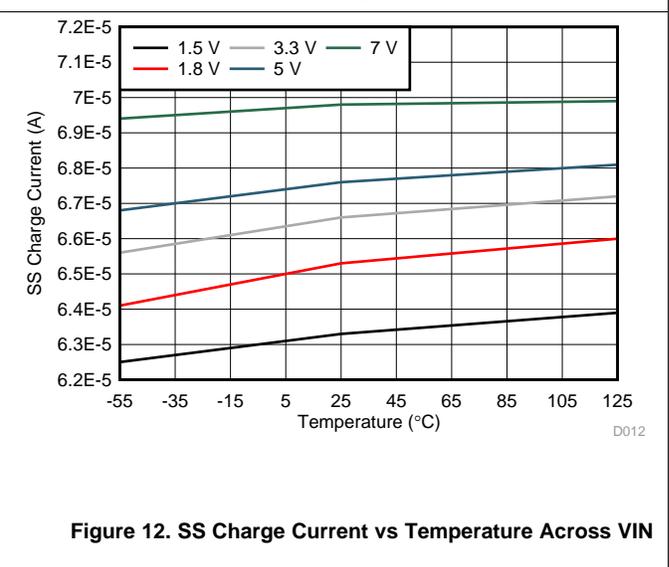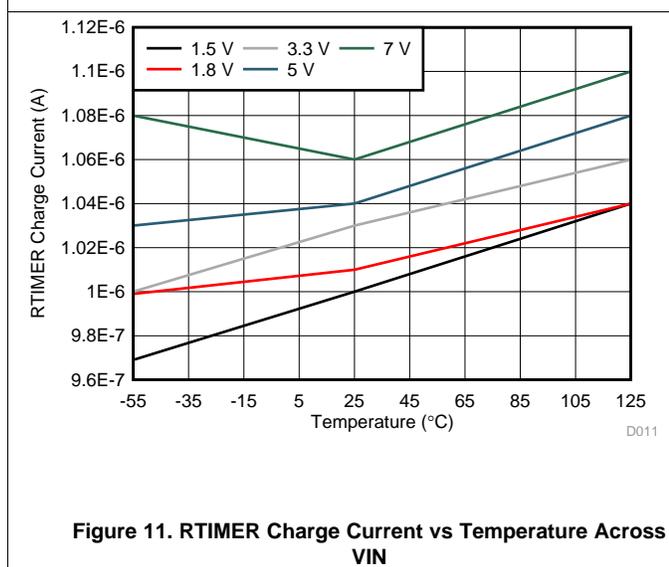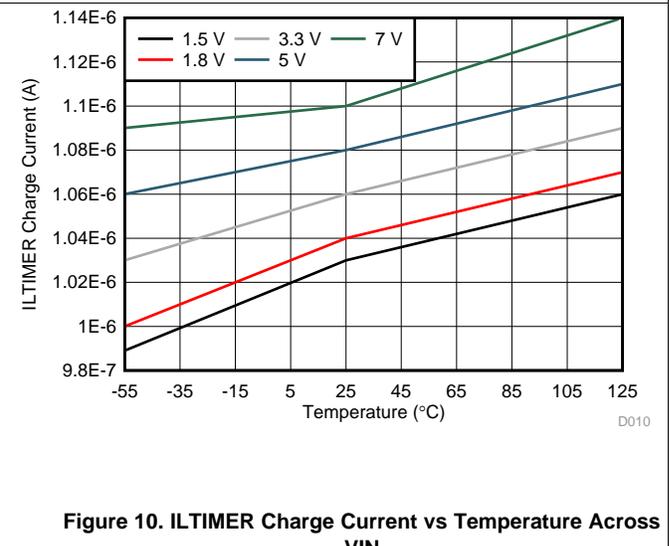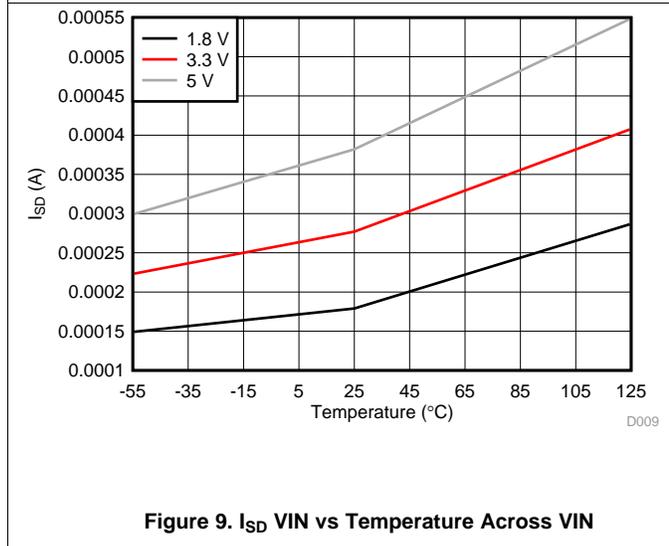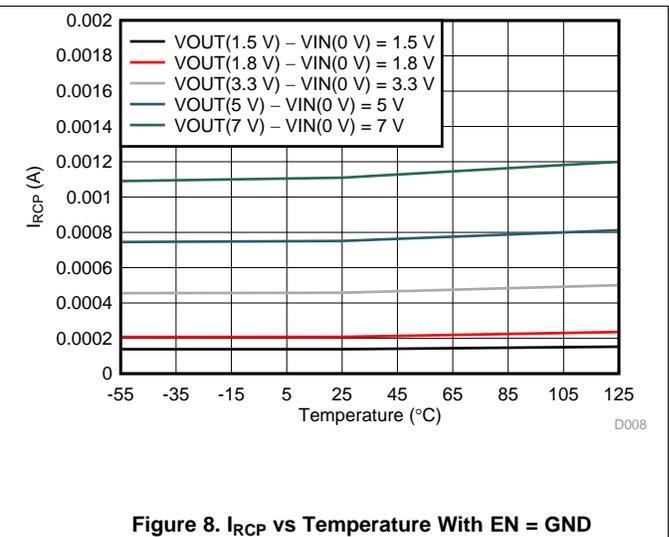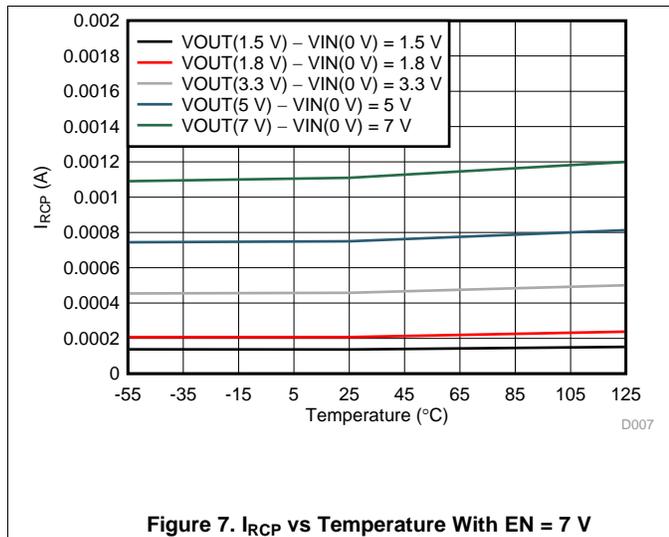
Typical Characteristics (continued)
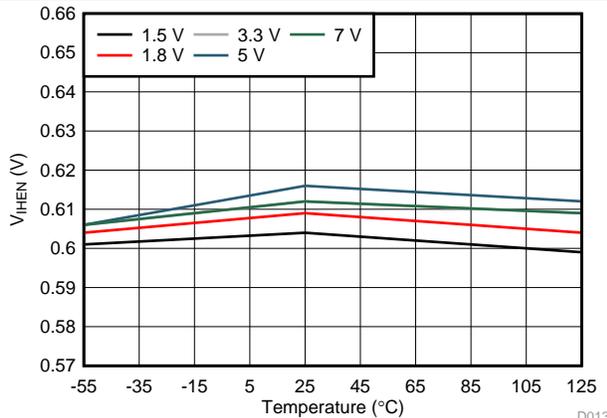
EN pin driven directly

Figure 13. V_IHEN vs Temperature Across VIN
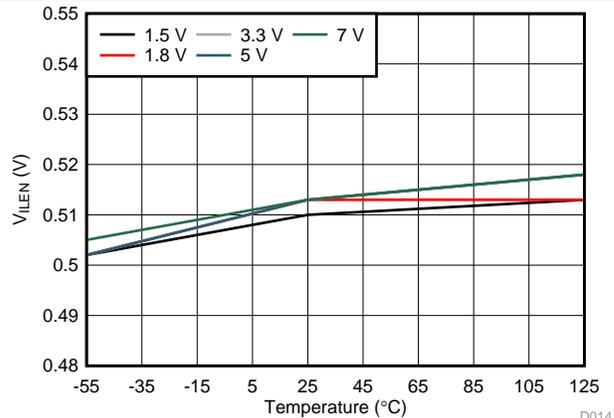
EN pin driven directly

Figure 14. V_ILEN vs Temperature Across VIN
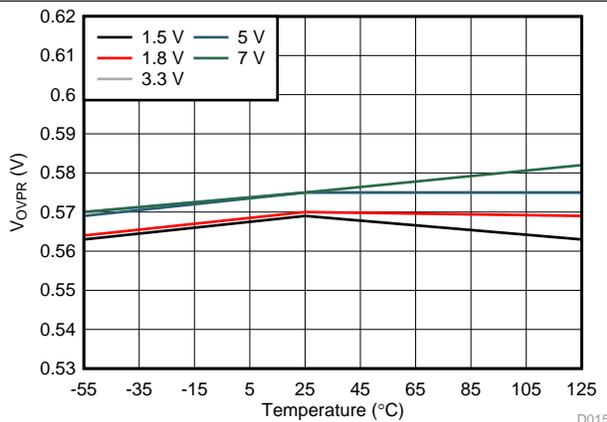
OVP pin driven directly

Figure 15. V_OVPR vs Temperature Across VIN
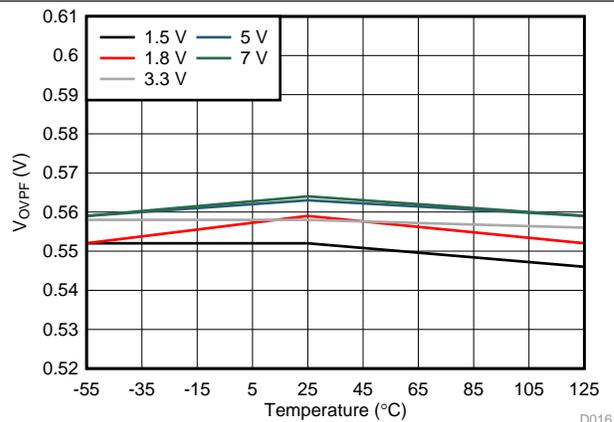
OVP pin driven directly

Figure 16. V_OVPF vs Temperature Across VIN
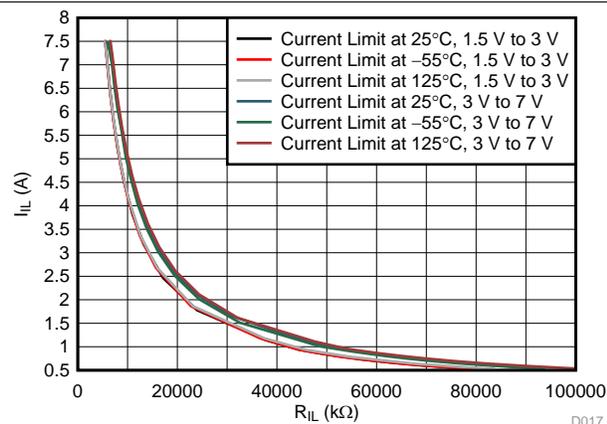
Figure 17. I_IL vs R_IL Across Temperature
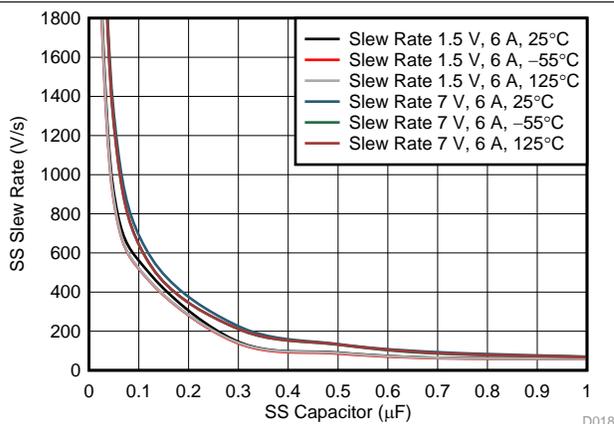
Figure 18. SS Slew Rate vs SS Capacitor Across Temperature

7 Parameter Measurement Information
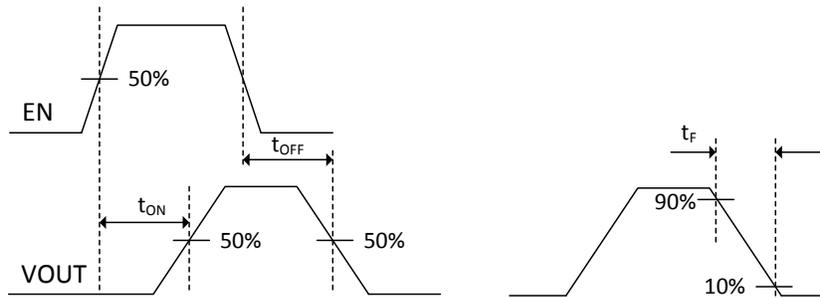
Figure 19. t_{ON}/t_{OFF} Waveforms
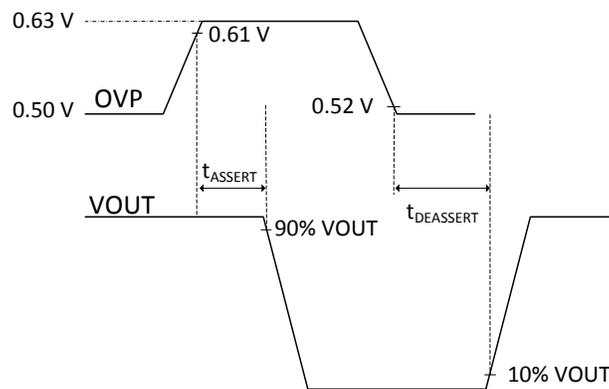
Figure 20. $t_{ASSERT}/t_{DEASSERT}$ Waveforms
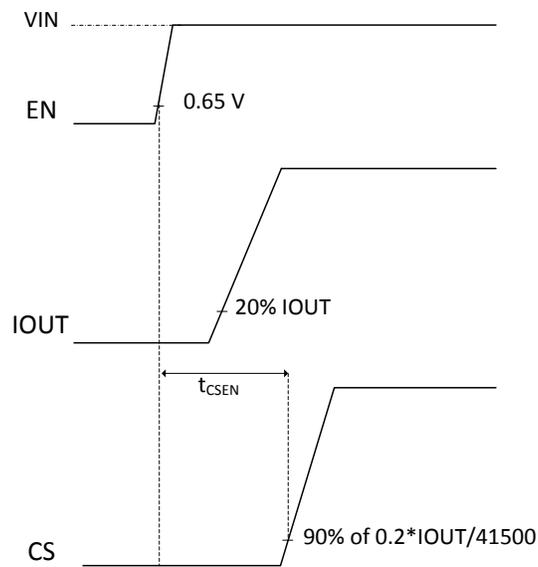
Figure 21. t_{CSEN} Waveforms
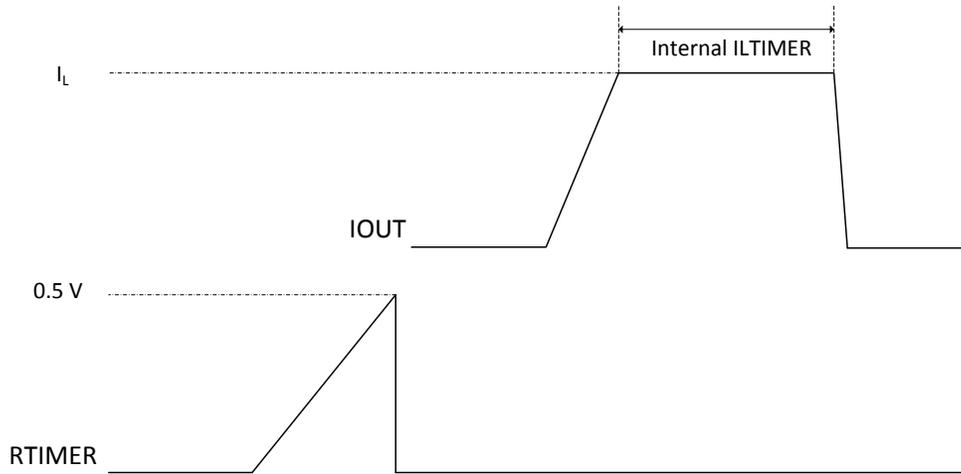
Figure 22. Internal ILTIMER Waveforms
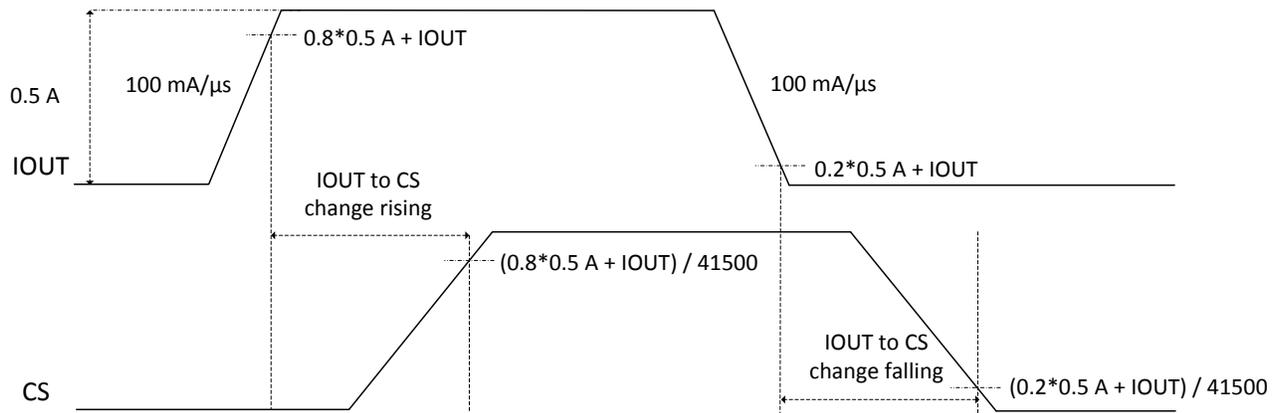
Figure 23. VOUT Current to CS Change Delay Time

8 Detailed Description

8.1 Overview

The TPS7H2201-SP device is a single channel, 6-A load switch with a programmable slew rate for applications that require specific rise-time as well as programmable current limit for protection purposes. In addition, the TPS7H2201-SP features a reverse current protection capability for power distribution applications.

8.2 Functional Block Diagram

Product Folder Links: *TPS7H2201-SP*
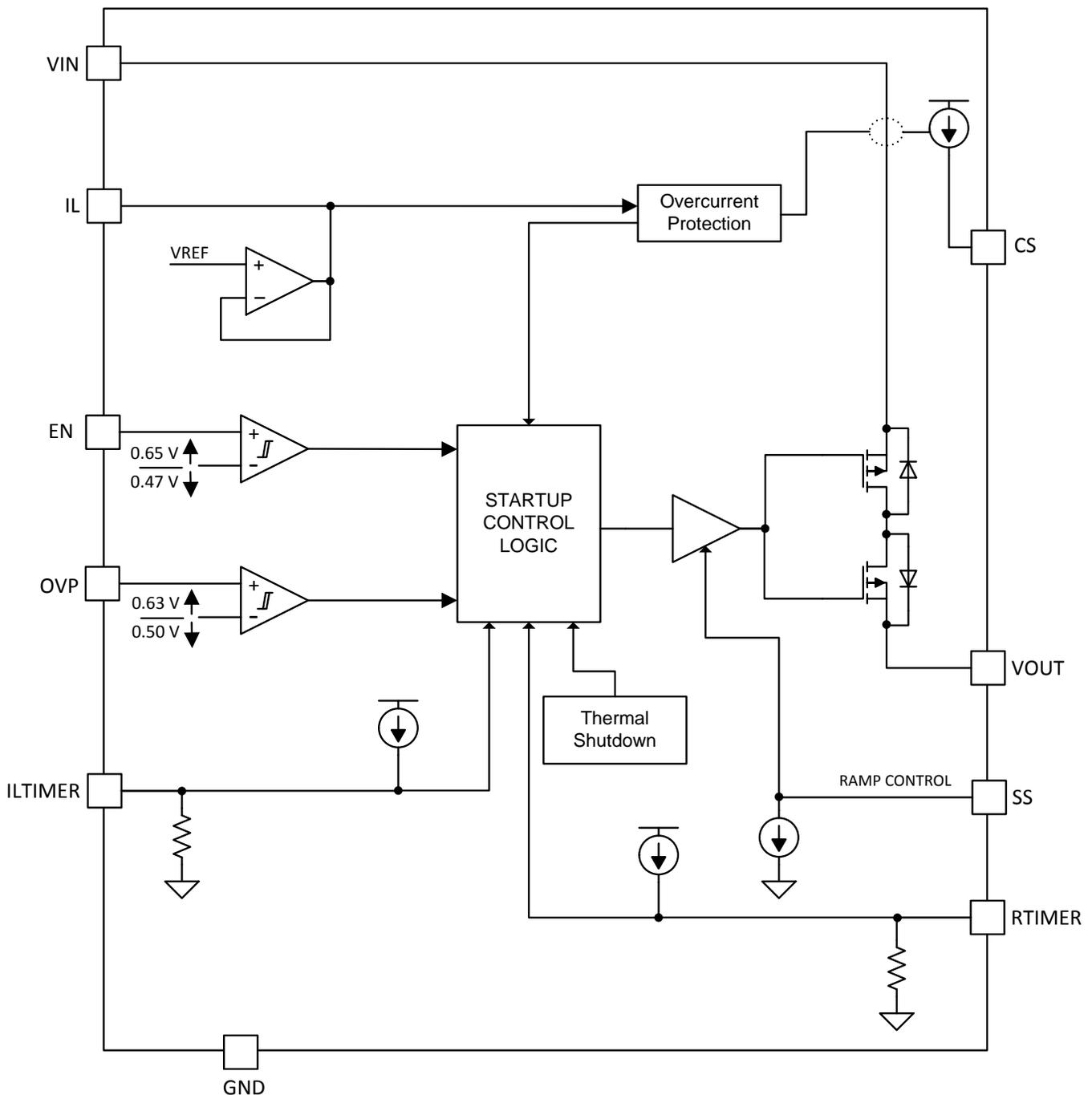
8.3 Feature Description

8.3.1 Enable, Undervoltage, and Overvoltage Protection

Figure 24 shows how resistor dividers from VIN connected to the EN and OVP pins can be used to set the UVLO and OVP trip voltages. The EN pin controls the ON and OFF state of the internal FET. A voltage at this pin greater than V_{IHEN} turns on the FET and a voltage less than V_{ILEN} turns it off. The addition of an external resistor divider from VIN allows the EN pin to configure a different enable rising voltage or an undervoltage monitor (UVLO) based on the V_{IHEN} and V_{ILEN} specifications respectively. Typically, applications are optimized to either configure the enable rising voltage or the UVLO threshold. As an example, Equation 1 can be used to calculate the UVLO trip point fixing R_{TOP_EN} = 100 kΩ.

In a similar way to the EN pin, the overvoltage protection (OVP) feature of the device can be configured using a resistor divider from VIN connected to the OVP pin. The trip voltage for the OVP has to be less than the absolute maximum VIN voltage. A voltage at the OVP pin greater than V_{OVPR} will trip the OVP feature and will turn off the FET and a voltage less than V_{OVPF} will keep the FET on. If this feature is not desired, the OVP pin should be grounded. Equation 2 can be used to calculated the rising OVP trip point fixing R_{TOP_OVP} = 100 kΩ.
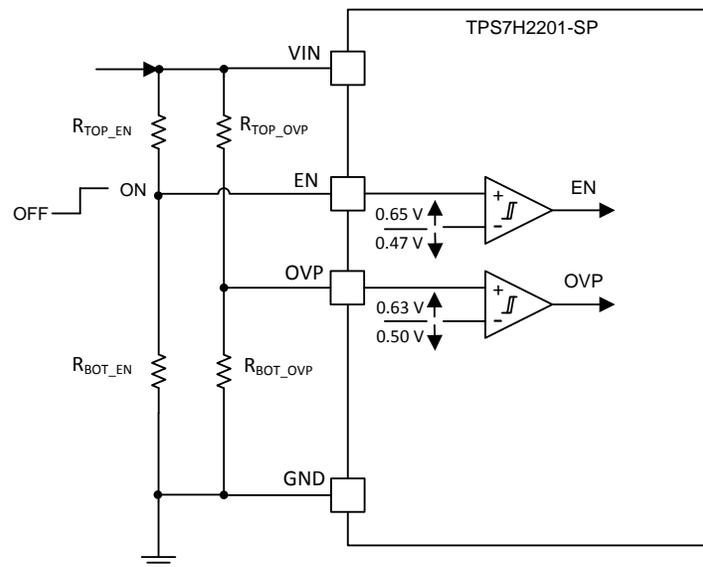

Figure 24. UVLO and OVP Thresholds Set by Resistor Dividers

$$R_{BOT\_EN}(k\Omega) \leq \frac{47}{V_{UVLO\_TRIP}(V) - 0.47}$$

(1)

$$R_{BOT\_OVP}(k\Omega) \geq \frac{63}{V_{OVP\_TRIP}(V) - 0.63}$$

(2)

8.3.2 Adjustable Rise Time

An external capacitor, C_{SS}, connected between the VOUT and SS pins sets the slew rate. The desired slew rate VOUT$_{SR}$ is determined by t_r, the rise time in seconds, and ∆V, the change in VOUT voltage in Volts as shown in Equation 3.

$$VOUT_{SR}(V/s) = \frac{\Delta V_{OUT}(V)}{t_r(s)}$$

(3)

In order to avoid false trips due to the programmable current limit, the desired slew rate must be less than VOUT$_{SR,MAX}$ as shown in Equation 4, where I_L is the programmed current limit, I_{VOUT} is the normal operation current flowing through the switch, and C_{OUT} is the output capacitor.

$$VOUT_{SR,MAX}(V/s) < \frac{0.8 \times I_L(A) - 0.95 \times I_{VOUT}(A)}{C_{OUT}(F)}$$

(4)

Feature Description (continued)

Once the slew rate has been calculated and meeting the constraint in Equation 4, the C_{SS} capacitor is then calculated using Equation 5 for VIN < 3-V and IOUT ≥ 3-A applications. For all other applications, use Equation 6.

$$C_{SS}(\mu F) = \frac{45}{VOUT_{SR}(V/s)}$$

for VIN < 3 V and IOUT ≥ 3 A

(5)

$$C_{SS}(\mu F) = \frac{65}{VOUT_{SR}(V/s)}$$

for all other conditions

(6)

8.3.3 Programmable Current Limiting

A current limit can be programmed using an external resistor connected from the IL pin to GND. This programmed current limit (±20% accurate) refers to the continuous current through the device and therefore, when operated at its maximum current rating (6 A), the programmed current limit needs to be set 20% higher. As shown in Figure 25, a current limit event of this nature is defined as a soft short. The resistor value R_{IL}, can be calculated using Equation 7 for VIN ≤ 3 V, and Equation 8 for VIN > 3 V, where I_L is the programmed current limit value in amperes. This programmable current limiting feature is different from the internal current limiting activated during fast trip mode as shown in Figure 26. A current limit event in this case is defined as a hard short and this current limit (typical of 22 A) cannot be programmed.

$$R_{IL}(\Omega) = \frac{45500}{I_L(A)}$$

for VIN ≤ 3 V

(7)

$$R_{IL}(\Omega) = \frac{49000}{I_L(A)}$$

for VIN > 3 V

(8)

8.3.4 Programmable Fault Timer

A capacitor connected from the ILTIMER pin to GND determines the programmable current limit fault time duration. The ILTIMER pin will charge the capacitor to 0.5 V during an overload condition and will discharge it otherwise through an internal pull down resistance. The time that the device will be in current limit before turning off is configured by $C_{ILTIMER}$ and the time can be calculated using Equation 9. Connecting this pin to VIN will cause the device to be disabled once the internal current limit timer expires as shown in Figure 22. However, connecting it to GND will disable the internal timer functionality completely and therefore, in the case of a short, the device will remain at the programmed current limit indefinitely. When using the internal timer, only the fast trip off current limit is active.

$$t(\mu s) = \frac{C(pF)}{2}$$

(9)

The time that the device remains disabled after the current limit timer expires is configurable through a capacitor connected from the RTIMER pin to GND. The RTIMER pin will charge the capacitor to 0.5 V after the switch is turned off and will discharge it otherwise. The time can be calculated using Equation 9. Connecting this pin to GND will keep the device disabled and it will require the device to be enabled by cycling the EN pin. The behavior of the ILTIMER and RTIMER pins for a soft short, hard short and internal timer conditions are shown in Figure 25, Figure 26, and Figure 27, respectively. Please notice that Figure 25 and Figure 26 assume the fault is not present after the switch has been disabled and enabled again (retry mode). If the fault is present after the retry mode, the device will go into current limit mode and this cycle will repeat until the fault is no longer present.

Feature Description (continued)
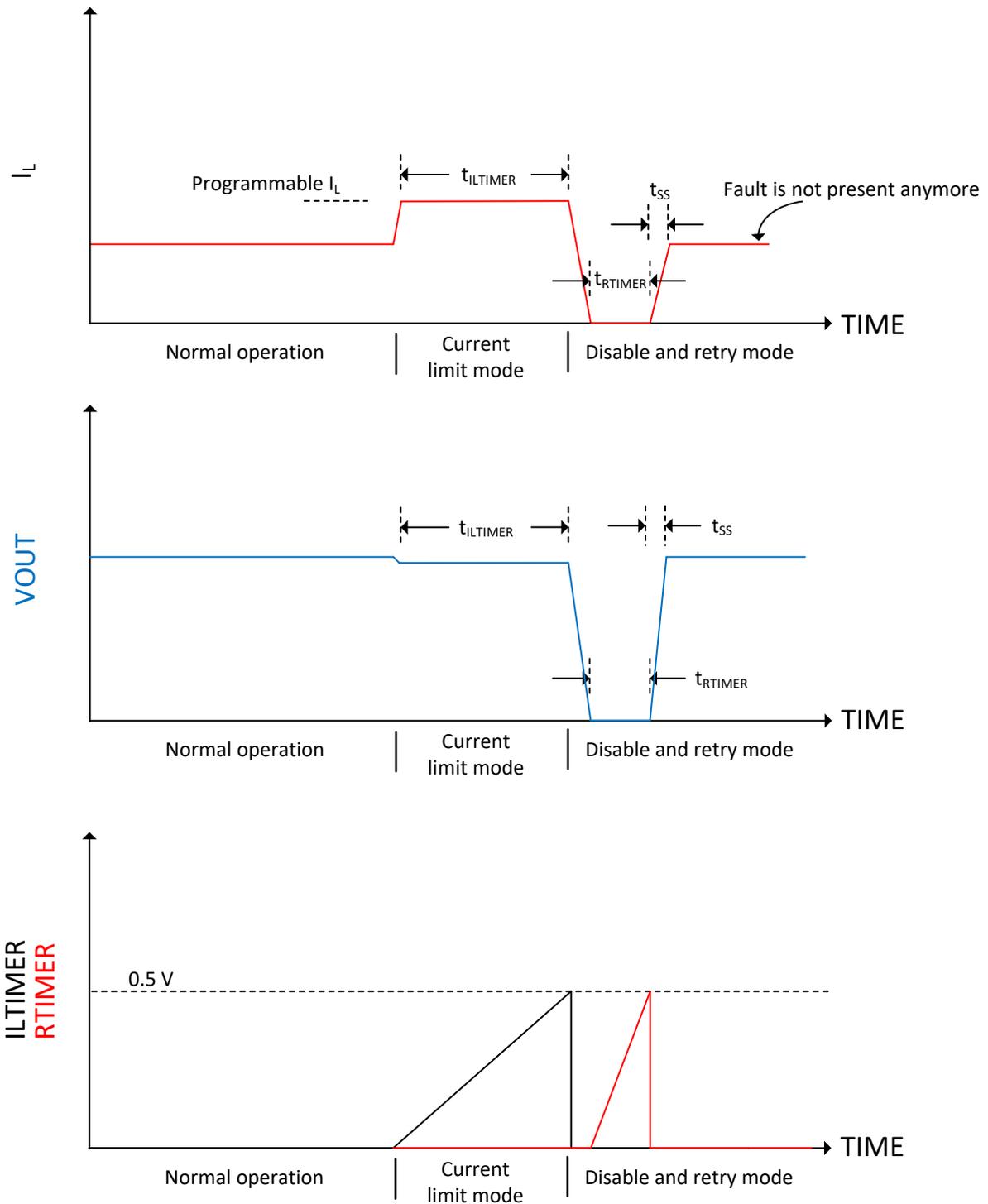
Figure 25. Soft Short Programmable Fault Timer Operation Connecting Capacitors to ILTIMER and RTIMER Pins

Product Folder Links: *TPS7H2201-SP*

Feature Description (continued)

Figure 26. Hard Short Programmable Fault Timer Operation Connecting Capacitors to ILTIMER and RTIMER Pins

Feature Description (continued)
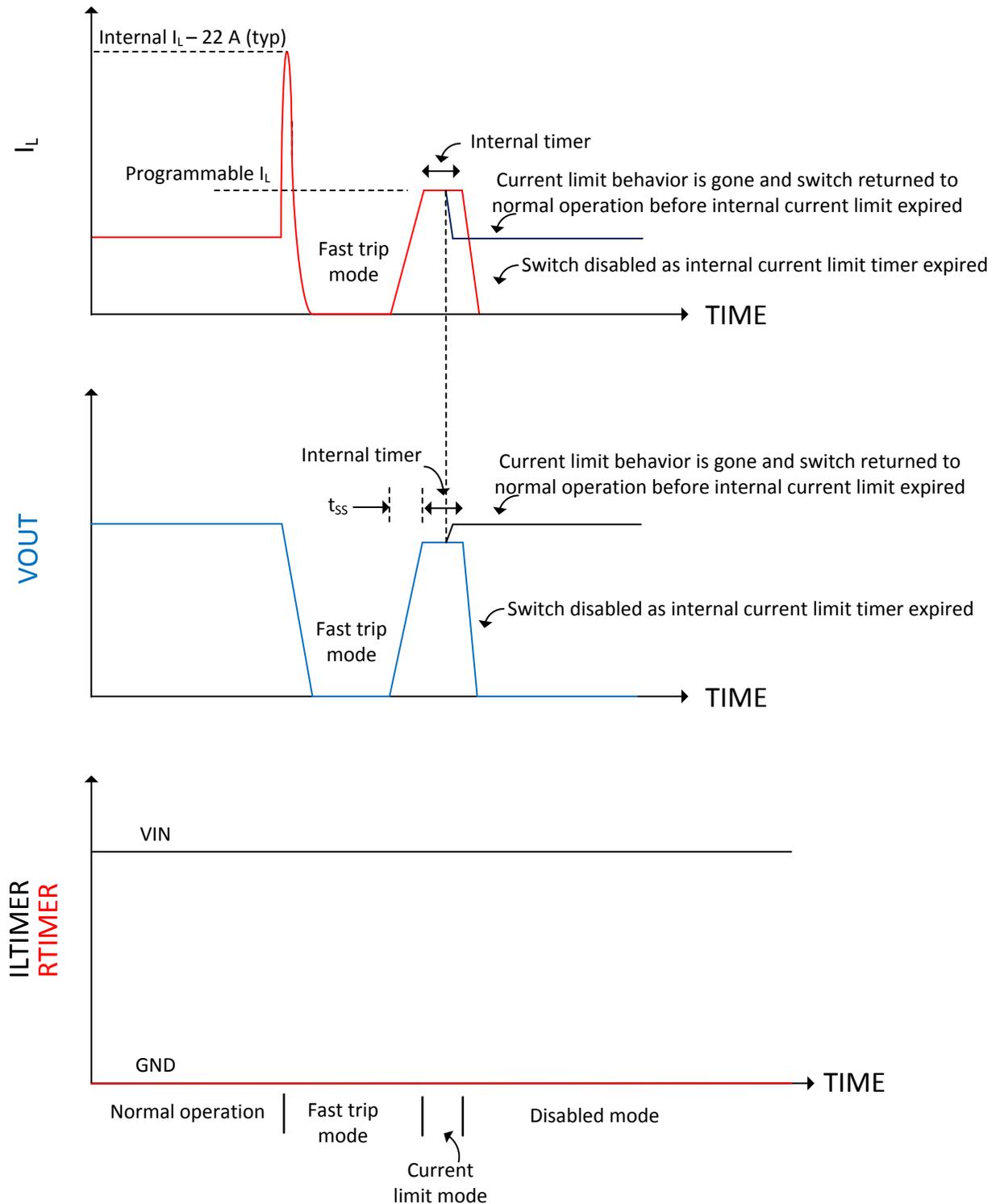
**Figure 27. Programmable Fault Timer Operation Using the Internal Current Limit Timer and Disabling the Retry Mode**

Feature Description (continued)

The programmable fault timers, ILTIMER and RTIMER, should be set in such a way that the capacitor for one timer is discharged before the other timer expires to ensure proper operation. In the specific case of using the internal ILTIMER, the RTIMER capacitor should be sized such that it is discharged before the internal ILTIMER expires, assuming the fault is still present. Figure 28 shows a situation where this constraint is not met as the RTIMER is much larger than the ILTIMER and therefore, the C_{RTIMER} is not discharged before the $C_{ILTIMER}$ reaches 0.5 V, which is when the ILTIMER will expire. In order to avoid this situation, the constraint shown in Equation 10 must be met. Using this equation, once a capacitor for a timer has been selected (C_1 in Equation 10), the maximum value for the capacitor of the second timer can be determined. The internal pull-down resistance for each of the timers can be found in the *Electrical Characteristics* table. For the situation shown in Figure 28, C_1 and R_{PD1} in Equation 10 correspond to the RTIMER.
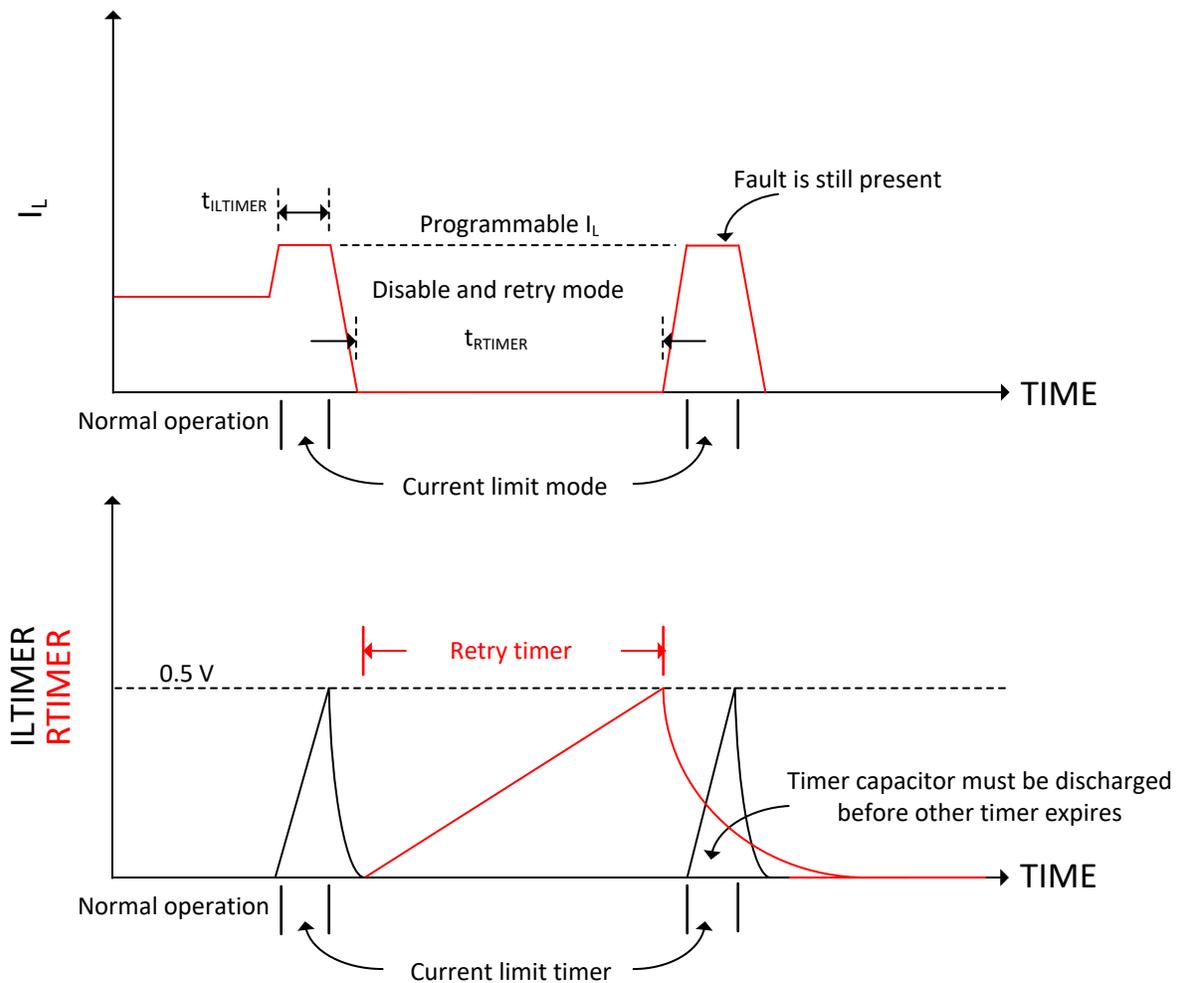

Figure 28. Programmable Fault Timer Capacitors Constraint

$$C_1(\mu F) < \frac{C_2(pF)}{8 \times R_{PD1}(\Omega)}$$

(10)

Product Folder Links: *TPS7H2201-SP*

Feature Description (continued)

8.3.5 Current Sense

This pin will output a current proportional to the output current of the switch for current sensing applications. A resistor to GND will convert this current to voltage for current sensing purposes. The output current will be the switch current divided by 41,500. The CS pin will have a valid output 5 ms after the device has been enabled.

8.3.6 Parallel Operation

The TPS7H2201-SP can be configured in parallel operation either to increase the current capability, up to 12 A, or to reduce the on-state resistance. In this case, all pins are shared as shown in Figure 29, except the current limit resistor (R_{IL}) for proper operation of the internal current limit loop. The current limiting resistors must be sized as described in the Programmable Current Limiting section.

Product Folder Links: TPS7H2201-SP

Feature Description (continued)
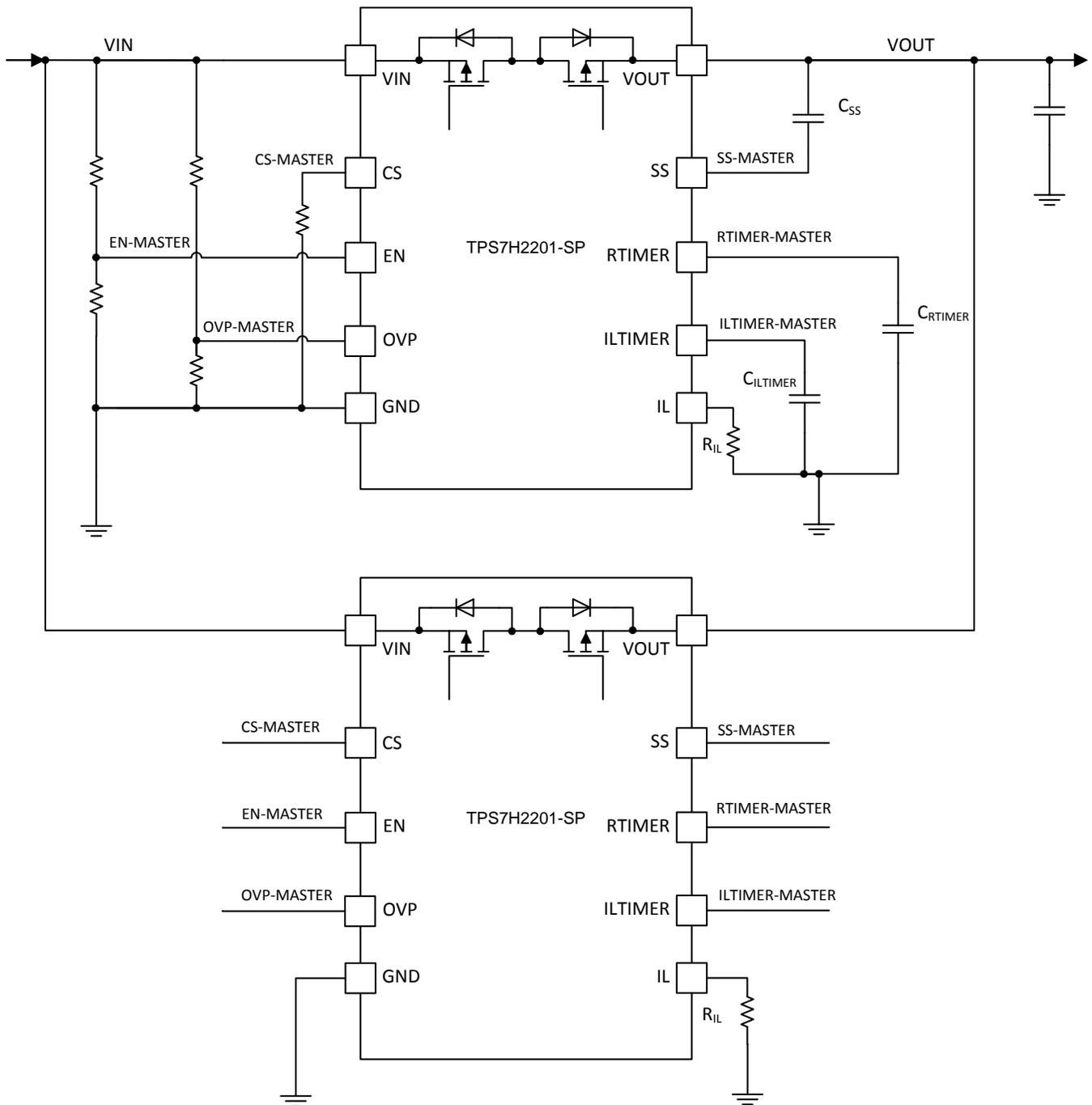
Figure 29. Parallel Configuration to Reduce Resistance or Increase Current Capability

8.4 Device Functional Modes

Table 3 lists the VOUT pin states as determined by the EN pin.

Table 3. VOUT Connection

EN PIN	TPS7H2201-SP
< V_{ILEN}	Open
> V_{IHEN}	VIN

Product Folder Links: *TPS7H2201-SP*

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H2201-SP device is a single channel, 6-A load switch with multiple programmable features such as current limit, undervoltage and overvoltage, current limit and retry timers, and soft start. In addition, the TPS7H2201-SP features a reverse current protection capability for power distribution applications and current sensing for load monitoring purpose. The TPS7H2201-SP user's guide is available on the TI website, *TPS7H2201EVM-CVAL Evaluation Module (EVM) User's Guide*. The guide highlights standard EVM configurations, test results, schematic, and BOM for reference.

9.2 Typical Applications

In addition to the standard power management applications where a power switch can be used, there are 2 main applications in which the TPS7H2201-SP can be used in space power applications:

- Redundancy for primary and secondary voltage rails common in satellite applications
- Protection for critical or SEL sensitive loads

9.2.1 Redundancy

In applications where primary and secondary (redundant) power rails are present, the TPS7H2201-SP is ideal to implement redundancy because of its reverse current blocking capability. In this case, since the load switch is placed at the input of the point of load regulator, the on-resistance of the switch is not as critical.

Typical Applications (continued)
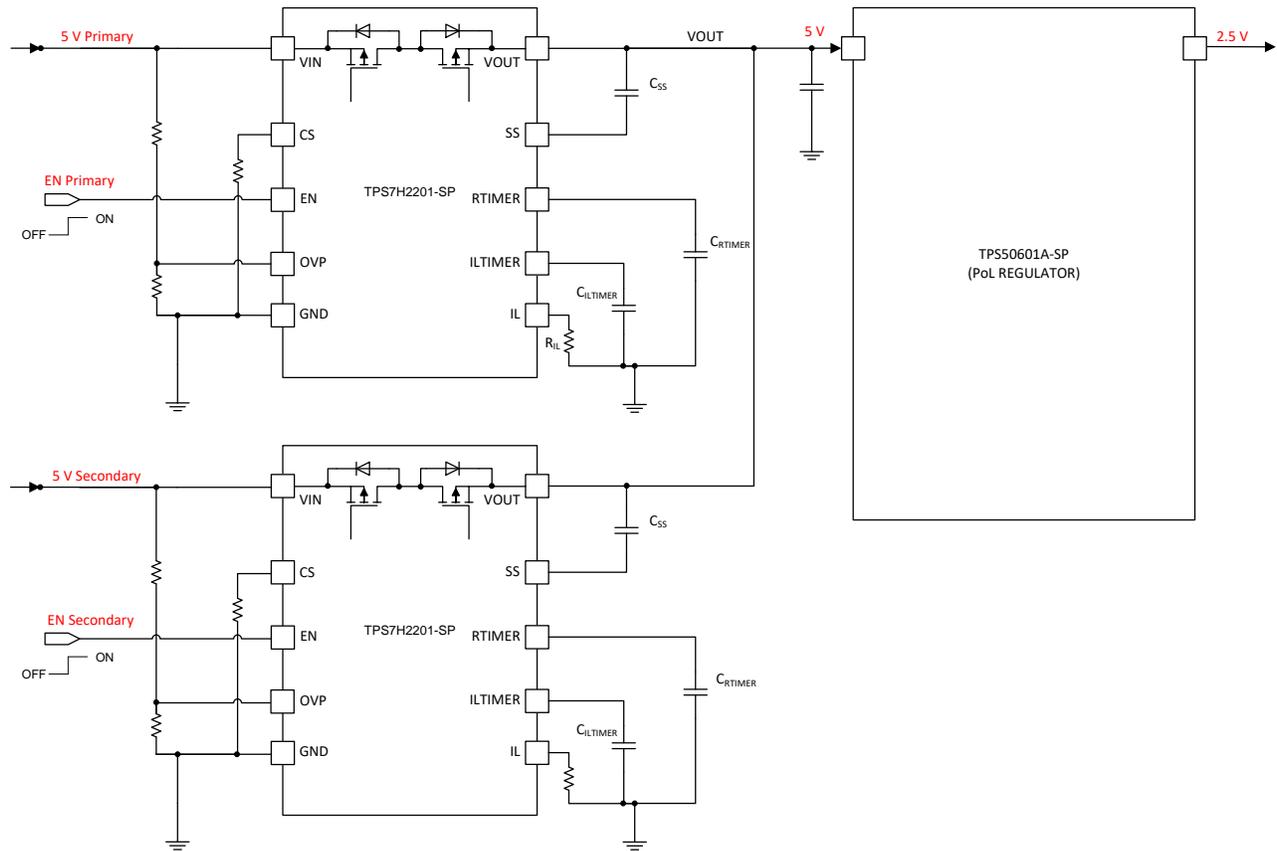
Figure 30. Redundancy Example Using the TPS7H2201-SP

9.2.2 Protection

The protection features of the TPS7H2201-SP can also be used for SEL sensitive loads. In such case, the on-resistance of the switch might be more relevant as it is placed after the point of load regulator but in such case, two load switches can be placed in parallel to reduce the on-resistance if needed. The main advantages of using the load switch at this location is faster response to SEL events and automatic recovery due to the retry mode of the programmable fault timer.

Typical Applications (continued)
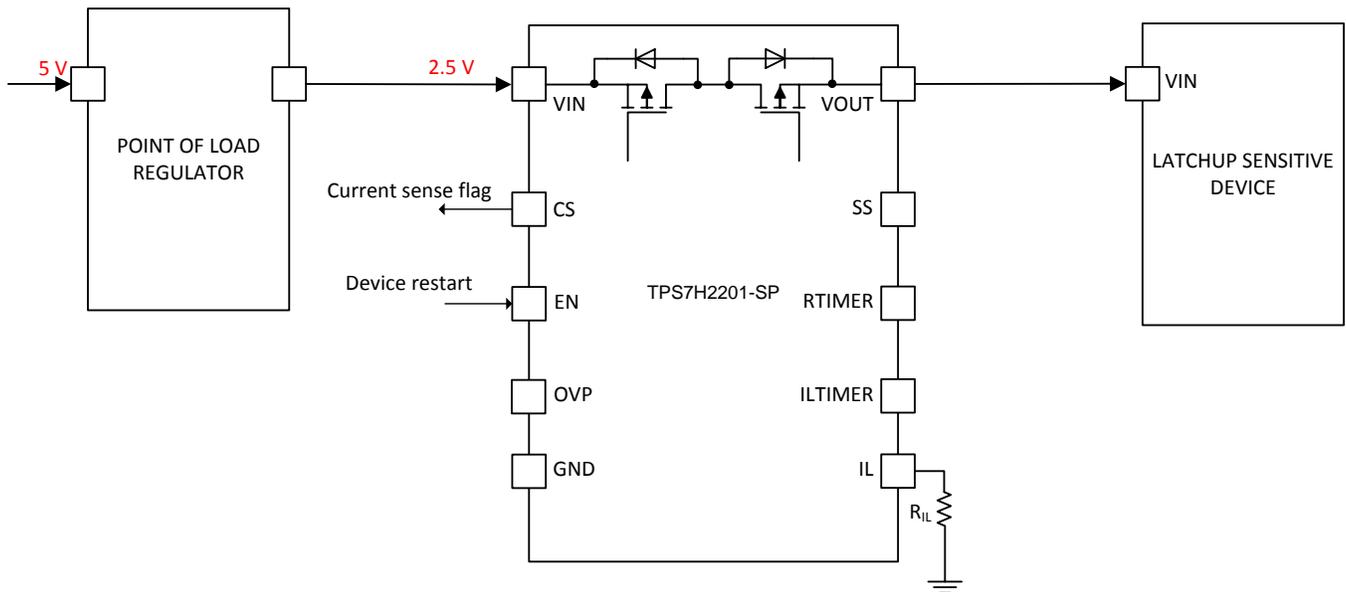
Figure 31. Protection Example Using the TPS7H2201-SP

9.2.3 Design Requirements

Figure 32 shows a typical application schematic that is applicable to both the redundancy and the protection applications previously discussed.
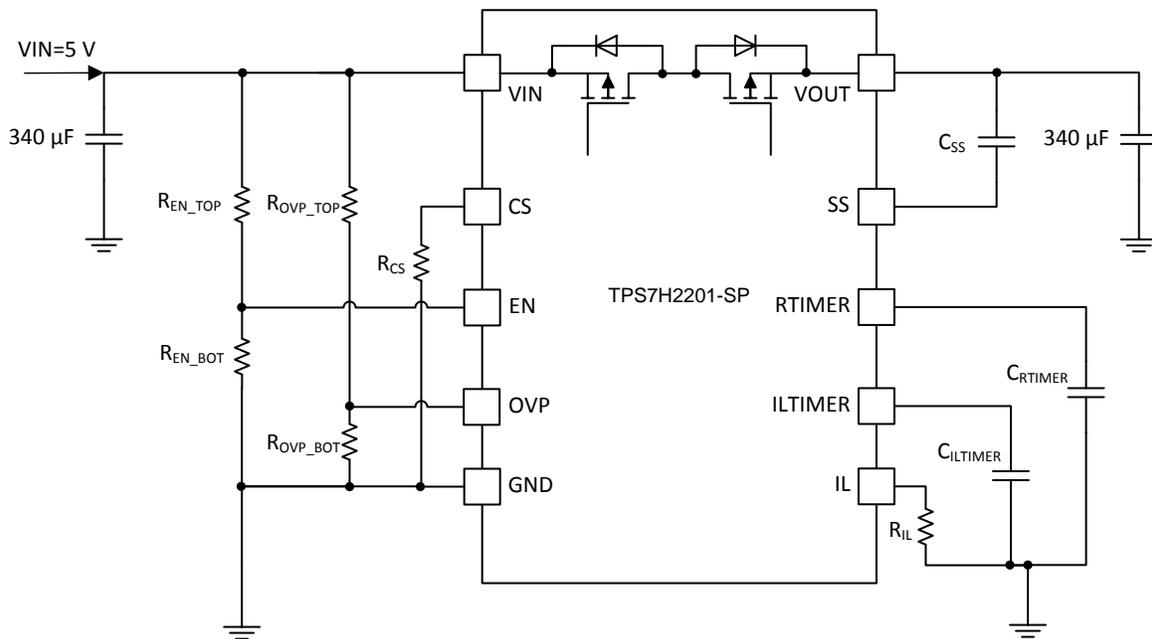

Figure 32. Typical Application Schematic

Table 4 shows the design parameters.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VIN	5 V
Undervoltage lockout set point	3.5 V
Overvoltage protection set point	6.5 V
Output current	6 A
Current limit	7.5 A
Current limit timer	1 ms
Retry timer	1 ms
Soft start time	9 ms
Input and output capacitors	340 μF

9.2.4 Detailed Design Procedure

9.2.4.1 Undervoltage Lockout

The undervoltage lockout set point is configured using the resistor divider, R_{EN_TOP} and R_{EN_BOT} connected to the EN pin. Set the R_{EN_TOP} = 100 kΩ and, using Equation 1, calculate the value for R_{EN_BOT}. For an UVLO = 3.5 V, R_{EN_BOT} = 15.5 kΩ. When choosing the UVLO set point, the resistor divider must ensure that the device will still get enabled for the VIN used in the application. This is achieved by making sure that the V_{IHEN} requirement is still met with the chosen resistor divider and that the VIN needed to meet the requirement is smaller than the VIN used in the application. Equation 11 shows this VIN and V_{IHEN} requirement to set the UVLO point. For this particular application, the requirement is met as the result is 4.84 V.

$$V_{IHEN} \times \frac{R_{EN\_TOP} + R_{EN\_BOT}}{R_{EN\_BOT}} \leq VIN$$

(11)

9.2.4.2 Overvoltage Protection

In a similar way to the UVLO set point, the overvoltage protection set point is configured using the resistor divider, R_{OVP_TOP} and R_{OVP_BOT} connected to the OVP pin. Set the R_{OVP_TOP} = 100 kΩ and, using Equation 2, calculate the value for R_{OVP_BOT}. For an OVP = 6.5 V, R_{OVP_BOT} = 10.7 kΩ. When choosing the OVP set point, the resistor divider must ensure that the device will still get enabled for the VIN used in the application. This is achieved by making sure that the V_{OVPF} requirement is still met with the chosen resistor divider and that the VIN needed to meet the requirement is larger than the VIN used in the application. Equation 12 shows this VIN and V_{OVPF} requirement to set the OVP point. For this particular application, the requirement is met as the result is 5.16 V.

$$V_{OVPF} \times \frac{R_{OVP\_TOP} + R_{OVP\_BOT}}{R_{OVP\_BOT}} \geq VIN$$

(12)

9.2.4.3 Current Limit

The current limit is configured using R_{IL}. Based on the output current for this design, the minimum current limit that can be programmed is IOUT + 1.5 A for a total of 7.5 A. As a result, using Equation 8, the resistor value is 6.53 kΩ.

9.2.4.4 Programmable Fault Timers

The programmable fault timers are configured using the $C_{ILTIMER}$ and the C_{RTIMER} capacitors. For this particular design, both timers are set to 1 ms. Therefore, using Equation 9, the value for each capacitor is 2000 pF. These capacitor values meet the requirement in Equation 10.

9.2.4.5 Soft Start Time

The soft start time is configured using the C_{SS} capacitor. In order to calculate the value of the capacitor, the VOUT slew rate needs to be calculated using Equation 3 to make sure the maximum VOUT slew rate requirement shown in Equation 4 is satisfied. This requirement is particularly important for space applications where large output capacitance is typically used, which translates to a lower maximum allowable VOUT slew rate. For this particular design, the VOUT slew rate is 555 V/s which is less than the maximum VOUT slew rate of 882 V/s, meeting the requirement from Equation 4. Now, the soft start capacitor value can be calculated as 117 nF using Equation 6, since VIN = 5 V for this application.

9.2.5 Application Curves

The power-up behavior of this design example is shown in Figure 33 and the current limit behavior is shown in Figure 34.
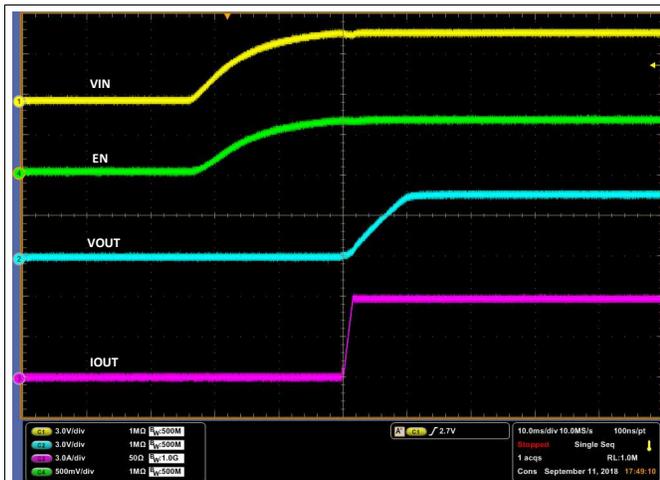
Figure 33. Power-up Behavior of the TPS7H2201-SP
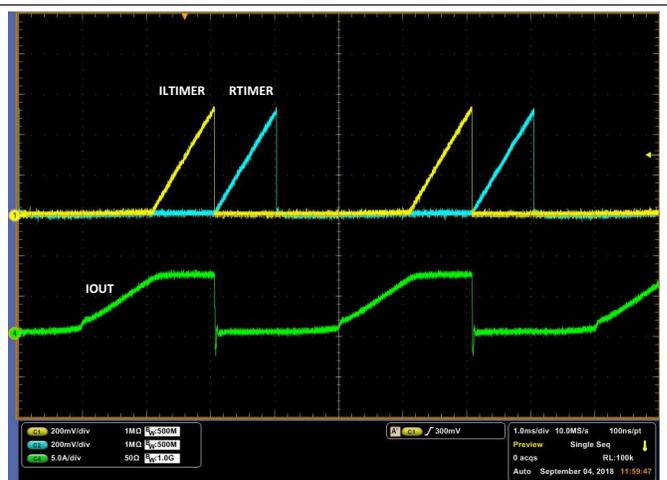
Figure 34. ILTIMER and RTIMER Waveforms When IL is Set to 7.5 A

10   Power Supply Recommendations

The TPS7H2201-SP is designed to operate from an input voltage supply range between 1.5 V to 7 V. This supply voltage must be well regulated and proper local bypass capacitors should be used for proper electrical performance from VIN to GND. Due to stringent requirements for space applications, typically numerous input bypass capacitors are used and the total capacitance is much larger than for commercial applications. The TPS7H2201-SP Evaluation Module uses one 330-µF tantalum capacitor in parallel with one 10-µF and one 0.1-µF ceramic capacitor.

11   Layout

11.1   Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects. In general, the components should be placed close to the device such that traces remain as short as possible to avoid parasitic capacitance. In addition, due to the possibility of large power dissipation in fault conditions (short at VOUT), thermal vias should be placed in the PCB for the thermal pad.

11.2   Layout Example
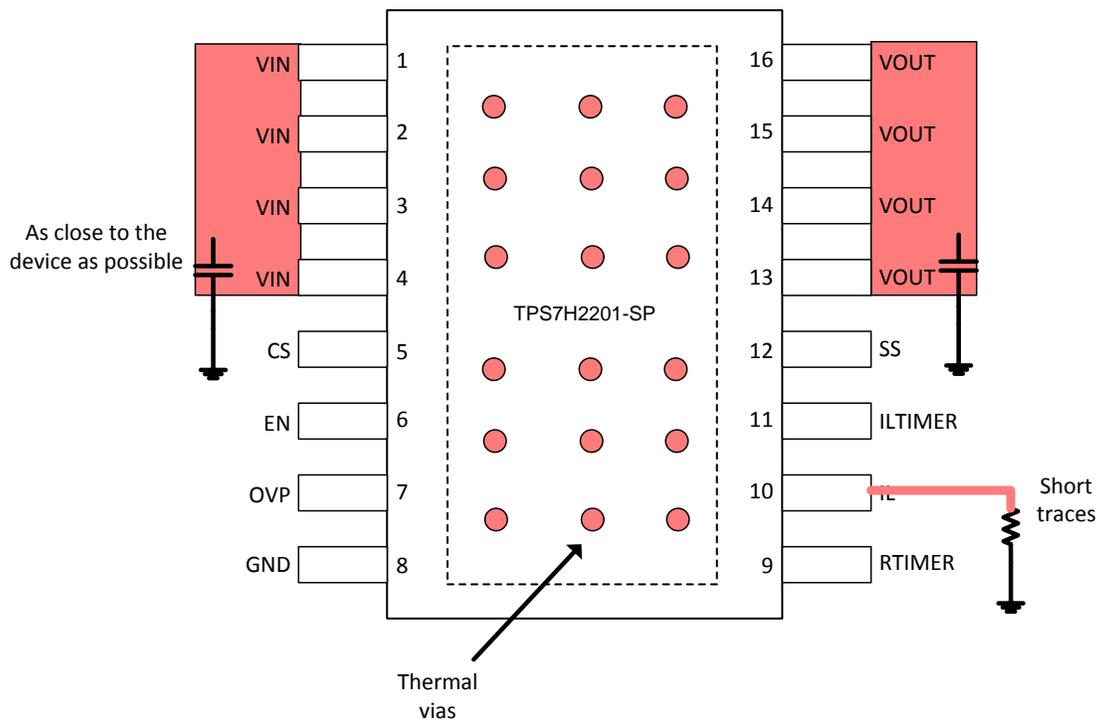
Figure 35. Layout Recommendation

Product Folder Links: *TPS7H2201-SP*

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H2201EVM-CVAL Evaluation Module (EVM) User's Guide*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1722001VXC	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962-1722001VXC TPS7H2201MHKRV	Samples
5962R1722001V9A	ACTIVE	XCEPT	KGD	0	25	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962R1722001VXC	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R1722001VXC TPS7H2201MHKRV	Samples
TPS7H2201HKR/EM	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	25 to 25	TPS7H2201HKREM	Samples
TPS7H2201Y/EM	ACTIVE	XCEPT	KGD	0	5	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
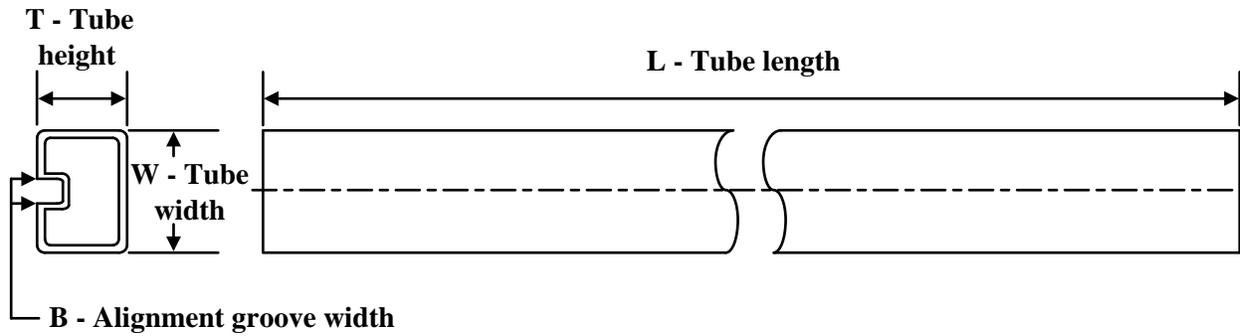
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1722001VXC	HKR	CFP	16	1	506.98	26.16	6220	NA
5962R1722001VXC	HKR	CFP	16	1	506.98	26.16	6220	NA
TPS7H2201HKR/EM	HKR	CFP	16	1	506.98	26.16	6220	NA

PACKAGE MATERIALS INFORMATION

TRAY

L - Outer tray length without tabs

KO - Outer tray height

W - Outer tray width

P1 - Tray unit pocket pitch

CW - Measurement for tray edge (Y direction) to corner pocket center
CL - Measurement for tray edge (X direction) to corner pocket center
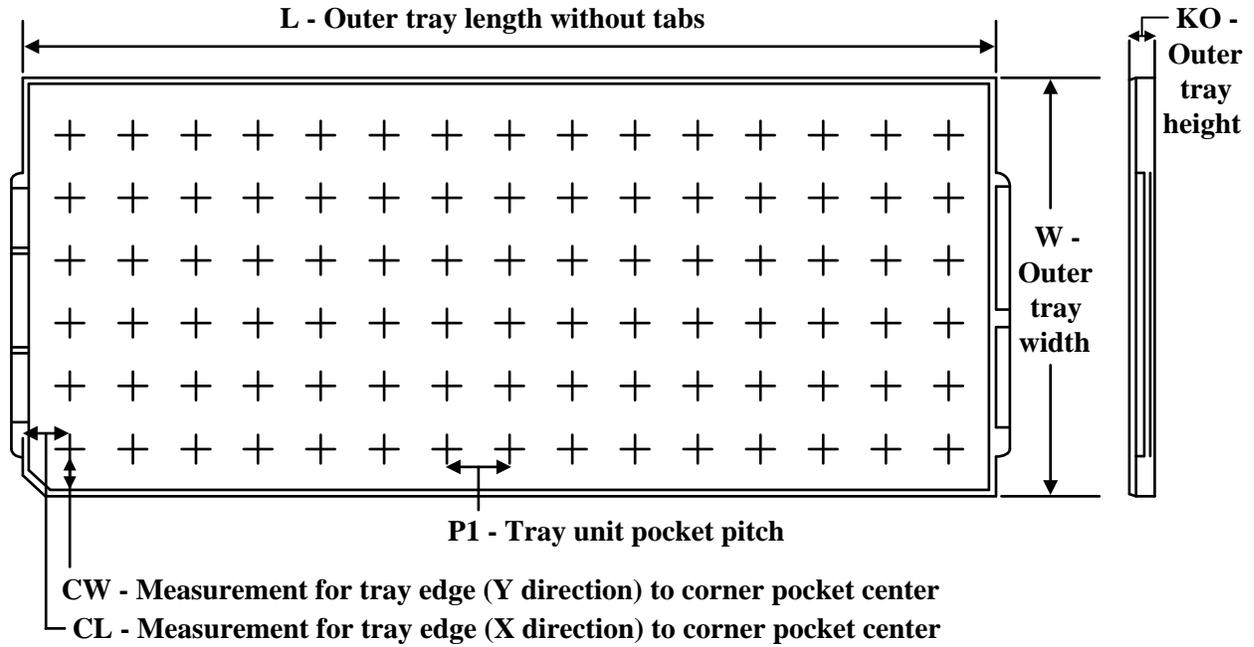
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TPS7H2201Y/EM	KGD	XCEPT	0	5	5 x 5	70	6.35	3.81	610	1.3	8.89	8.13
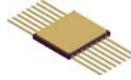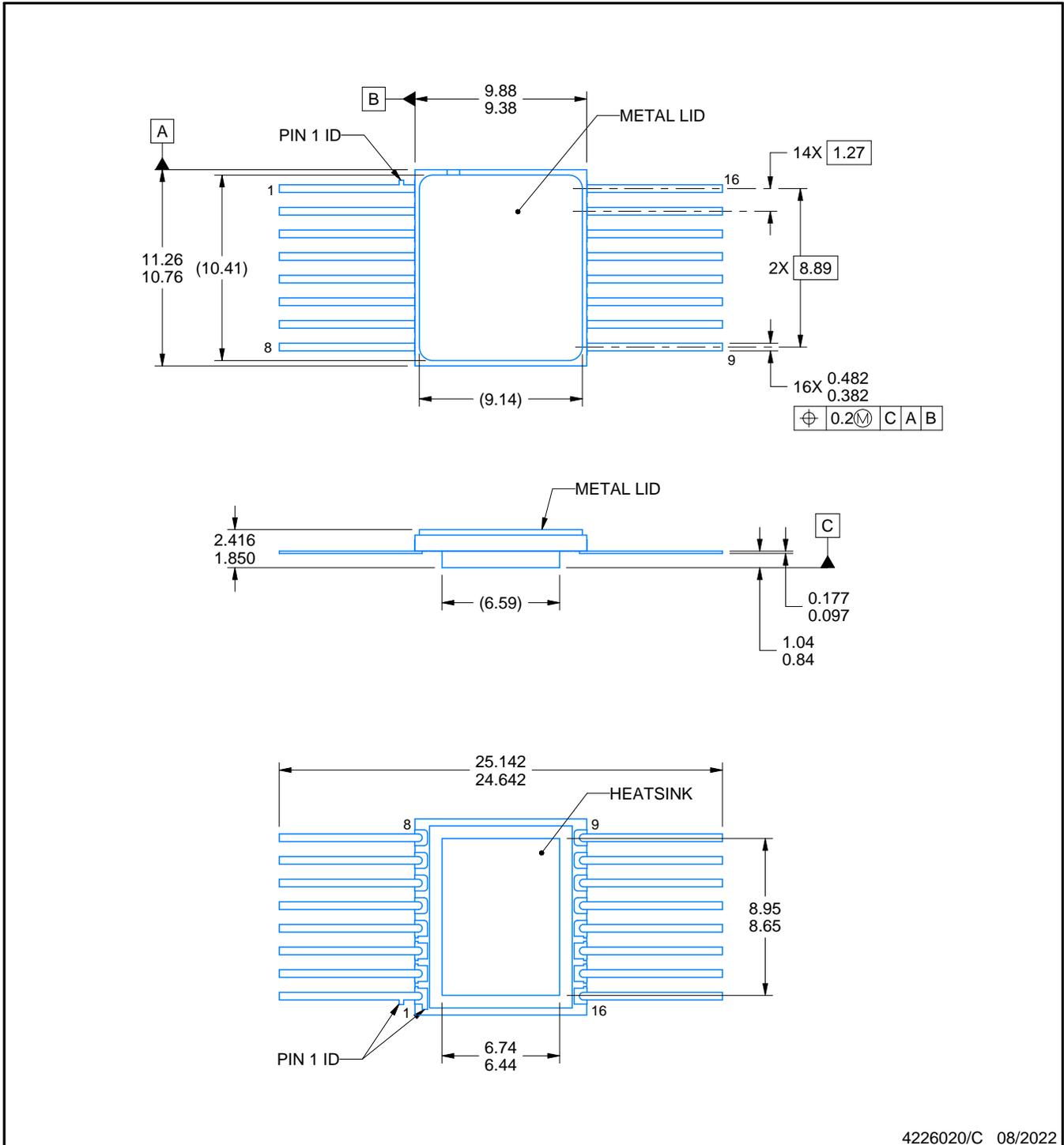
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink.
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.

(6.59)

(1.2) TYP

(0.6)

(1.2) TYP

(0.6)

(8.8)

PKG

PKG

(⌀ 0.2) TYP

(R0.05) TYP
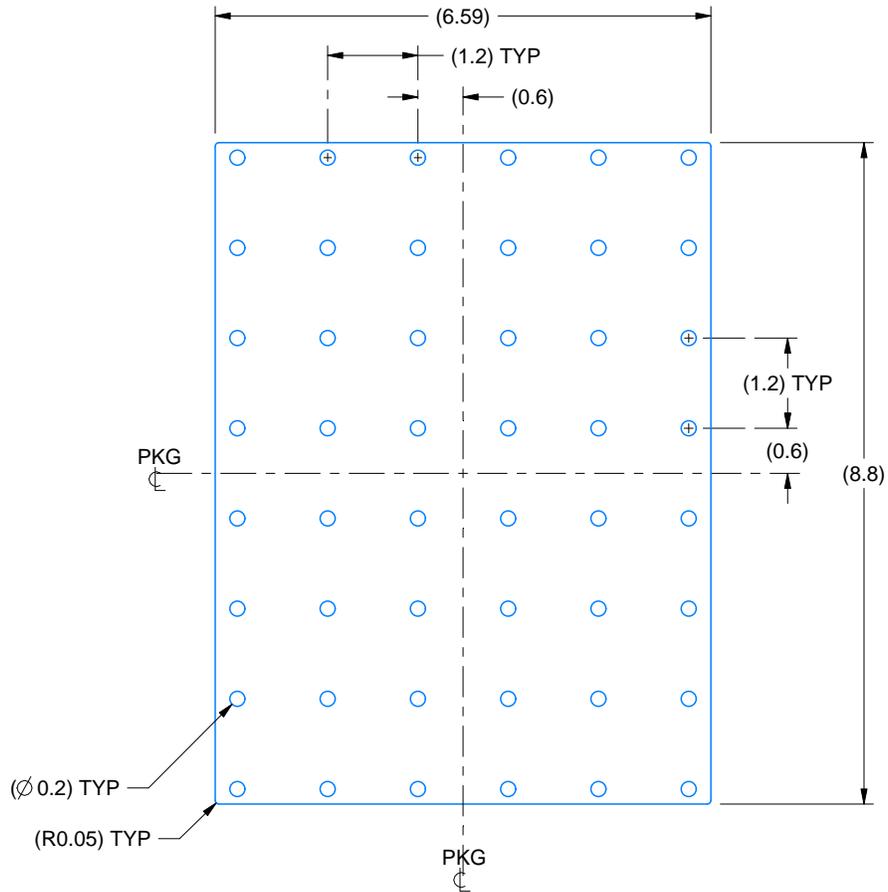
HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

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