

U\_B12  
B12.SchDoc

U\_B13  
B13.SchDoc

U\_B14  
B14.SchDoc

U\_B15  
B15.SchDoc

U\_B16  
B16.SchDoc

U\_B34  
B34.SchDoc

U\_FPGA-MGT  
FPGA-MGT.SchDoc

U\_FPGA-CFG  
FPGA-CFG.SchDoc

U\_FPGA-MISC  
FPGA-MISC.SchDoc

U\_FPGA-PWR  
FPGA-PWR.SchDoc

U\_PWR1  
PWR1.SchDoc

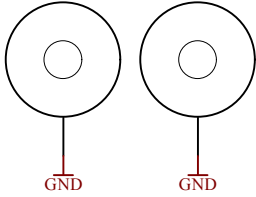
U\_PWR2  
PWR2.SchDoc

U\_Clock  
Clock.SchDoc

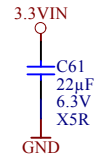
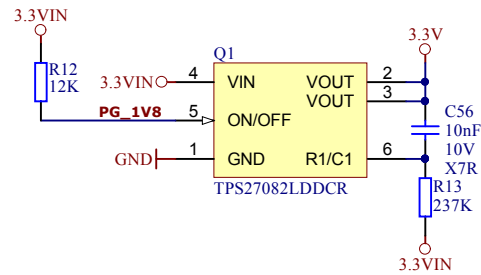
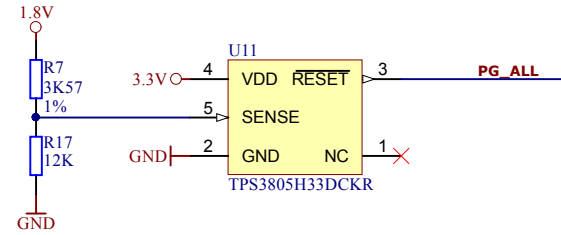
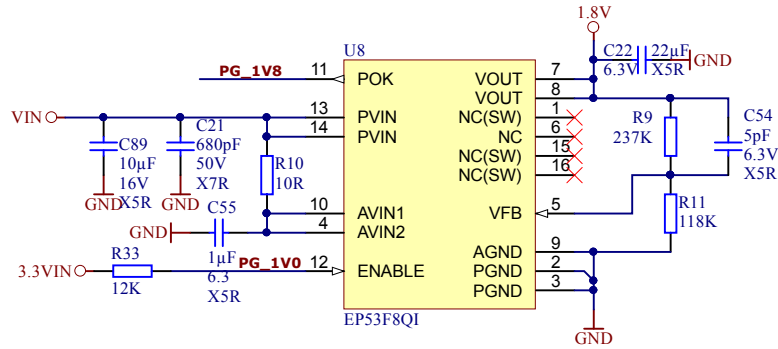
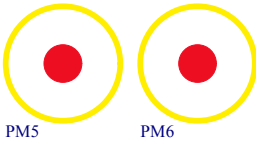
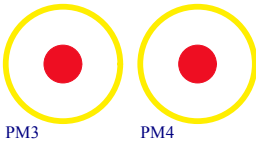
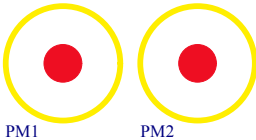
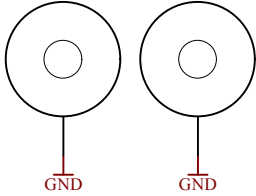
U\_B2B-Connectors  
B2B-Connectors.SchDoc

U\_B33  
B33.SchDoc

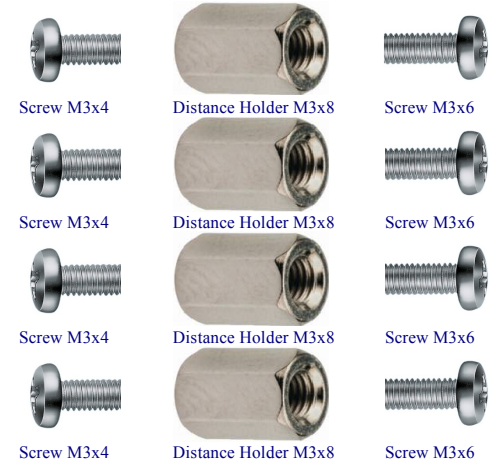
Mount.Hole 3.2mm    Mount.Hole 3.2mm



Mount.Hole 3.2mm    Mount.Hole 3.2mm



**Top of Board**

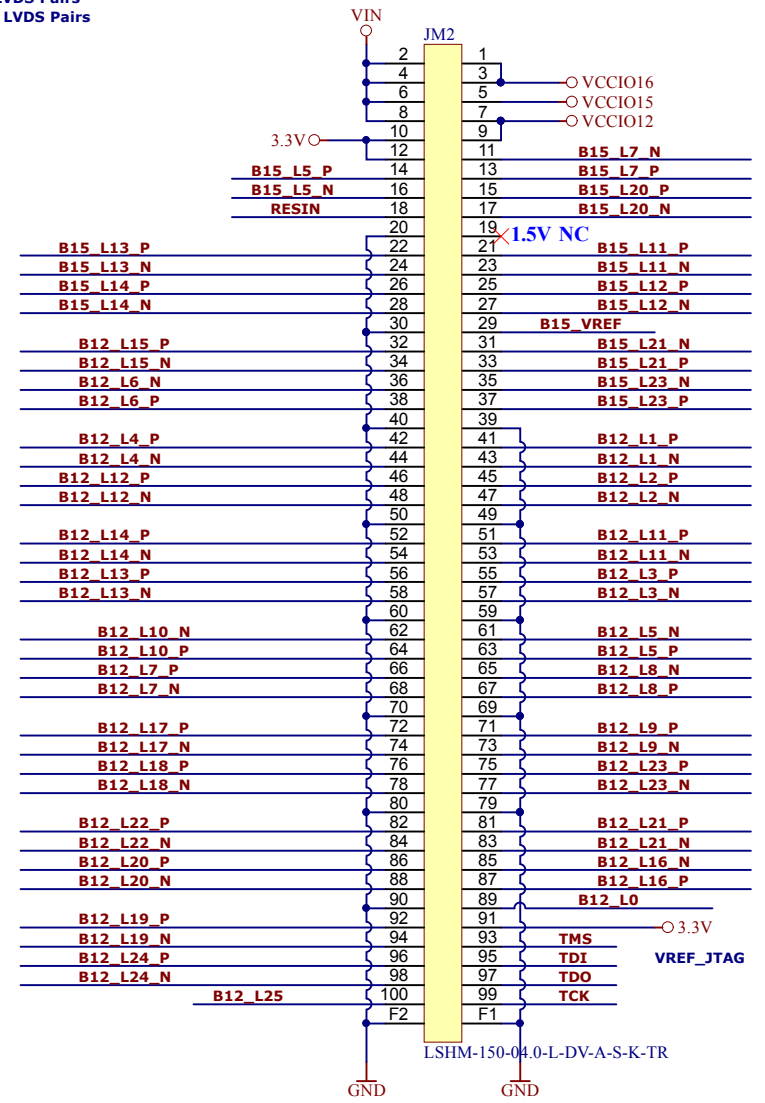
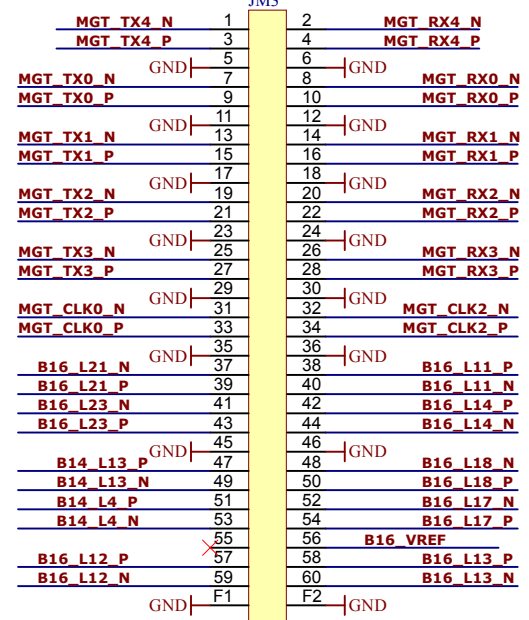
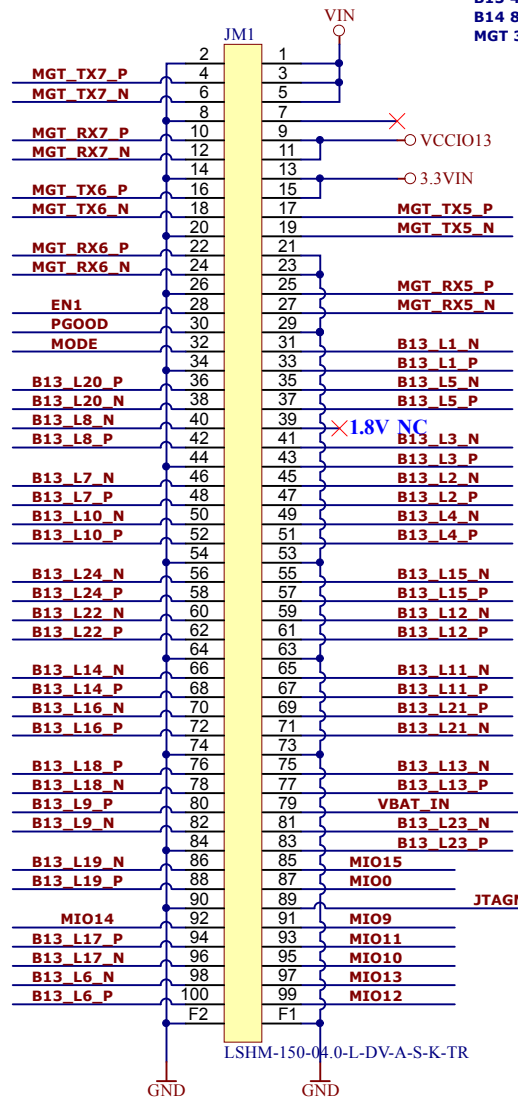


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**B13 48 IO, 24 LVDS Pairs**  
**B14 8 IO, 3.3V**  
**MGT 3 Lanes**

**B16 16 IO, 8 LVDS Pairs**  
**MGT 4 + 1 Lanes**  
**B14 4 IO, 3.3V**

**B15 18 IO, 9 LVDS Pairs**  
**B12 48 IO, 24 LVDS Pairs**  
**B12 2 IO**



TE0720 Compatibility

MIO0 8 pins => 8 IO B14  
 USB D+,D-, vbusen,otg\_id => 4 IO B14  
 SGMII => MGT  
 MIO1(SDCARD) => MGT  
 ETH MD1 => MGT  
 B34 => B16, MGT  
 B35 => B13  
 B13 => B12  
 B33 => B15

Clock Capable I/O  
 All pins named  
 Bxx\_H\_X  
 Bxx\_I\_X  
 Bxx\_O\_X  
 Bxx\_T\_X  
 Bxx\_V\_X  
 Bxx\_W\_X  
 Bxx\_X\_X  
 Bxx\_Y\_X  
 Bxx\_Z\_X  
 Are Clock Capable I/O's

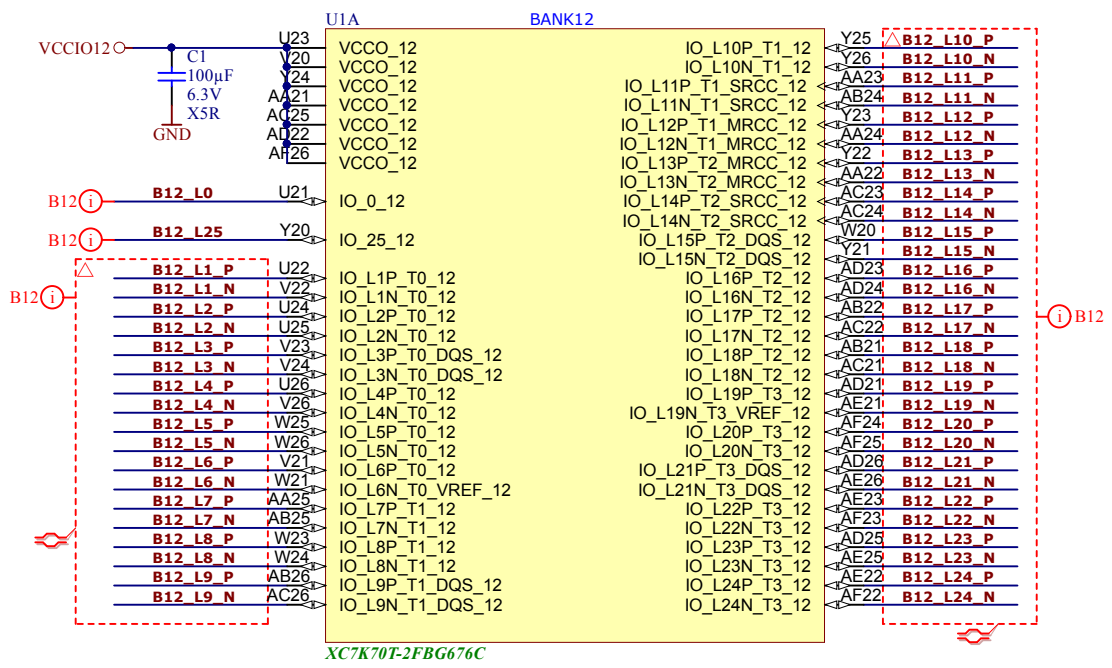


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B12\_FIXED (i) △

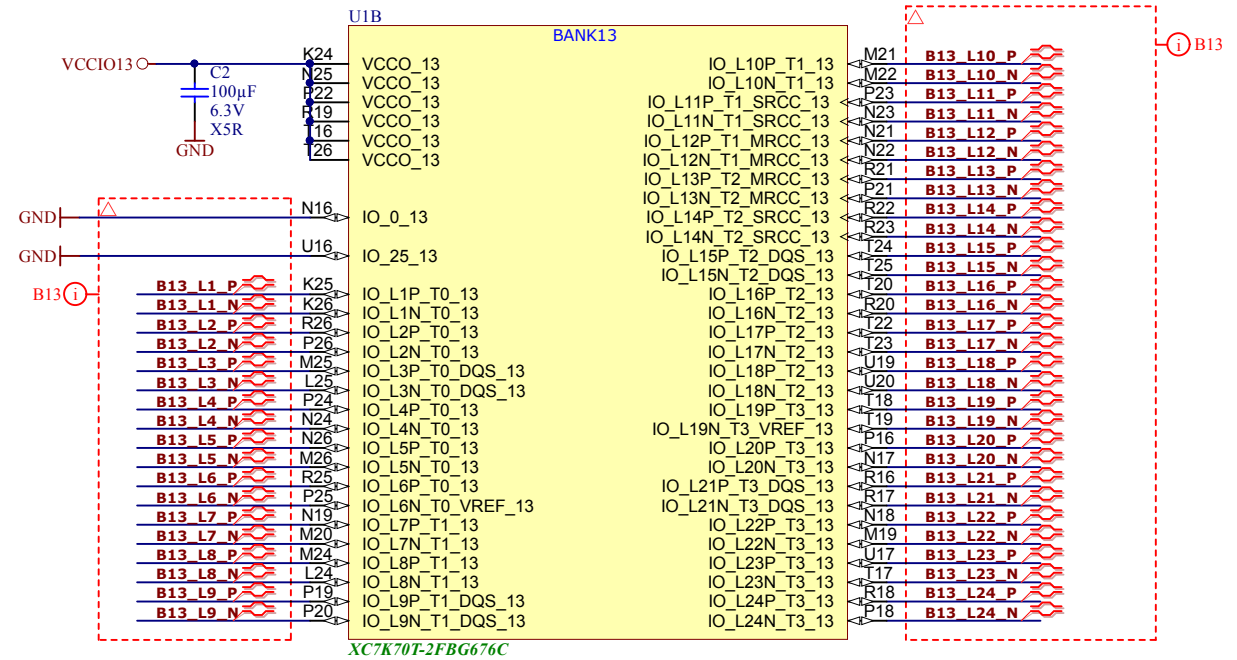
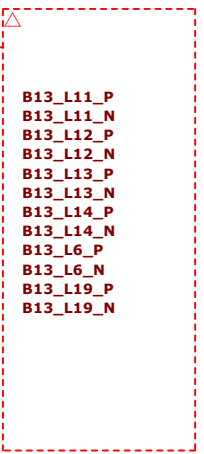
B12 L11 P
B12 L11 N
B12 L12 P
B12 L12 N
B12 L13 P
B12 L13 N
B12 L14 P
B12 L14 N
B12 L19 P
B12 L19 N
B12 L6 P
B12 L6 N

**K70T version does not have this bank!**



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B13\_FIXED



XC7K70T-2FBG676C



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1

2

3

4

A

A

B

B

C

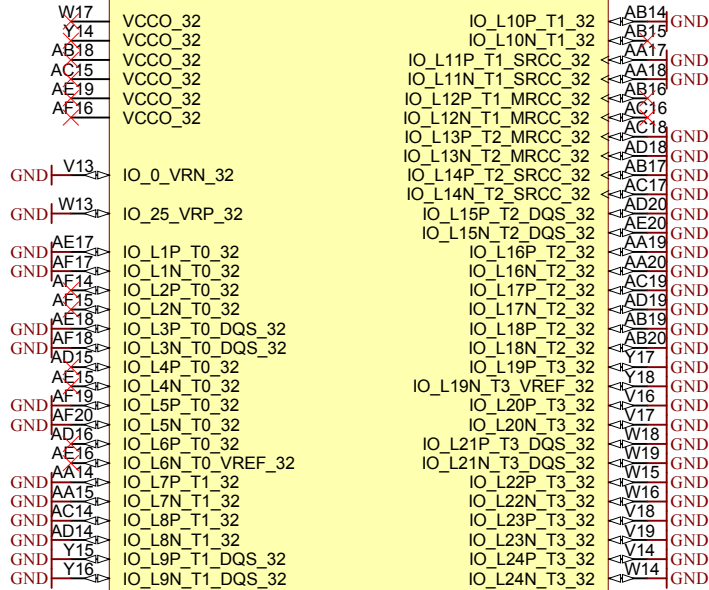
C

D

D

UIF

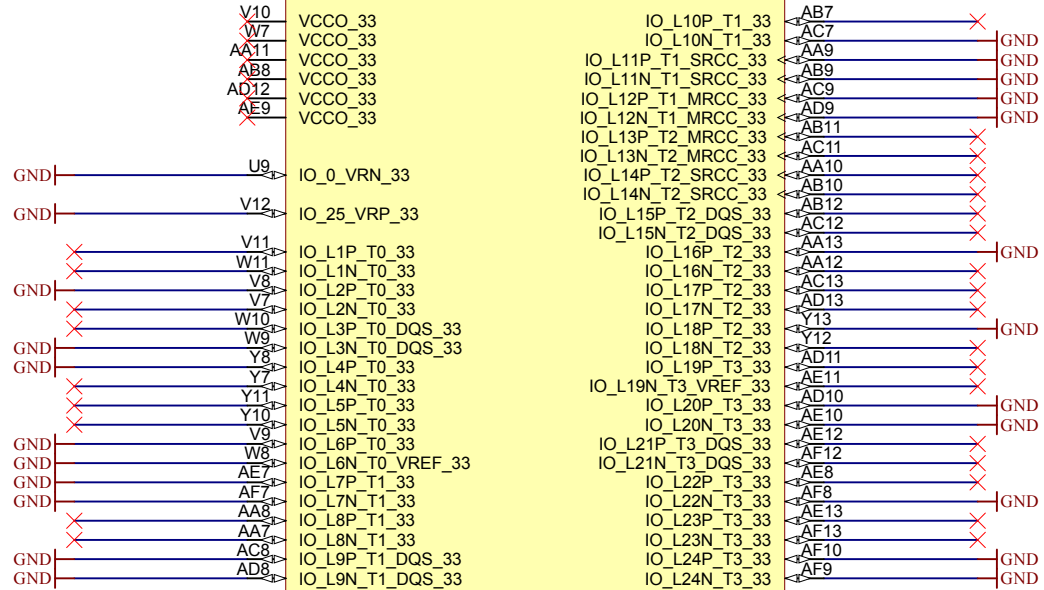
BANK32



XC7K70T-2FBG676C

UIG

BANK33



XC7K70T-2FBG676C



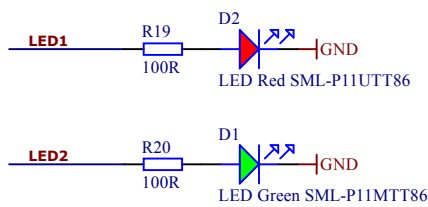
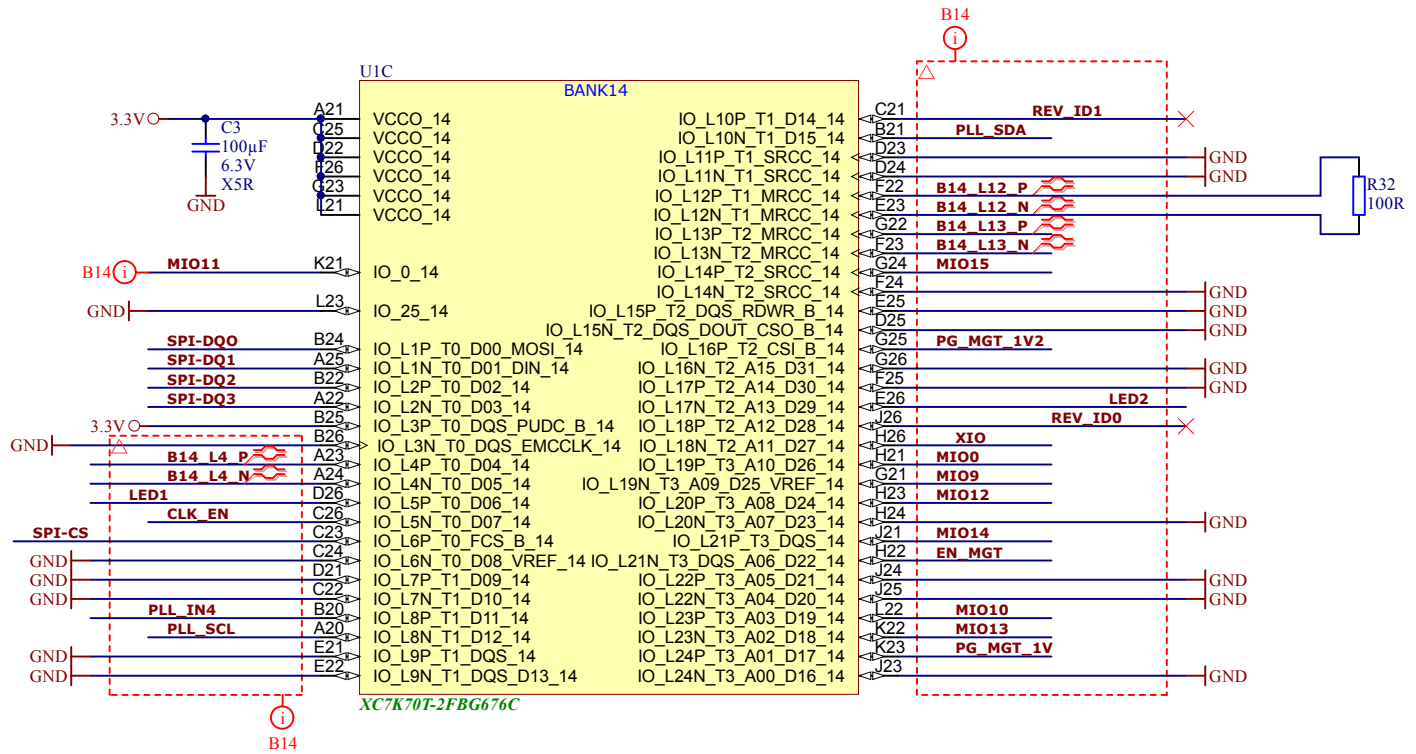
Title: TE0741		
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Filename: B33.SchDoc		

1

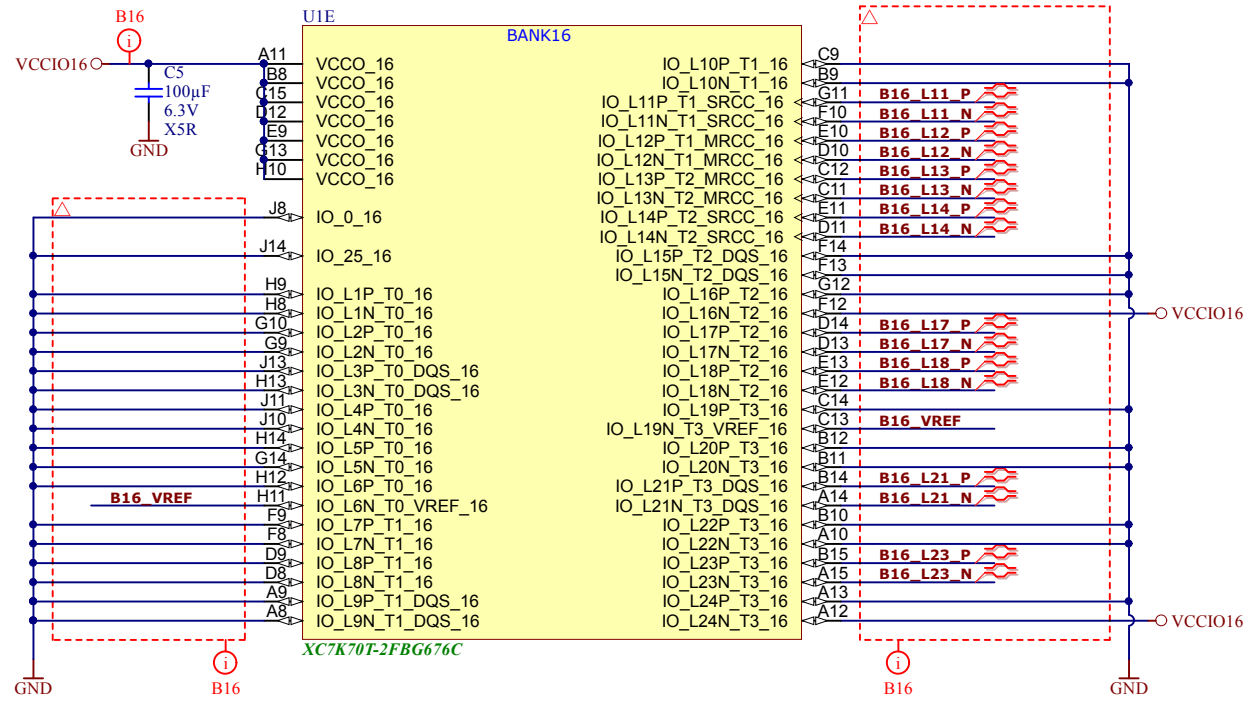
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3

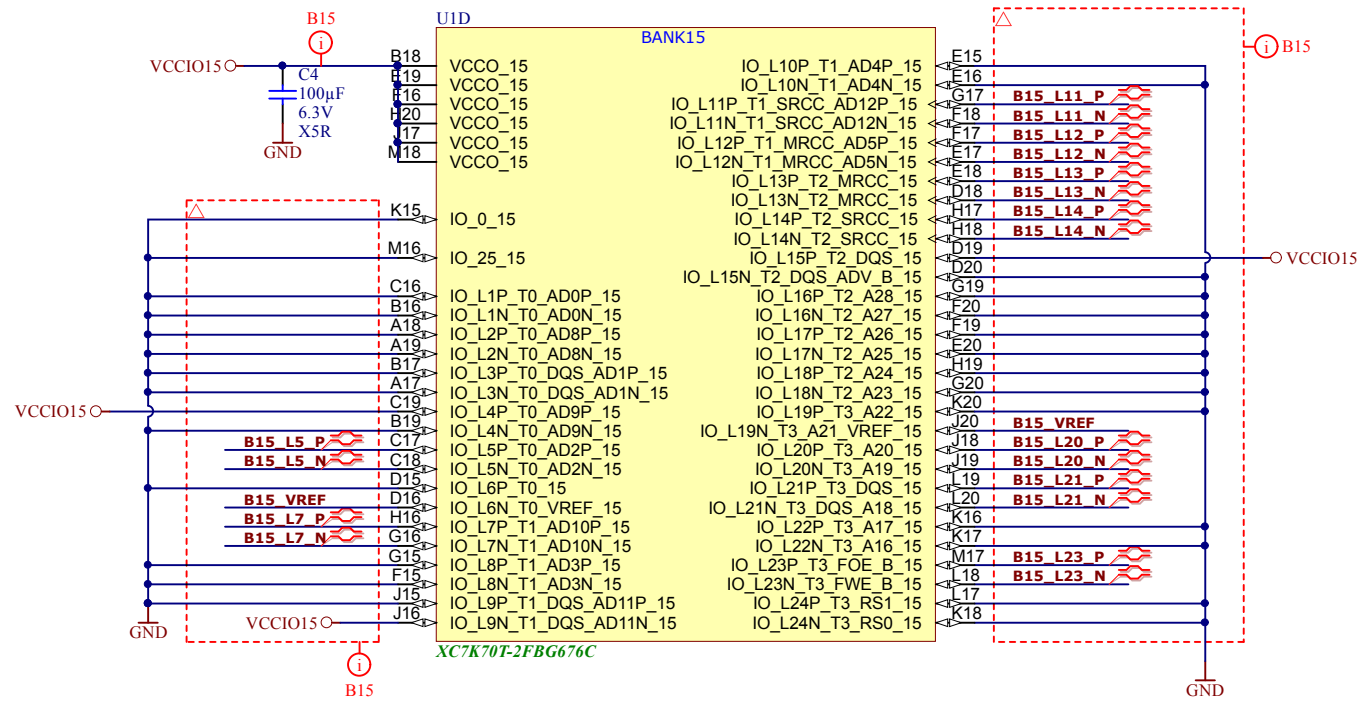
4



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		Title: TE0741	
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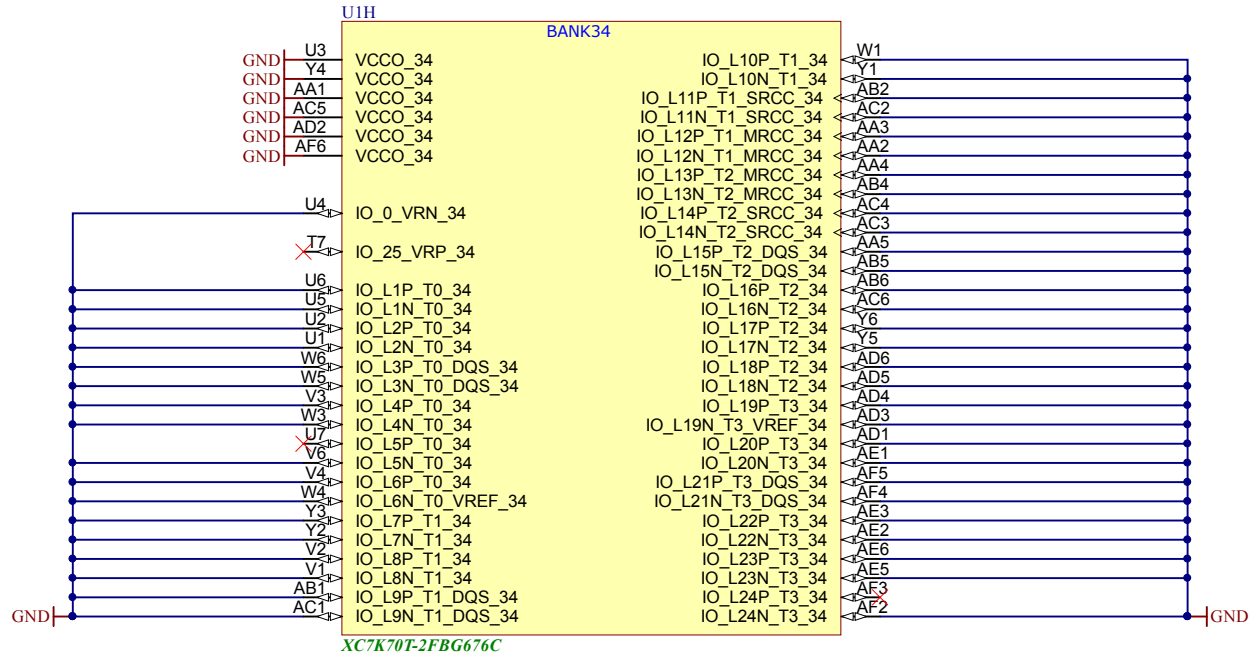



XC7K70T-2FBG676C

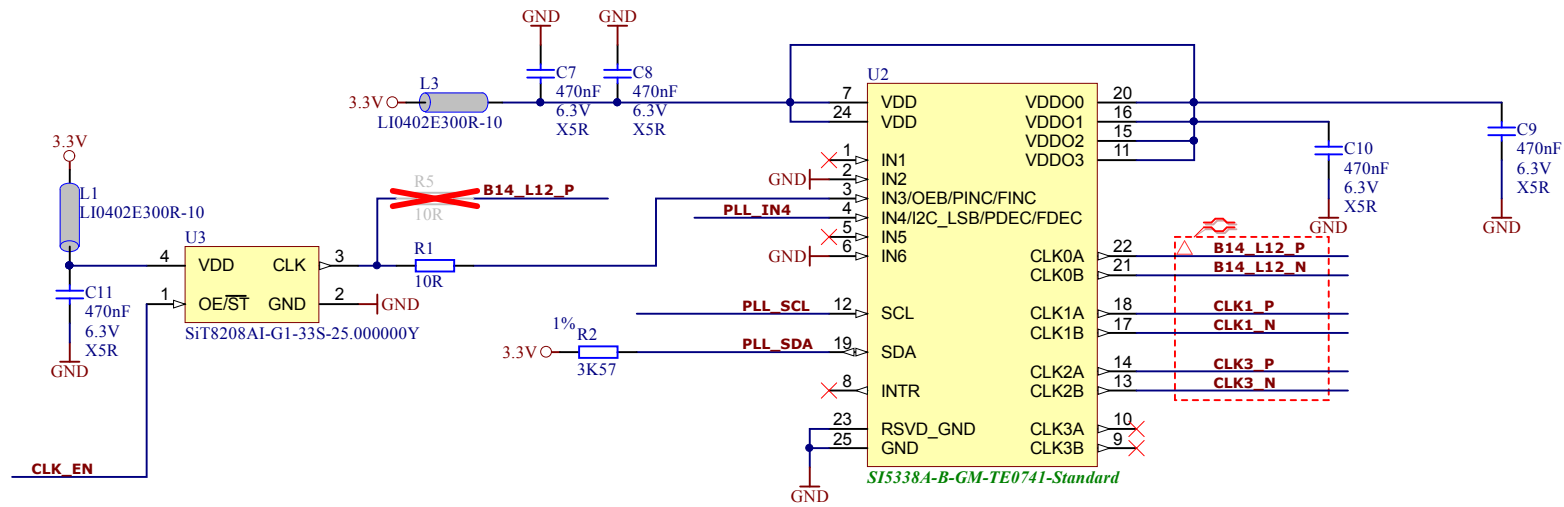



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A4	Number: TE0741 TE0741-070-2CF	Rev. 02
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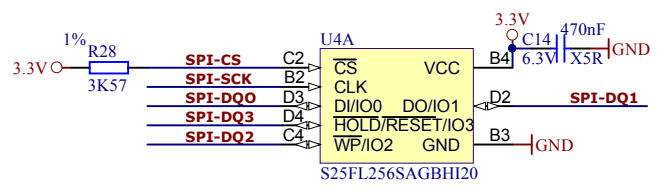
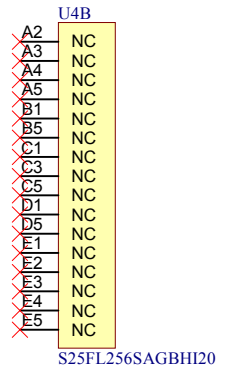
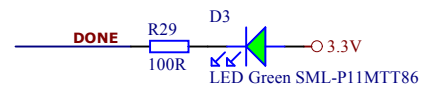
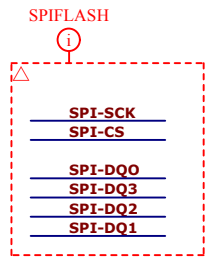
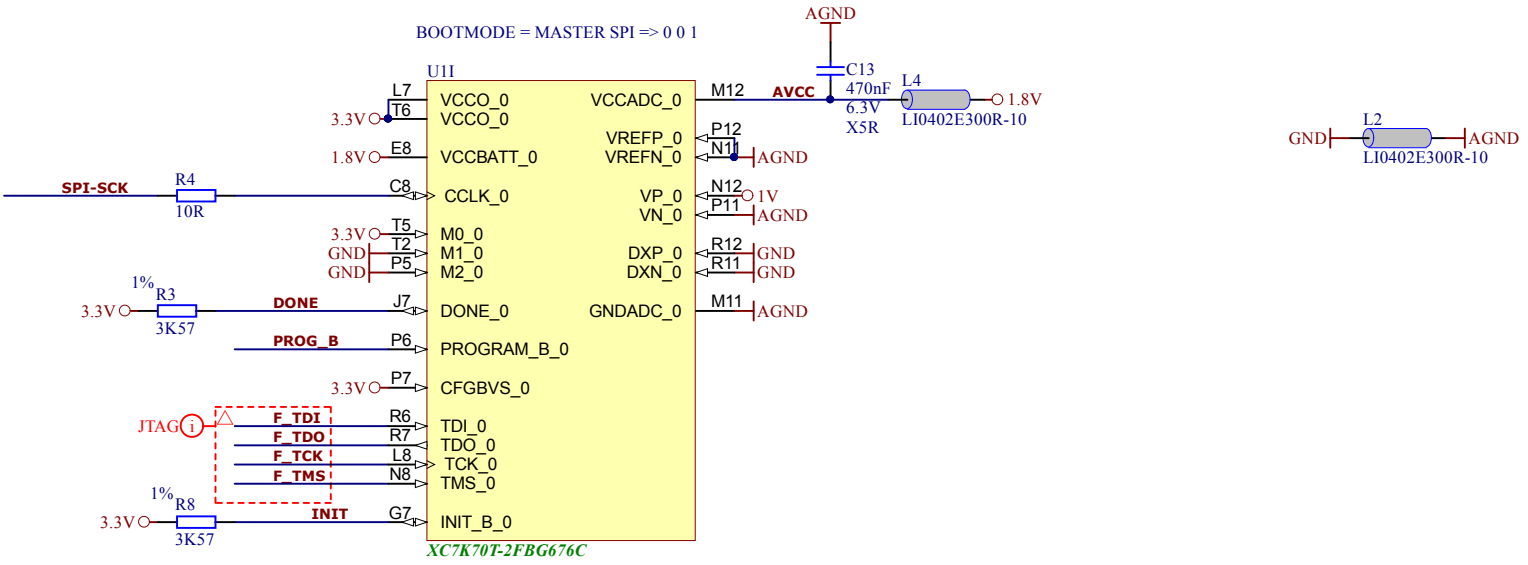



Title: <b>TE0741</b>		
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Filename: <b>B34.SchDoc</b>		

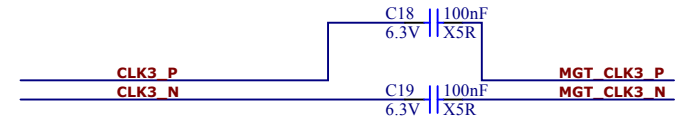
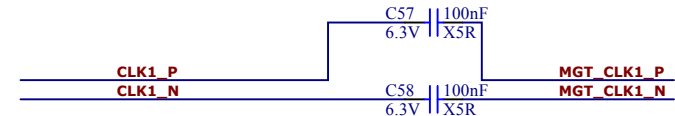
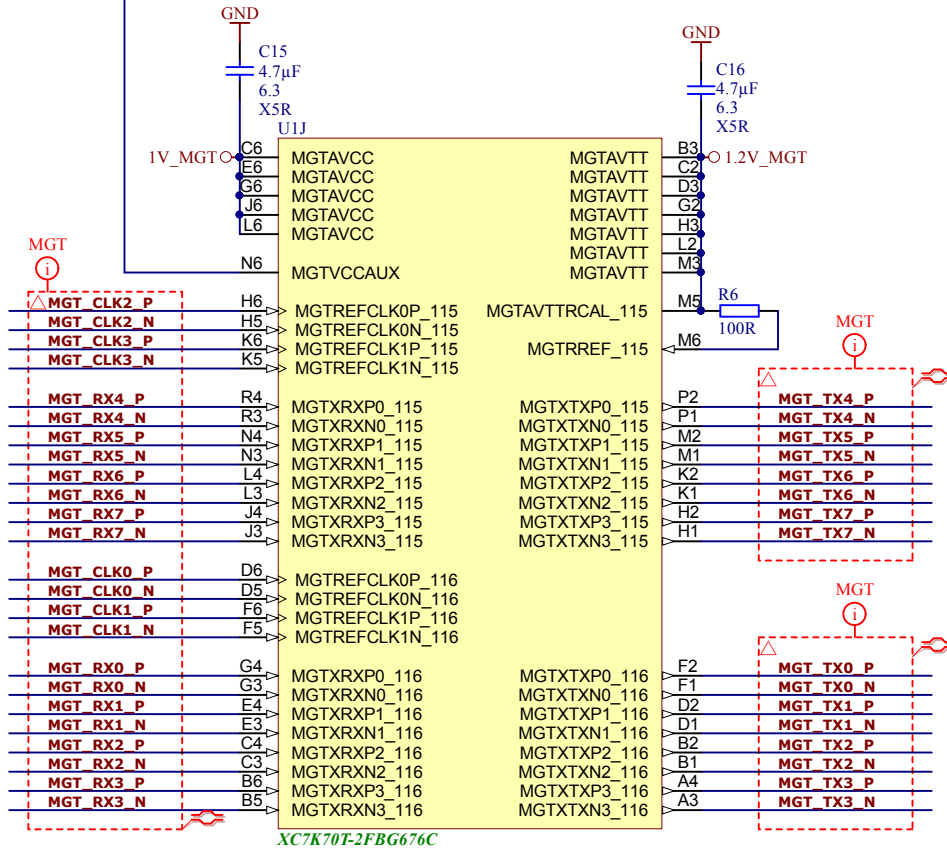
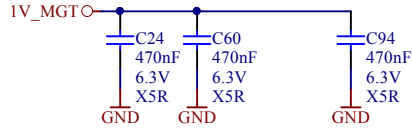
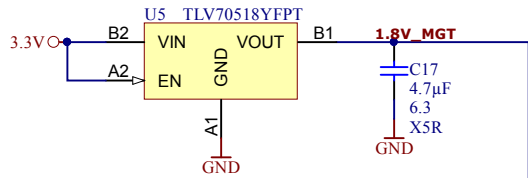



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Filename: Clock.SchDoc		Page9 of 15	

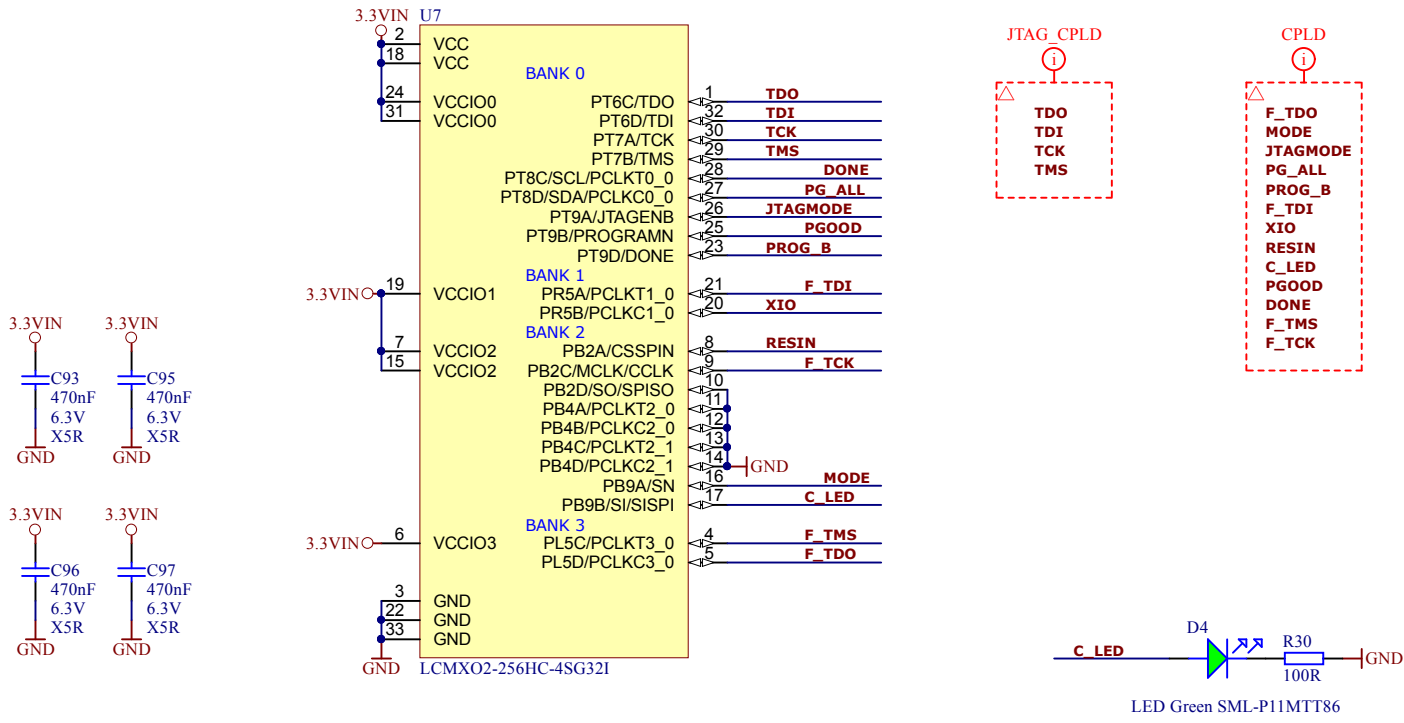
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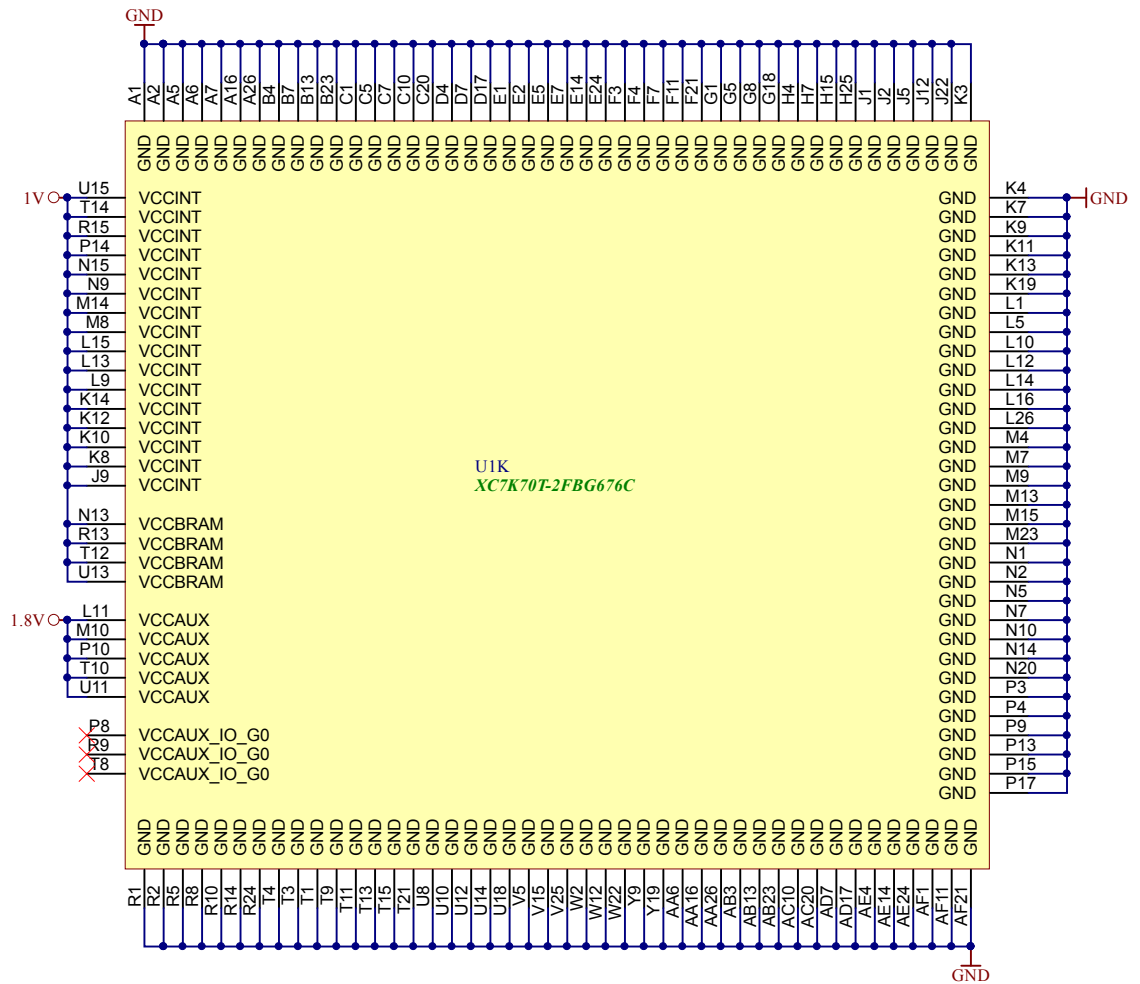
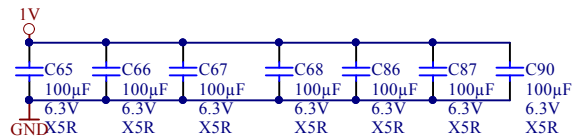
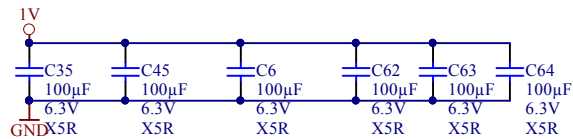
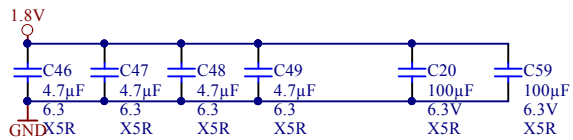
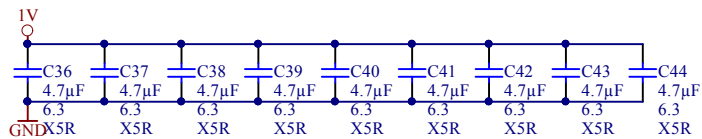
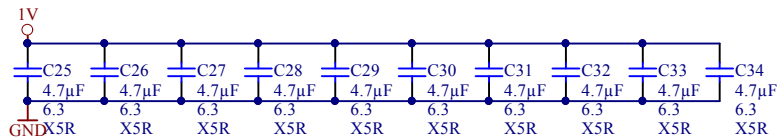
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A4	Number: TE0741 TE0741-070-2CF	Rev. 02
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Filename: FPGA-CFG.SchDoc		

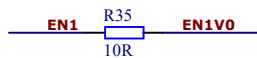
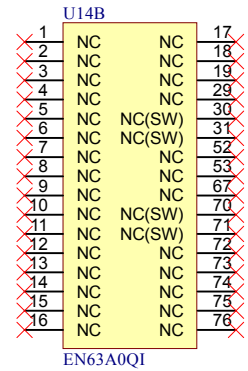
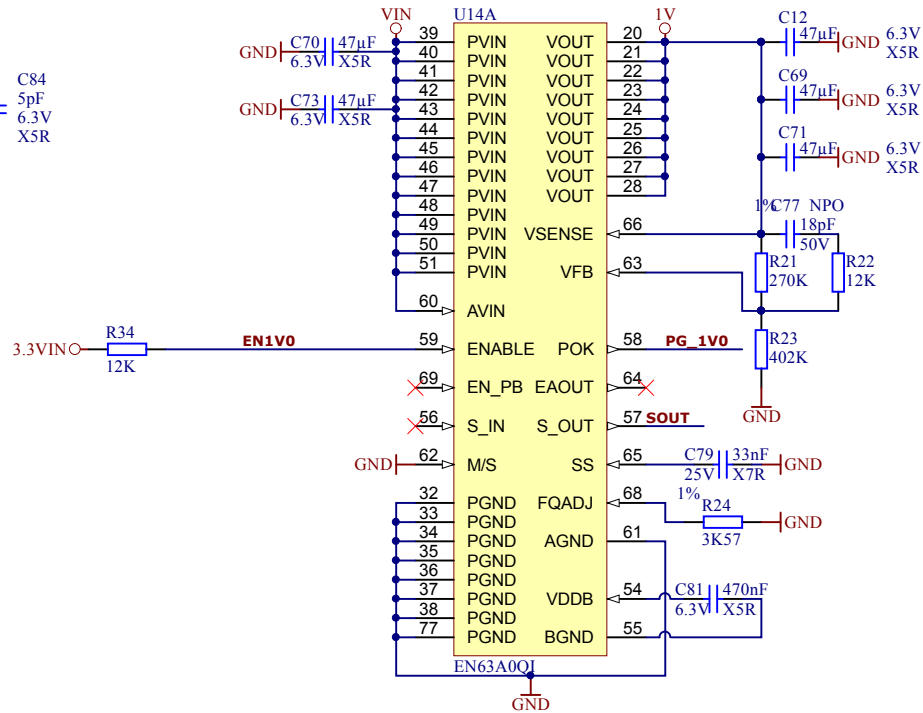
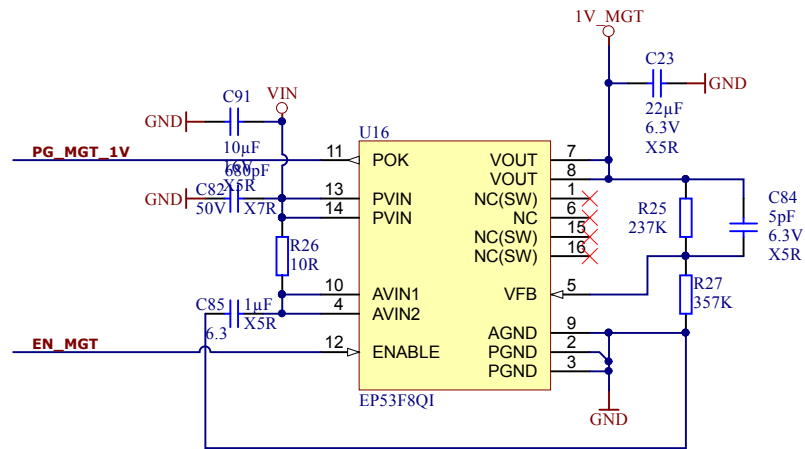
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Filename: FPGA-MGT.SchDoc		



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A4	Number: TE0741 TE0741-070-2CF	Rev. 02
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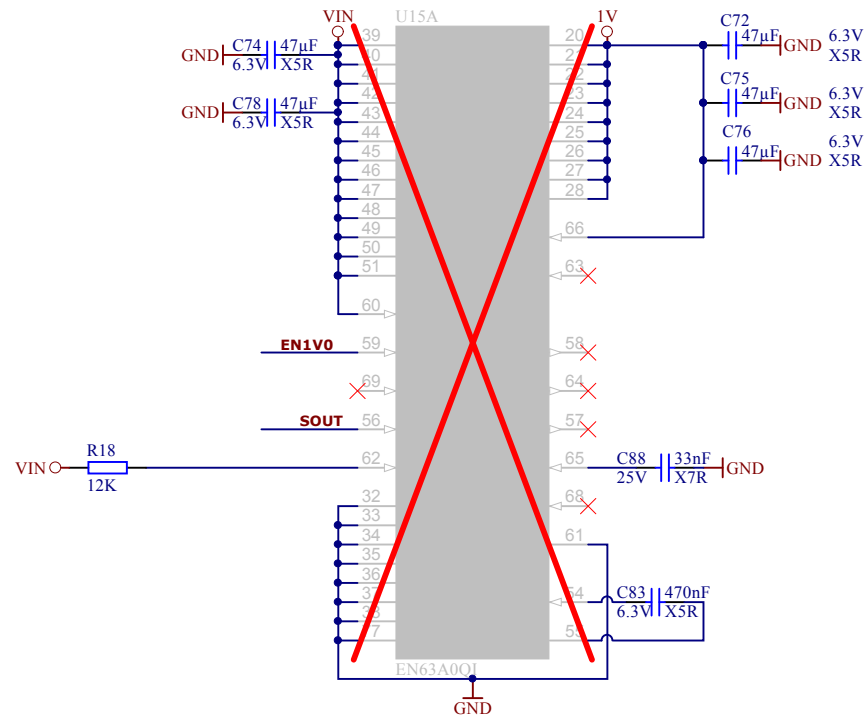
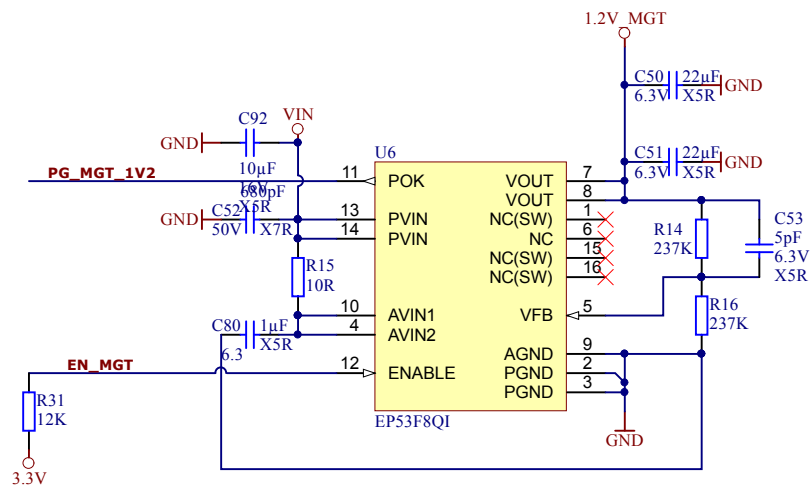
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A4	Number: TE0741 TE0741-070-2CF	Rev. 02
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Filename: FPGA-PWR.SchDoc		




Not mount if baseboard EN1 circuit cause problems



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	Title: TE0741		
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	Filename: PWR2.SchDoc		