

TPS652510 Buck Converter Evaluation Module User's Guide



ABSTRACT

This document presents the information required to power the TPS652510 PMIC as well as the support documentation including schematic and bill of materials.

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Trademarks

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1 Background and EVM Limitations

The TPS652510 PMIC is designed to provide 3, 2 and 2 A continuous outputs with an operational range of 4.5 to 16V and an externally set switching frequency ranging from 300kHz to 2.2MHz, with automatic PFM/PWM operation. When the PMIC is not fully loaded, buck1 can be loaded to 3.5A and buck 2 and 3 to 2.5A.

As there are many possible options to set the converters, table 1 presents the performance specification summary for the EVM.

Table 1-1. Input Voltage and Output Current Summary

Evaluation Module	Test Conditions	Output Current Range
TPS652510EVM	$V_{in} = 4.5 \text{ V to } 15 \text{ V}$ $F_{sw} = 500 \text{ KHz}$	Buck1, 1.2 V, 3A Buck2, 1.8 V, 3A Buck3, 3.3 V, 3A (25°C ambient)

This evaluation module is designed to provide access to the features of the TPS652510. Some modifications can be made to this module to test performance at different input and output voltages, current and frequency operation. Please contact TI Field Applications Group for advice on these matters.

2 Power-up Procedure

1. Define which converters are to be enabled or disabled by connecting jumpers to JP3, JP11 and JP20 accordingly, or to wiring external drive signals to the ENx headers.
2. If PGOOD signal is required connect JP27 or wire the PGOOD pin to a pull-up supply
3. Connect loads to the output connectors.
4. Apply a DC voltage to header J3. Polarity is marked on the silk-screen.
5. Converters will start according to the setting on JP3, JP11 and JP20. Check the outputs

3 TPS652510EVM Schematic

The resistor and capacitor values have been chosen according to the guidelines presented on the TPS652510 spec that will be available at

<http://focus.ti.com/docs/prod/folders/print/TPS652510.html>

Note that for the purpose of gains-phase measurements R14, R17 and R37 (zero ohm on the EVM) need to be replaced by suitable low value resistors as per the network analyzer setup required. Test points connections are provided on either end of the resistors to allow for easy measurement.

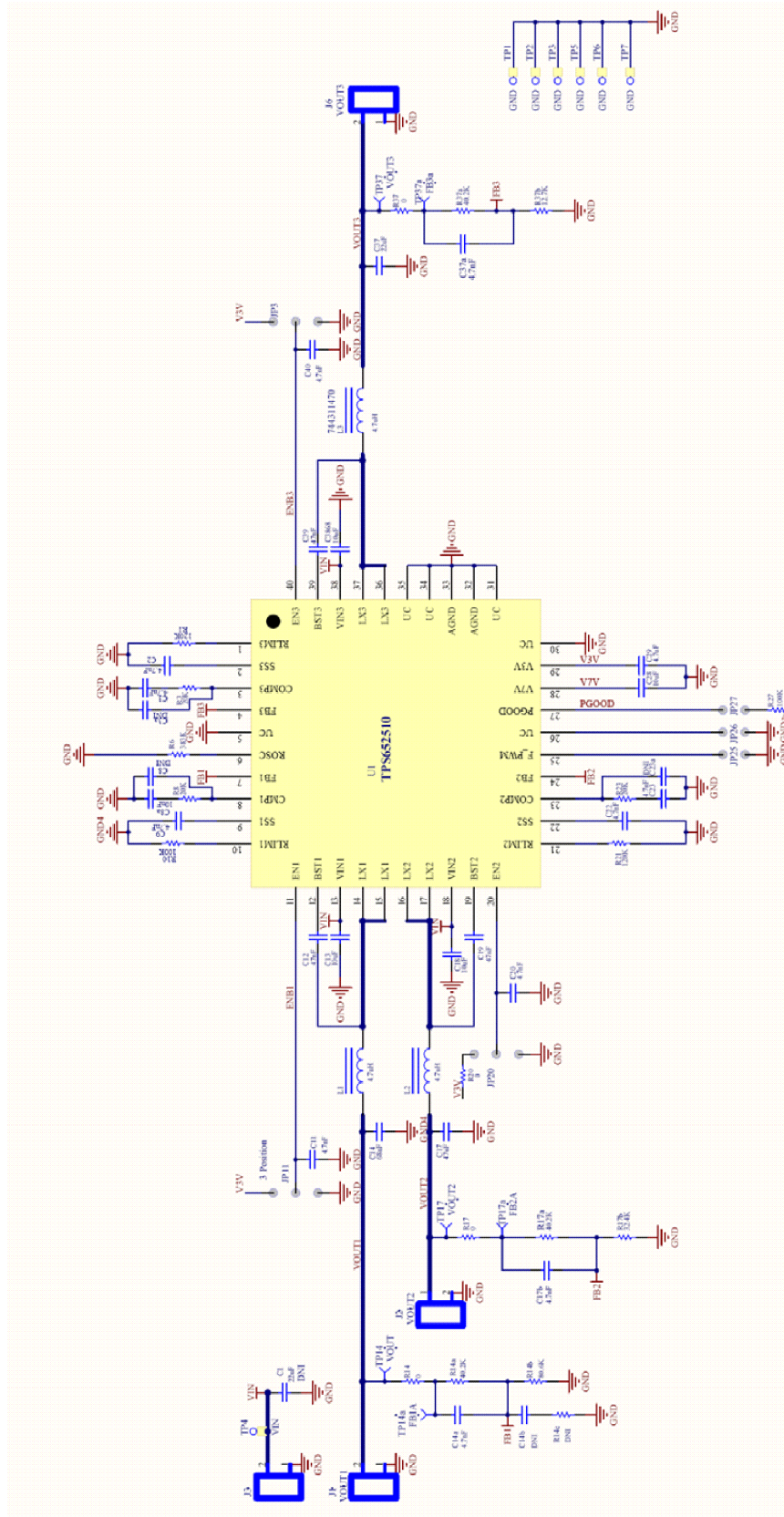
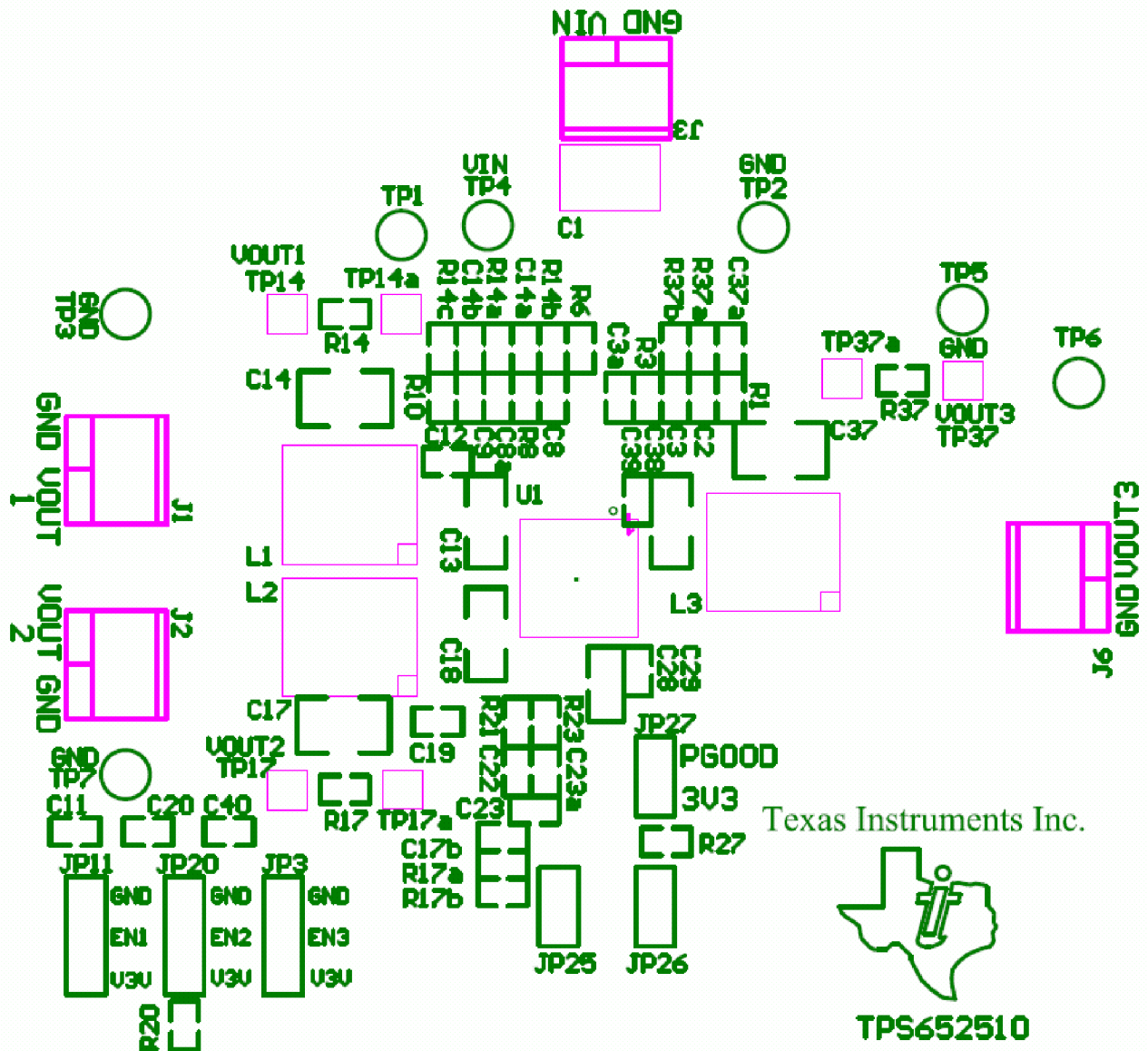


Figure 3-1. TPS652510EVM Schematic



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TPS652510

Figure 3-2. Composite Layer

4 EVM Layout

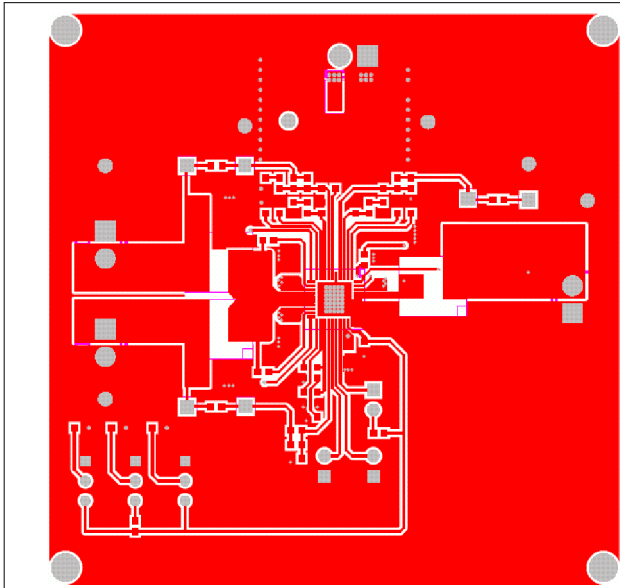


Figure 4-1. Top Layer

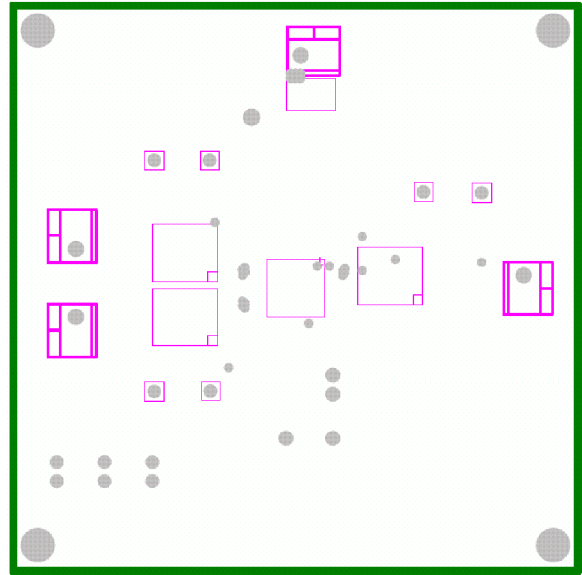


Figure 4-2. Middle Layer (2nd), Solid Cu Ground

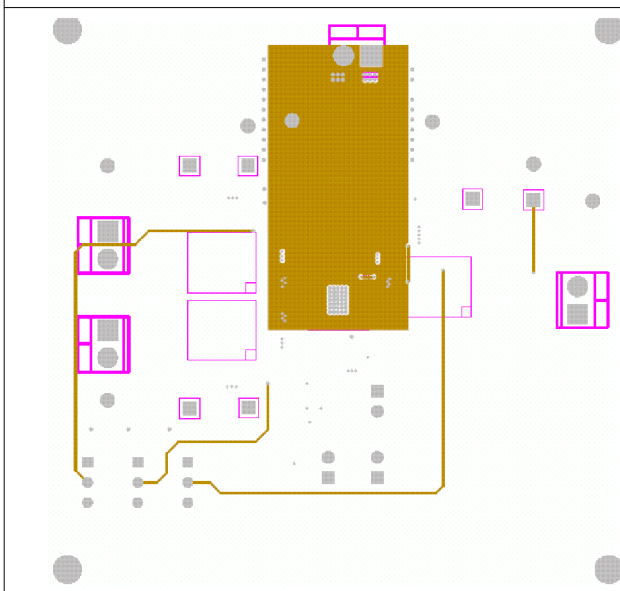


Figure 4-3. Middle (3rd) Layer

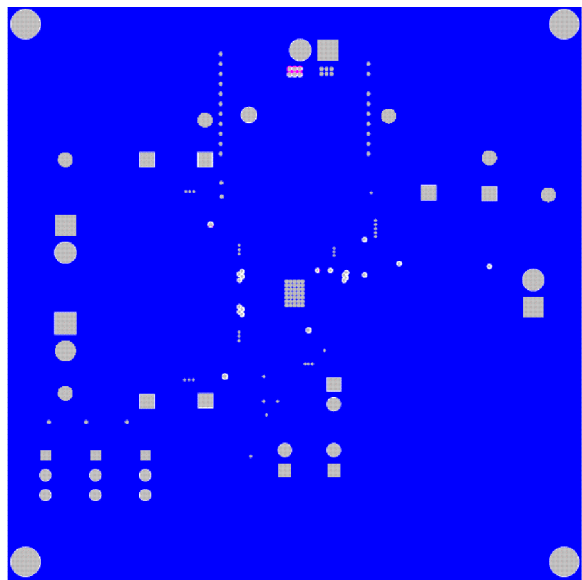
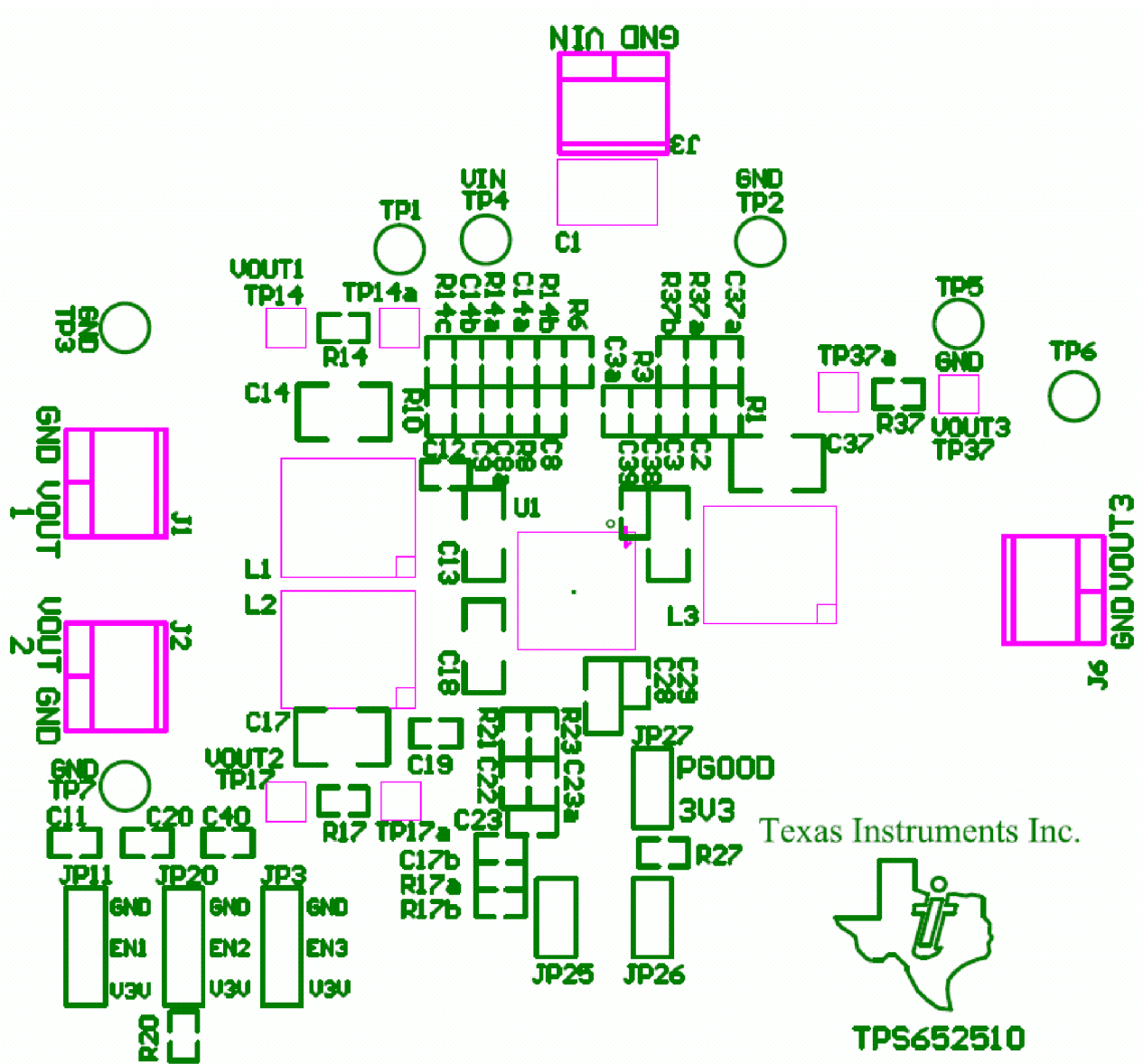


Figure 4-4. Bottom Layer

5 Bench Test Setup Conditions

Headers description and jumper placement.



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5.1 Headers Description

Header Number	Function	LOC	Placement	Comment
JP11	BUCK1 enable (EN1)	SW	For immediate start-up fit jumper to V3V For sequencing do not fit jumper To disable converter fit jumper to GND	Fit according to test requirement
JP20	BUCK2 enable (EN2)	SW	For immediate start-up fit jumper to V3V For sequencing do not fit jumper To disable converter fit jumper to GND	Fit according to test requirement
JP3	BUCK3 enable (EN3)	SW	For immediate start-up fit jumper to V3V For sequencing do not fit jumper To disable converter fit jumper to GND	Fit according to test requirement
JP25	Forced PWM (F_PWM)	S	For forced PWM operation fit jumper to V3V For automatic PFM/PWM operation fit jumper to GND	Do not leave this header open. Use a jumper to set either forced PWM mode or automatic PFM/PWM mode
JP26	Test	S	Used for test purposes	Jumper must be fitted
JP27	PGOOD	S	PGOOD indicated pulled to 3V3	Fit according to test requirement

5.2 Test Points and Placement

Buck converter outputs are white and have a label for easy location. Close to any of these test points there are black ground test points to allow for DVM measurement or to use a metal exposed scope probe to reduce common mode noise measurements. All test points are described in the following table:

Test Point	Name	Signal	COLOR	Comment
TP1	GND	GND	Black	
TP2	GND	GND	Black	
TP3	GND	GND	Black	
TP4	Vin	Vin	Black	
TP5	GND	GND	Black	
TP6	GND	GND	Black	
TP7	GND	GND	Black	
TP14	Vout1	Output voltage Buck1	Not fitted	
TP14a		Injection Point gain-phase measurement buck1	Not fitted	Normally not used
TP17	Vout1	Output voltage Buck2	Not fitted	
TP17a		Injection Point gain-phase measurement buck2	Not fitted	Normally not used
TP37	Vout1	Output voltage Buck3	Not fitted	
TP37a		Injection Point gain-phase measurement buck3	Not fitted	Normally not used

Table 5-1. Bill of Materials⁽¹⁾

Count	RefDes	Value	Description	Size
1	C1	22 μ F	CAP CERAMIC 22UF 25V X5R 1210	1812
11	C2, C3, C9, C11, C14a, C17b, C20, C22, C23, C37a, C40	4.7 nF	CAP 4700PF 50V CERAMIC X7R 0603	0603
1	C8a	10 nF		0603
3	C3a, C8, C23a	DNI	CAP 10000PF 50V CERAMIC X7R 0603	0603
3	C12, C19, C39	47 nF	CAP 47000PF 25V CERM X7R 0603	0603
3	C13, C18, C38	10 μ F	CAP CERAMIC 10UF 25V X5R 1206	1206
1	C14	68 μ F	CAP CERAMIC 22UF 25V X5R 1210	1210
1	C17	47 μ F	CAP CERAMIC 22UF 25V X5R 1210	1210
1	C37	22 μ F	CAP CERAMIC 22UF 25V X5R 1210	1210
5	C28, C30, C31, C32, C33	10 μ F	CAP CER 10UF 10V X7R 0805	0805
1	C29	4.7 μ F	CAP CER 4.7UF 10V X5R 0603	0603
1	J1, J2, J3, J6	ED55/2DS	TERMINAL BLOCK 3.5MM 2POS PCB	TB_2X3.5MM
2	J4	ED55/3DS	TERMINAL BLOCK 3.5MM 2POS PCB	TB_3X3.5MM
6	JP3, JP5, JP11, JP20, JP25, JP34		CONN HEADER 50POS .100" SGL GOLD	JMP0.3
3	JP26, JP27, JP35 1		CONN HEADER 50POS .100" SGL GOLD	JMP0.2
3	L1, L2, L3	4.7 μ H	Magnetic-Core Inductor	IND_RLF7030
2	R1, R21	120 K	RES 120K OHM 1/10W 5% 0603 SMD	0603
1	R2	10 K	RES 10K OHM 1/10W 5% 0603 SMD	0603
3	R3, R8, R23	20 K	RES 20K OHM 1/10W 5% 0603 SMD	0603
1	R6	383 K	RES 383K OHM 1/10W 1% 0603 SMD	0603
4	R10, R26, R27, R35	100 K	RES 100K OHM 1/10W 5% 0603 SMD	0603
4	R14, R17, R20, R37	0	RES 0.0 OHM 1/10W 5% 0603 SMD	0603
3	R14a, R17a, R37a	40.2 K	RES 40.2K OHM 1/10W 1% 0603 SMD	0603
1	R14b	80.6 K	RES 80.6K OHM 1/10W 1% 0603 SMD	0603
1	R17b	32.4 K	RES 32.4K OHM 1/10W 1% 0603 SMD	0603
1	R37b	12.7 k	RES 12.7K OHM 1/10W 1% 0603 SMD	0603
6	TP1, TP2, TP3, TP5, TP6, TP7		Glass Beaded Test Point	TEST POINT 0.052
1	TP4	STD	Glass Beaded Test Point	TEST POINT 0.052
1	TP14	STD	Test Point, 0.032 Hole	TP-032
1	TP14a	STD	Test Point, 0.032 Hole	TP-032
1	TP17	STD	Test Point, 0.032 Hole	TP-032
1	TP17a		Test Point, 0.032 Hole	TP-032
4	TP30, TP31, TP32, TP33	STD	Glass Beaded Test Point	TEST POINT 0.052
1	TP37	STD	Test Point, 0.032 Hole	TP-032
1	TP37a		Test Point, 0.032 Hole	TP-032
1	U1		TPS652510	QFN-40

(1) Items with gray backgrounds are optional/not needed for a reference design.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2011) to Revision A (May 2021)

Page

- Updated user's guide title..... 2
- Updated the numbering format for tables, figures, and cross-references throughout the document. 2

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