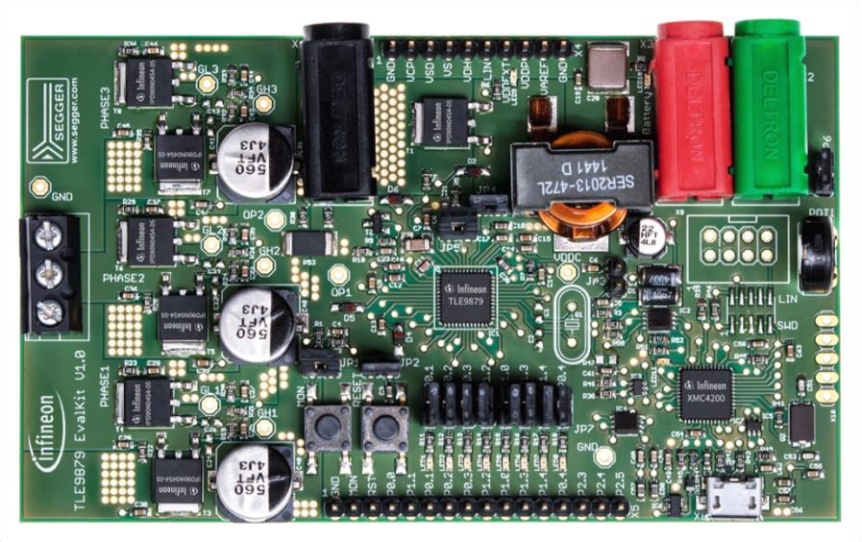
TLE9879 EvalKit V1.4 User Manual



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1 Abbreviations

BLDC	Brushless Direct Current
BSL	Bootstrap Loader
GH1,2,3	Gate High side MOSFET for Phases 1, 2, 3
GL1,2,3	Gate Low side MOSFET for Phase 1, 2, 3
GPIO	General Purpose Input / Output
ISP	In-system Programmer
LIN	Local Interconnect Network
MON	Monitor
n.c.	not connected
n/u	not used
OP1	Negative operational Amplifier Input
OP2	Positive operational Amplifier Input
RST	Reset
SL	Source Low side MOSFETs
SWD	Arm® Serial Wire Debug
TMS	Test Mode Select
UART	Universal Asynchronous Receiver Transmitter
VAREF	Reference Voltage
VBAT	Battery Voltage Supply
VCOM	Virtual COM-Port
VCP	Voltage Charge Pump
VDDC	Core Supply
VDDEXT	External Voltage Supply Output
VDDP	I/O Port Supply
VDH	Voltage Drain High side MOSFET
VS	Battery Supply Input
VSD	Battery Supply Input for MOSFET Driver

Table 1: Abbreviations

2 Concept

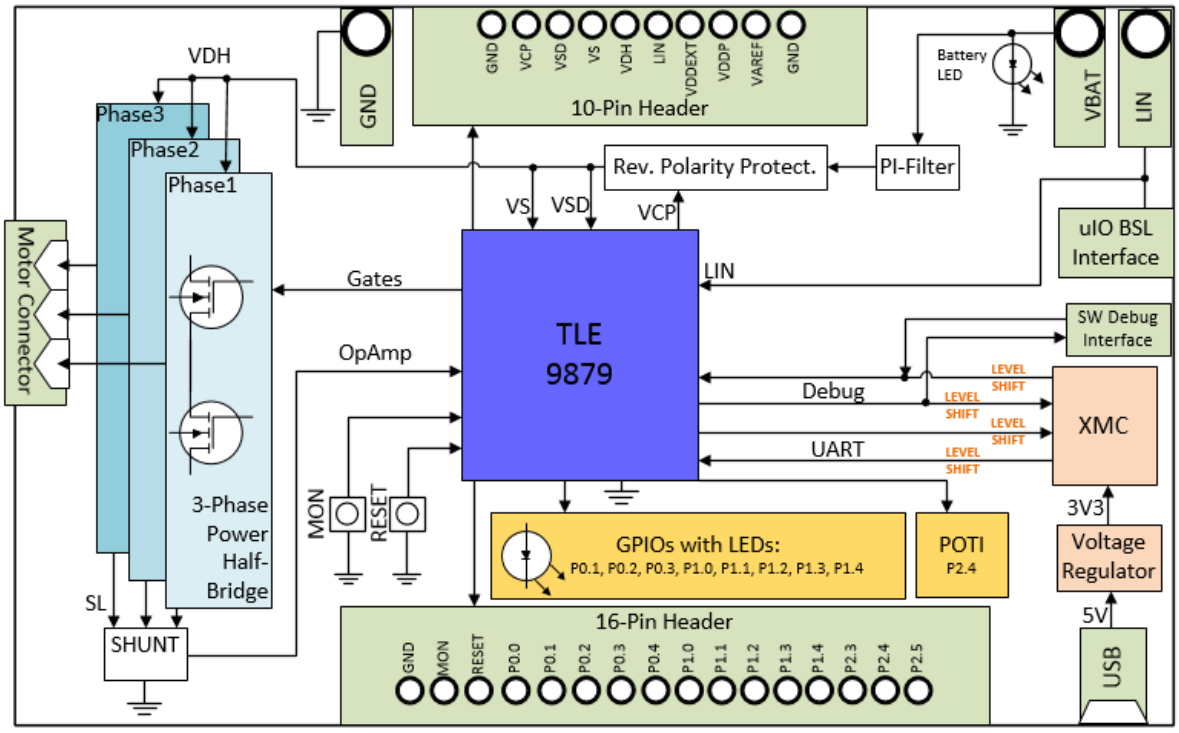


Figure 1: Board Concept

This board provides a simple, easy-to-use tool for getting familiar with Infineon's Embedded Power IC TLE9879QXA40 (further to be named: TLE9879). It contains the TLE9879 and its typical application circuit including three MOSFET half bridges to drive a BLDC motor. The board is ready to connect with car supply or similar and has an onboard J-Link debugger.

All relevant chip pins are connected to pin headers at the edge of the board, where signals can be probed or applied directly (see Table 2, Table 3). By different jumper settings LEDs can be put in parallel to several ports and selected functions can be configured (see Table 6). Push button switches allow easy hardware reset and triggering of the MON input. There are intended test points for all six gate driver pins, for measurements at the shunt, VDDC and several ground points on the evaluation board (see Figure 3). For testing analog signals ADC inputs can be varied by the potentiometer on board. Three phases of motor current can be picked off at a terminal block to connect a DC brushless motor.

The evaluation board can be operated by standard laboratory equipment as power supply and LIN communication are working via banana jacks. Debugging and UART are provided via an USB interface combined with an onboard Segger J-Link (XMC4200). Bidirectional level shifters ensure that the respective XMC pins are in tristate as long as UART or debugging is not used.

An SWD interface is available to use another ISP than the onboard J-Link. To program the TLE9879 via LIN there is an additional uIO BSL interface (see Table 4). There is a battery LED that indicates that the board is supplied the right way. Otherwise reverse polarity protection secures the board from damage by cross connection.

3 Interconnects

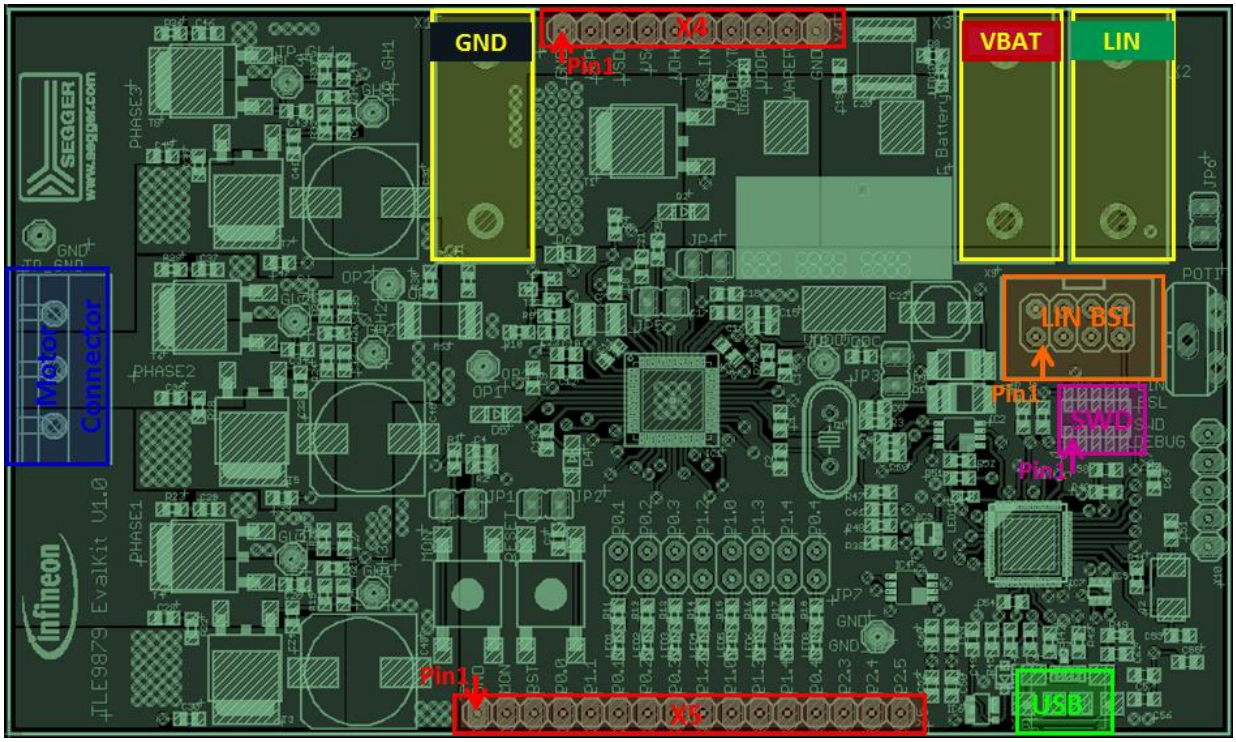


Figure 2: Interconnects

Banana jacks (marked yellow)
There are jacks in different colors for ground, supply (max.28V) and LIN communication via banana jack: GND (black), VBAT (red), LIN (green)

Pin Ports X4 and X5 (marked red)
Soldering pin headers with 2,54mm pitch for X4 (1x10) and X5(1x16) yields test points for the TLE9879 pins. The following signals are connected to the pins:

X4:

1	2	3	4	5	6	7	8	9	10
GND	VCP	VSD	VS	VDH	LIN	VDDEXT	VDDP	VAREF	GND

Table 2: Pin Configuration Top Line Pin Port (X4)

X5:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
GND	MON	RST	P0.0	P1.1	P0.1	P0.2	P0.3	P1.2	P1.0	P1.3	P1.4	P0.4	P2.3	P2.4	P2.5

Table 3: Pin Configuration Bottom Line Pin Port (X5)

Terminal block for connecting the motor (marked blue)
The three pins of the terminal block provide access to the three half bridges and are intended to connect a DC brushless motor.

USB for UART and Debugging (marked green)
With this Micro USB PC and evaluation board can get connected.

uIO BSL for LIN (marked orange)
For the uIO bootstrap loader an 8 pin header (2 x 4) with 2.54 mm pitch is placed on the board.
It is intended to connect additional hardware for bootstrap loading. This uIO interface can be used to program the TLE9879 via LIN (see www.infineon.com/uio).

NC	1	2	GND
NC	3	4	NC
LIN	5	6	VS
RESET	7	8	NC

Table 4: Pin Configuration onboard uIO BSL

Pin Header for SWD (marked purple)
There is a 10 pin header (2x5) with 1,27mm pitch on the evaluation board. For debugging with another ISP than the onboard Segger this interface can be used.
DBPRE will be implicitly connected to GND by connecting the external ISP. This keeps the XMC in reset state to prevent interference of the SWD communication.

5 V	1	2	SWDIO (TMS)
GND	3	4	SWCLK (P0.0)
GND	5	6	n.c.
n.c.	7	8	n.c.
DBPRE	9	10	RESET

Table 5: Pin Configuration SWD Interface

4 Test Points

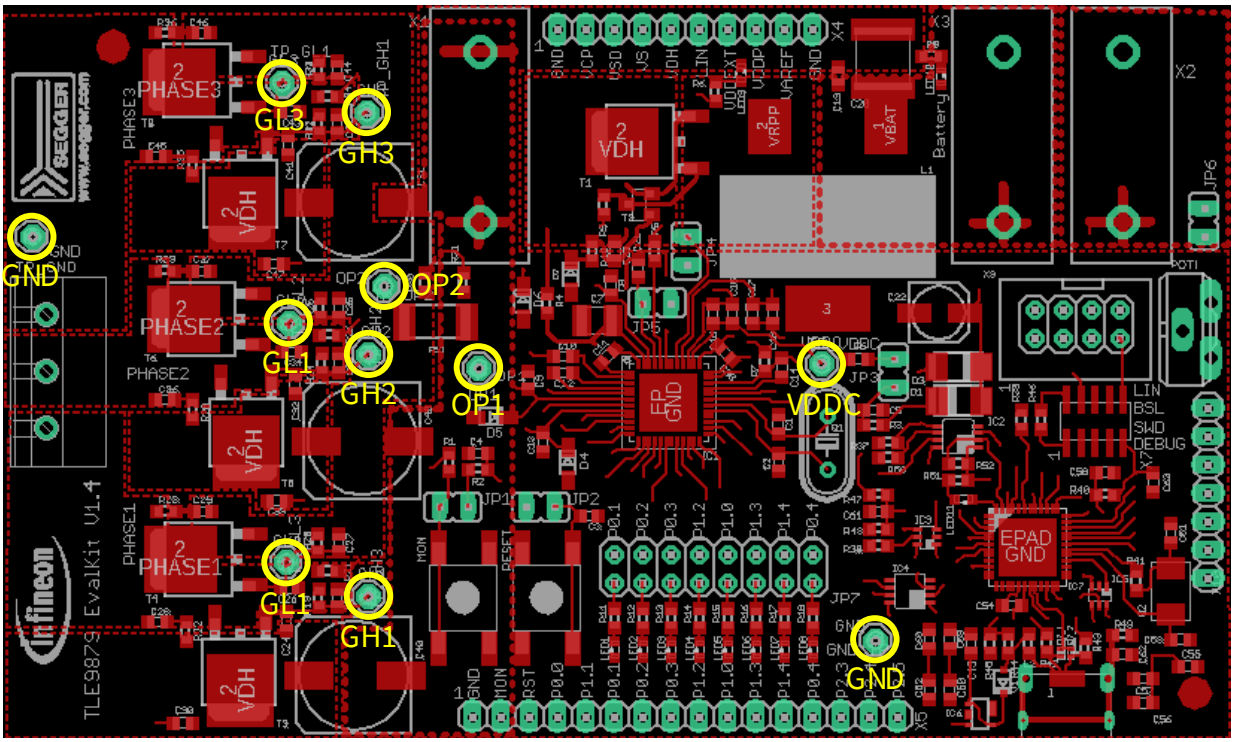


Figure 3: Test Points

The 3-phase power half-bridge is controlled by six gate driver pins, driving the gates of high side MOSFET and low side MOSFET for each phase. Each gate has an intended test point to measure the respective signals at high side gates and low side gates (GL1, GL2, GL3, GH1, GH2, GH3).
Test points OP1 and OP2 are provided at both sides of the shunt, which is 5mR.
Additionally, there is an intended test point for VDDC and various ground points.
All test points marked in the following figure are not populated. In order to use these pins, they have to be soldered in the designated solder holes.

5 Jumper Settings

The following table summarizes the jumpers' options. More information can be found in the text below.

JP1	Enable or disable MON button
JP2	Enable or disable RESET button
JP3	Select TLE9879 as LIN Master or LIN Slave
JP4	Connect or disconnect VAREF with VDDEXT
JP5	Replace by an ampere meter to measure input current
JP6	Enable or disable POTI
JP7	Enable or disable LED for respective GPIO

Table 6: Jumpers' functionalities

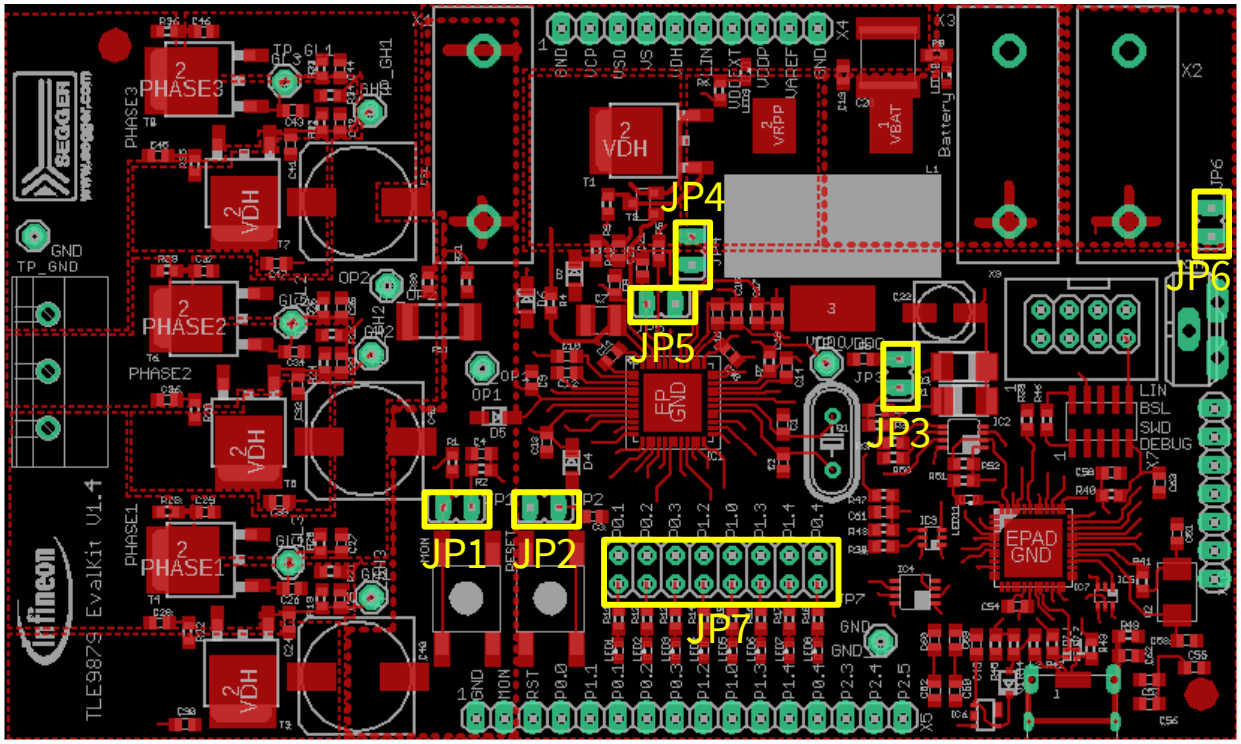


Figure 4: Jumpers

JP1: Close this jumper to connect MON button to MON input. Open it to disconnect MON button from MON input.
JP2: Close this jumper to connect RESET button to RESET input. Open it to disconnect RESET button from RESET input.
JP3: Close this jumper to connect an additional 1k pull-up resistor. This is intended for LIN master communication. Open the jumper to use the TLE9879 as slave in a LIN network. Software for LIN low level driver can be found at the homepage of IHR (www.ihr.de).
JP4: Close this jumper in order to supply VAREF by VDDEXT. In case VAREF is supplied externally the user has to take care by software that the internal VAREF is disabled. Open the jumper to use the internal VAREF which has to be enabled by software.
JP5: This jumper is closed by default. If this jumper is left open the device is not supplied. It is intended to open the VS line in order to measure the current flowing into the TLE9879.
JP6: Close this jumper to connect the potentiometer to P2.4. Open this jumper to disconnect the potentiometer.
JP7: Jumper 7 provides one individual jumper per LED in order to connect or disconnect the respective LED to the pin port.

P0.1	P0.2	P0.3	P1.2	P1.0	P1.3	P1.4	P0.4
LED1	LED2	LED3	LED4	LED5	LED6	LED7	LED8

Table 7: Combinations of GPIOs and LEDs

6 Communication Interfaces

6.1 LIN (via Banana jack and uIO BSL)

The device integrated LIN transceiver is connected to a banana jack and also to the uIO BSL interface. To integrate the device in a LIN network it is sufficient to use the single wire banana interface. The BSL interface is intended to program the device via LIN. For further information about the uIO interface see www.infineon.com/uio.

6.2 UART (via USB)

A virtual COM port provided by Segger driver enables a PC – board – communication via UART. The UART2 module of TLE9879 uses the pins P1.1 (transmit) and P1.2 (receive). Those are connected to the XMC4200, which emulates Rx and Tx on PC side with Segger firmware. Though they cannot be disconnected physically, bidirectional level shifters ensure that the XMC pins are hi-Z in case the virtual COM port is not used.
By connecting the evaluation board to the PC, a virtual COM port gets emulated by the Segger driver automatically. The port used will show up in the Microsoft® Windows® device manager.

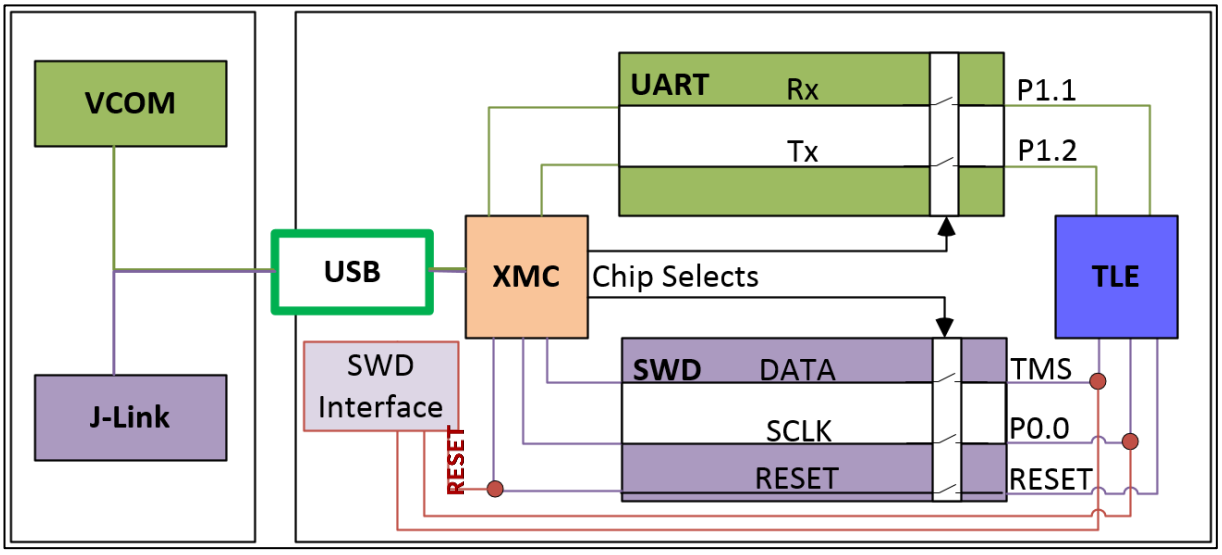


Figure 5: UART and Debugging

Note: Only one of the interfaces USB or SWD can be used at one time. While using the SWD interface the XMC is hold in reset. As long as a debugger is connected with the SWD interface it eliminates therefore debugging or UART via USB.

6.3 Debugging (via USB or SWD-Interface)

For serial wire debug the TLE9879 uses the pins TMS (data) and P0.0 (clock). Level shifters between XMC4200 and TLE9879 allow using P0.0, while it is not used for debugging.
The onboard J-Link module allows serial wire debugging via USB. An SWD interface is available in order to debug with another ISP than the onboard J-Link e.g. U-Link2. Therefore, the signals are routed through the 10 pin header SWD interface between the XMC4200 and the TLE9879. The pin configuration makes sure that the XMC is hold in reset while another debugger is physically connected as DBPRE will be implicitly connected to GND by connecting the external ISP (see Table 5).

7 Technical Data

Platine Size	110x66 mm
Voltage supply	max. 28V
Motor current	max. 20 A
Pin ports	5 V (GPIOs of TLE9879)

Table 8: Technical Data

8 Optional Additional Placements

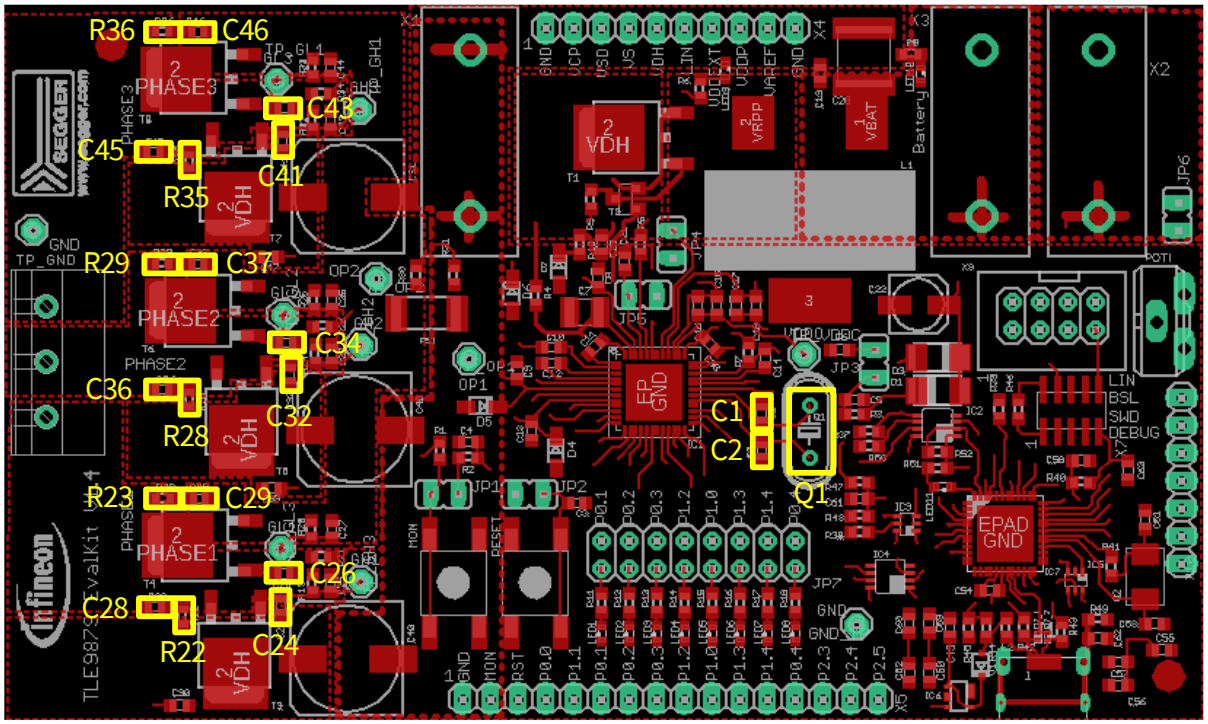


Figure 6: Additional Placements' positions

Values for these optional additional placements have to be determined depending on application.

Q1	External Oscillator
C1	Oscillator Capacitor 1
C2	Oscillator Capacitor 2
R22	Resistance Snubber High side MOSFET Phase 1
C28	Capacitor Snubber High side MOSFET Phase 1
C24	Gate Drain Capacitor High side MOSFET Phase 1
R23	Resistance Snubber Low side MOSFET Phase 1
C29	Capacitor Snubber Low side MOSFET Phase 1
C26	Gate Drain Capacitor Low side MOSFET Phase 1
R28	Resistance Snubber High side MOSFET Phase 2
C36	Capacitor Snubber High side MOSFET Phase 2
C32	Gate Drain Capacitor High side MOSFET Phase 2
R29	Resistance Snubber Low side MOSFET Phase 2
C37	Capacitor Snubber Low side MOSFET Phase 2
C34	Gate Drain Capacitor Low side MOSFET Phase2
R35	Resistance Snubber High side MOSFET Phase 3
C45	Capacitor Snubber High side MOSFET Phase 3
C41	Gate Drain Capacitor High side MOSFET Phase 3
R36	Resistance Snubber Low side MOSFET Phase 3
C46	Capacitor Snubber Low side MOSFET Phase 3
C43	Gate Drain Capacitor Low side MOSFET Phase 3

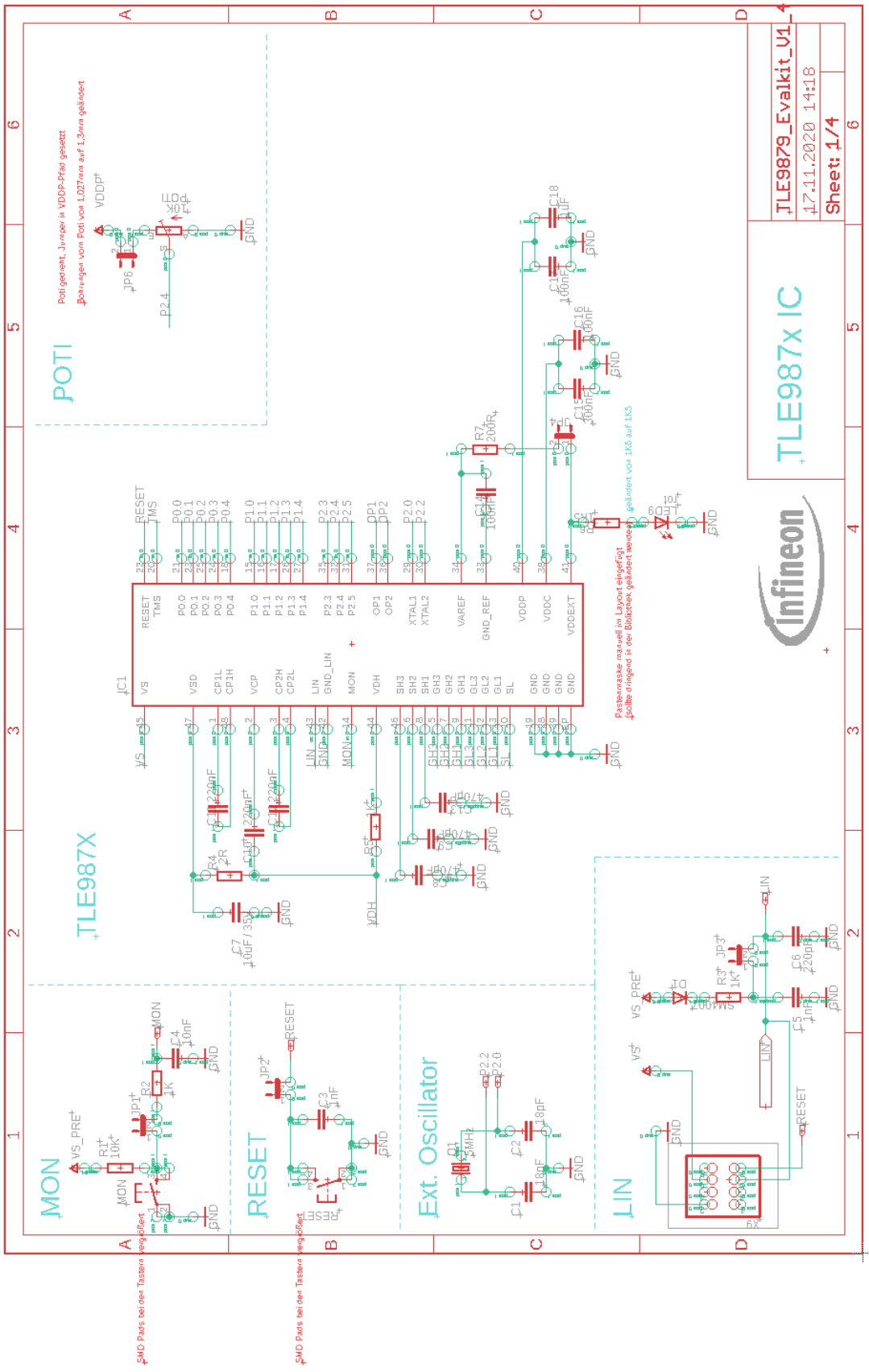
Table 8: Additional Placements

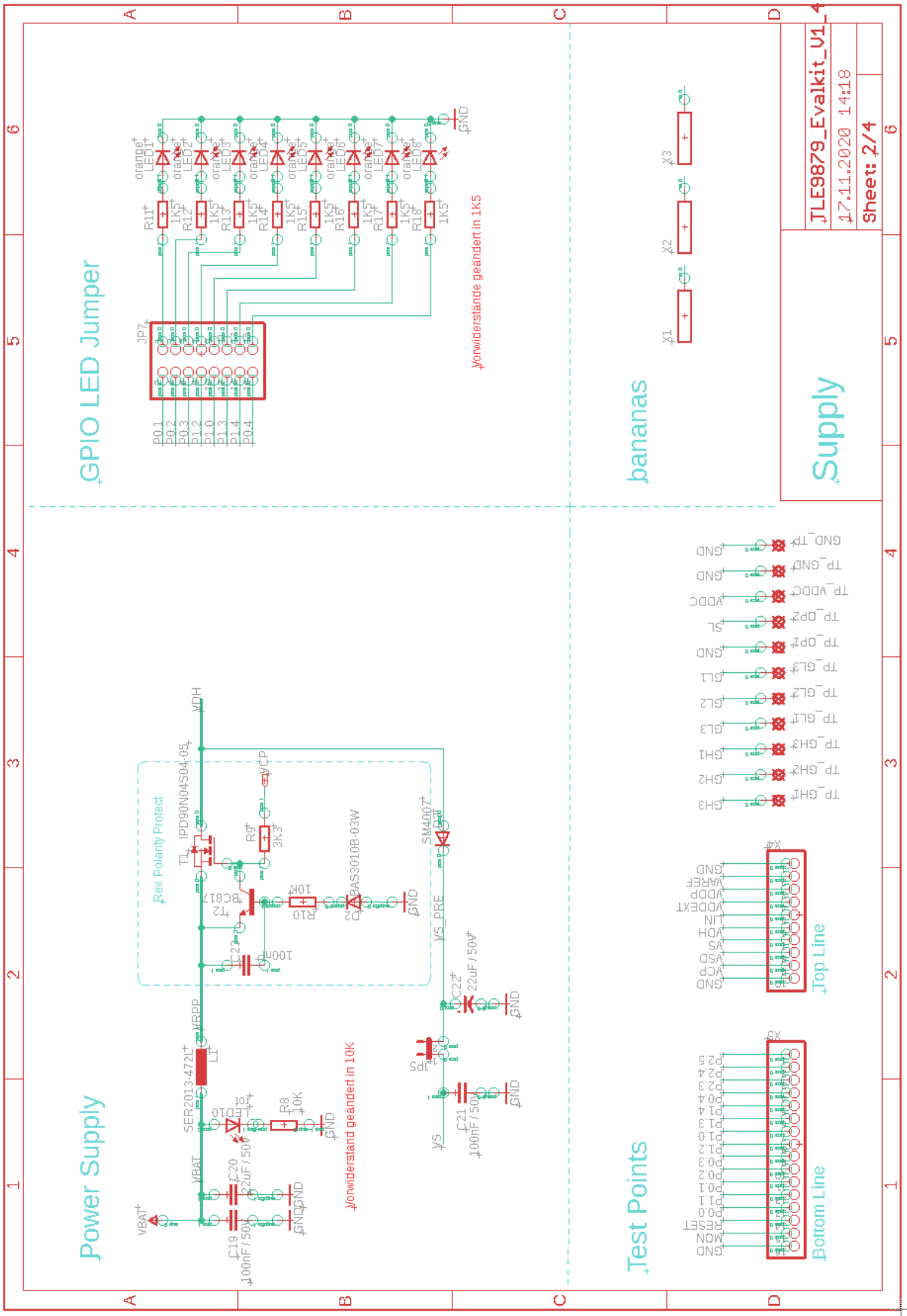
9 Changes with v1.3: Schematic

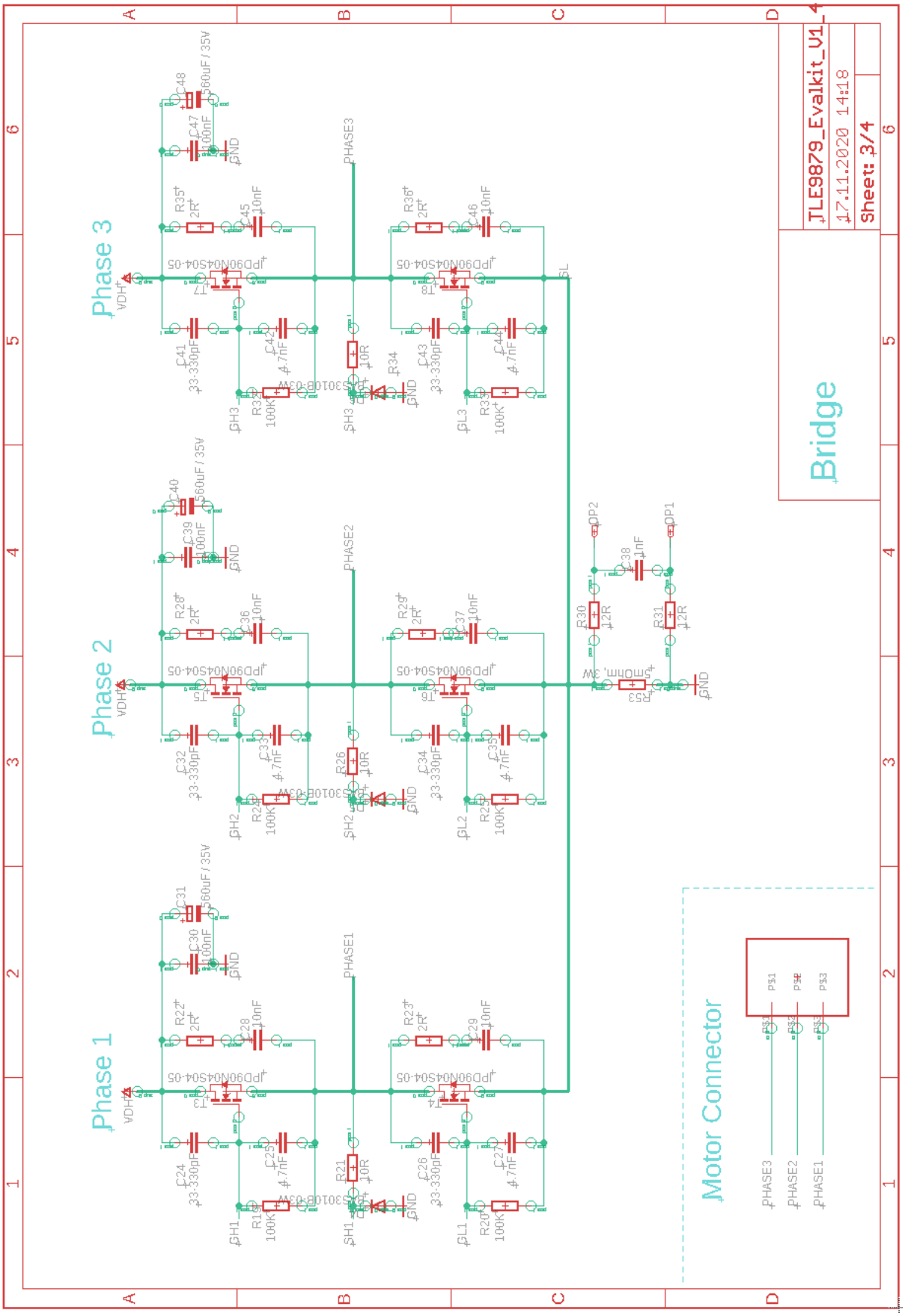
Pin P2.0 and pin P2.2 were swapped in the schematic.

10 Schematics and Layout

10.1 Schematic




GPIO LED Jumper
bananas
Supply
Power Supply
Test Points
Top Line
Bottom Line
Rev. Polarity Protect
TLE9879_Evalkit_V1_4
17.11.2020 14:18
Sheet: 2/4
Vorwiderstände geändert in 1K5
Vorwiderstand geändert in 10K


Phase 1
Phase 2
Phase 3
Bridge
Motor Connector
TLE9879_Evalkit_V1_4
17.11.2020 14:18
Sheet: 3/4
PHASE1
PHASE2
PHASE3
VDH
GND
SL
OP1
OP2
IPD90N04S04-05
IS3010B-03W
560uF / 35V
100nF
10nF
4.7nF
33-330pF
100K
10R
12R
5mOhm, 3W
1nF
2R
GH1
GH2
GH3
GL1
GL2
GL3
SH1
SH2
SH3
T3
T4
T5
T6
T7
T8
R19
R20
R21
R22
R23
R24
R25
R26
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R53
C24
C25
C26
C27
C28
C29
C30
C31
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C36
C37
C38
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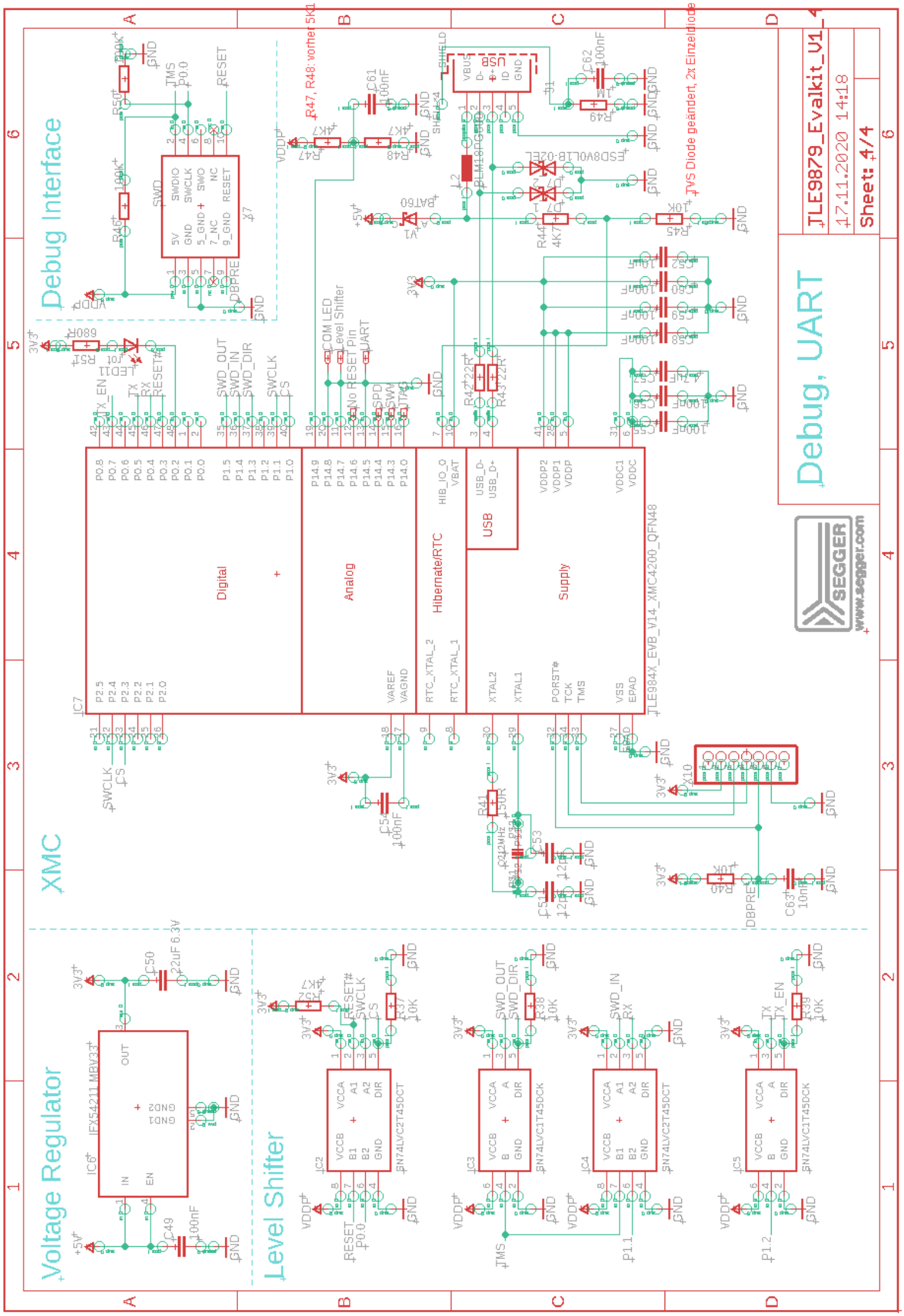
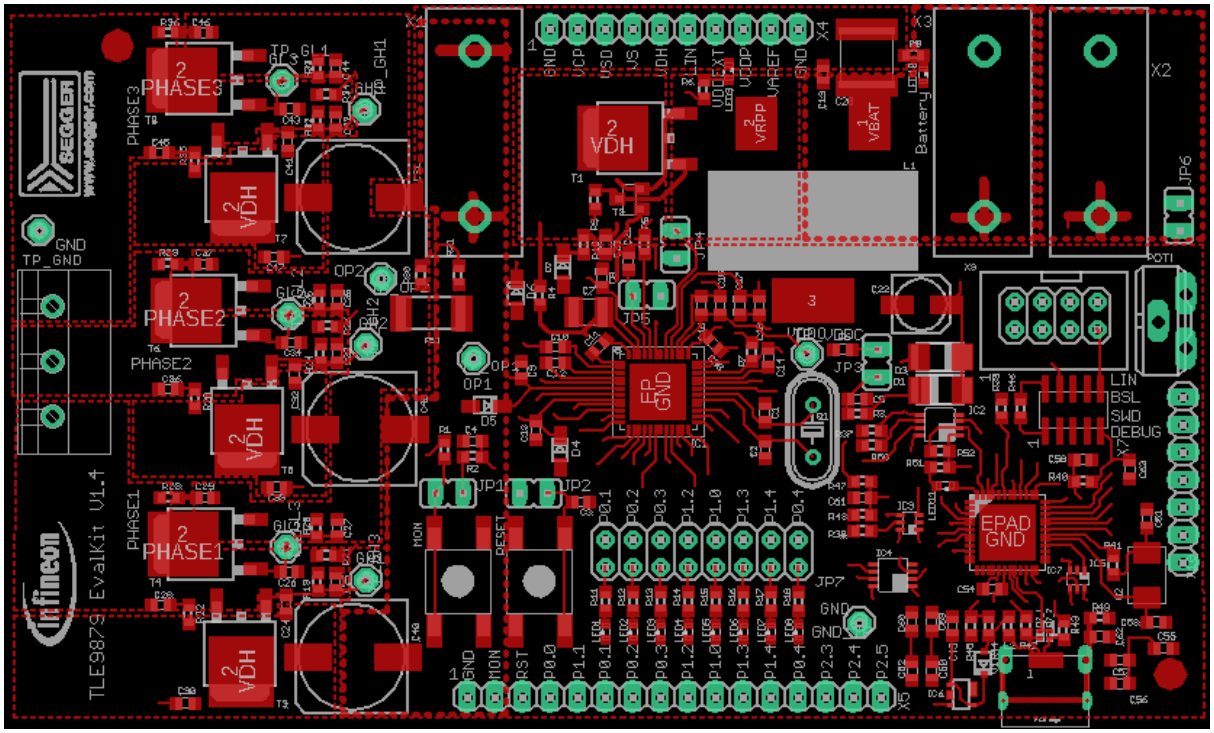
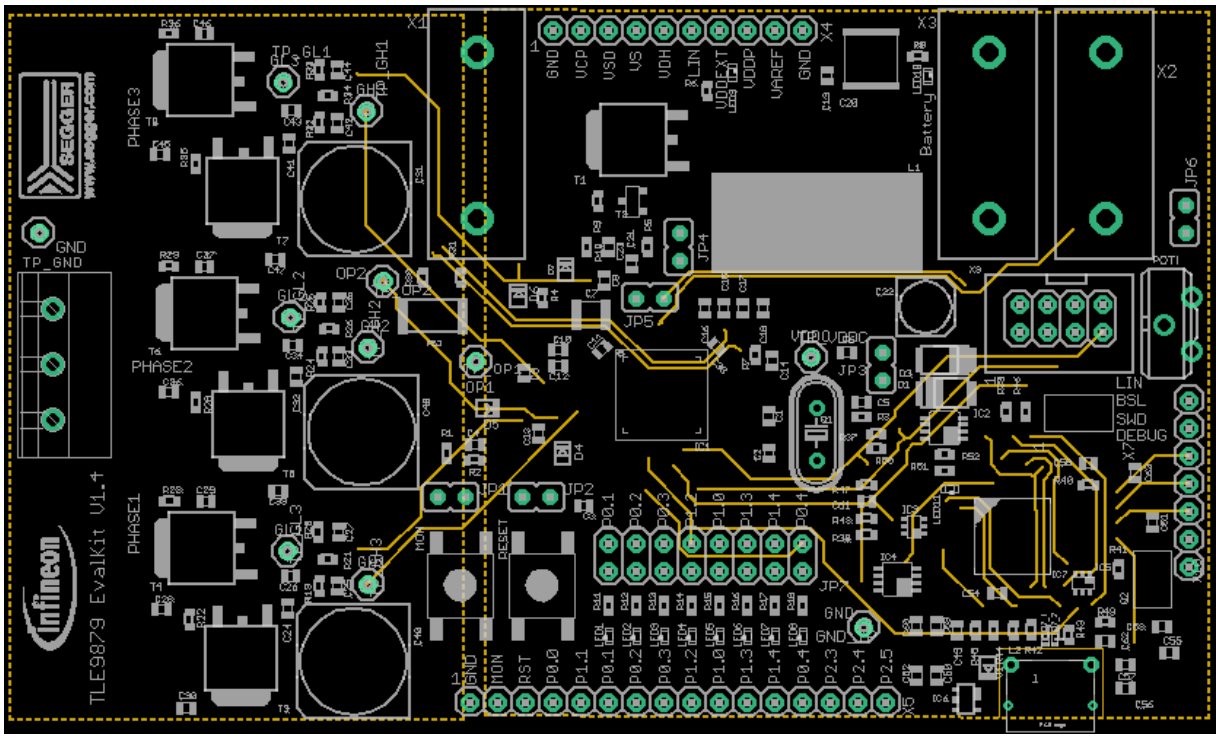
C40
C41
C42
C43
C44
C45
C46
C47
C48


Debug Interface
XMC
Debug, UART
Voltage Regulator
Level Shifter
TLE9879_Evalkit_V1_4
17.11.2020 14:18
Sheet: 4/4
R47, R48: vorher 5K1, jetzt 4K7
JVS Diode geändert, 2x Einzeldiode (bidirektional)
Digital
Analog
Hibernate/RTC
USB
Supply
TLE984X_EVB_V14_XMC4200_QFN48
IFX54211-MBV33
SN74LVC2T45DCT
SEGGER
www.segger.com

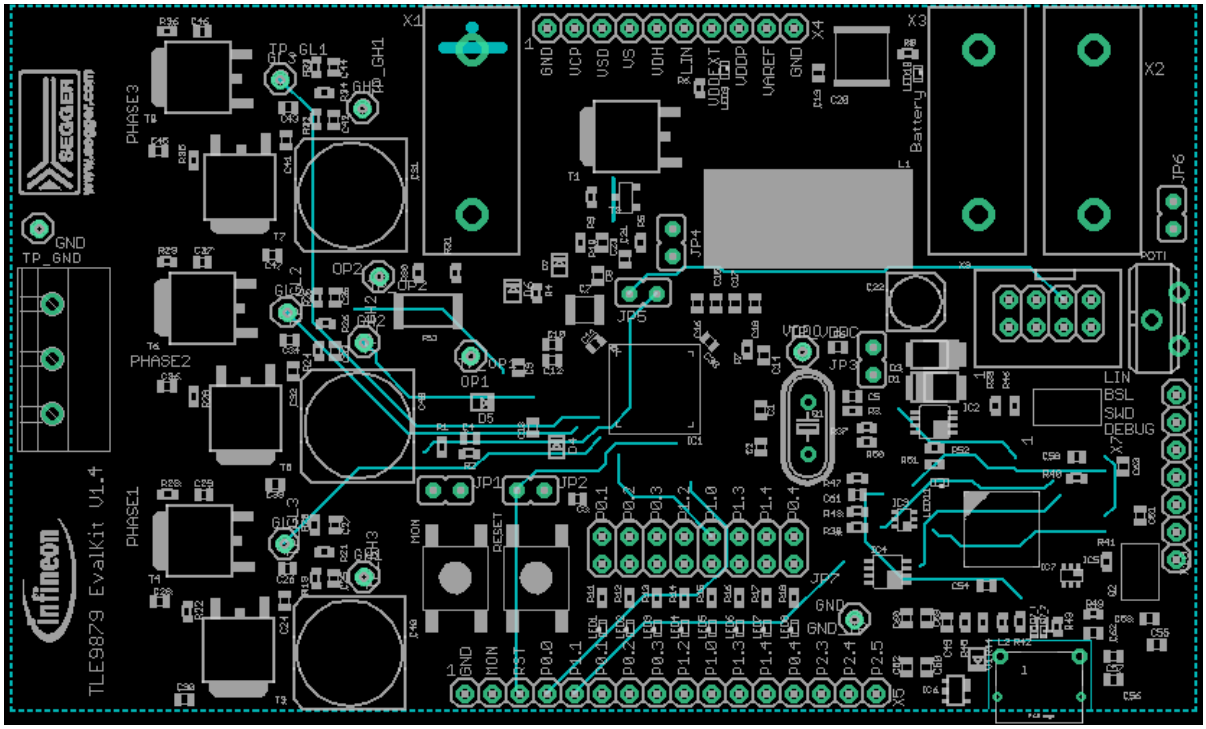
10.2 Layout



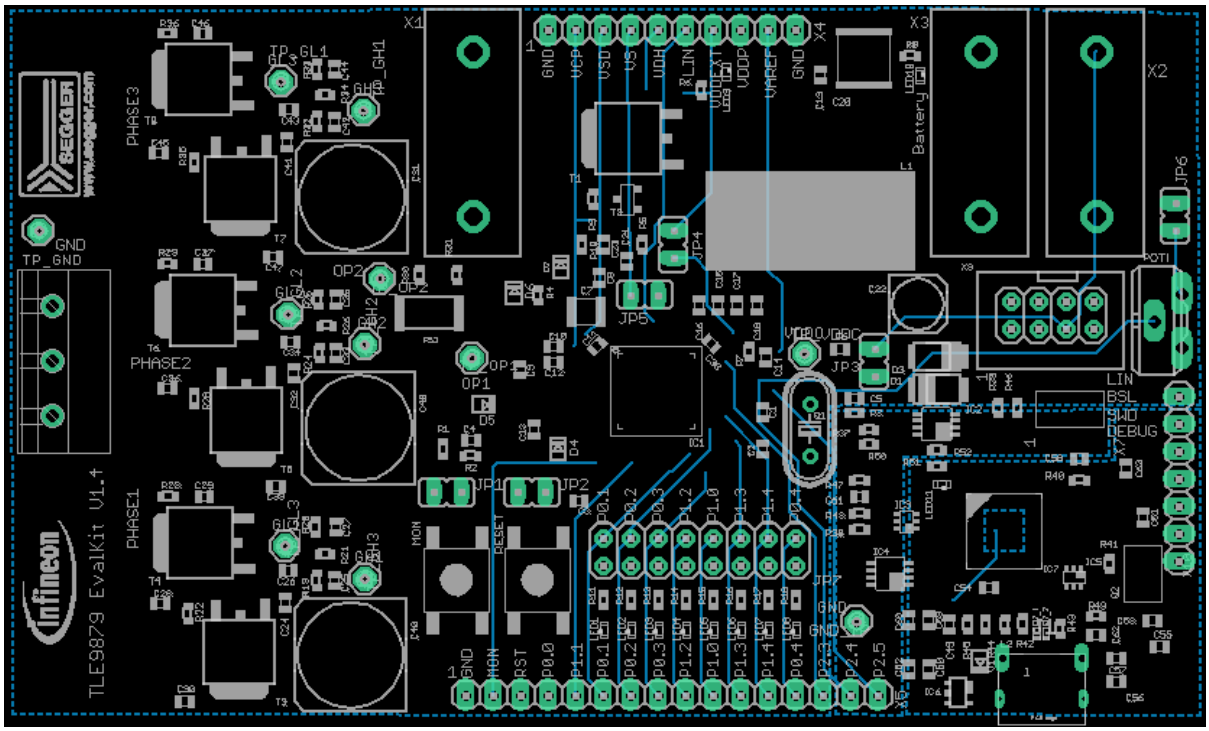
Top Layer



Layer 2



Layer 3



Bottom Layer