DEMO MANUAL DC209
HIGH SPEED A/D DEMO BOARD

LTC1404, SO-8 12-Bit 600ksps A/D Converter Demo Board

DESCRIPTION

The LTC®1404 is a 1.6µs, 600ksps, sampling 12-bit A/D converter that draws only 75mW from single 5V or ±5V supplies. The LTC1404 demo board provides the user with a way to evaluate the LTC1404 high speed A/D converter. In addition, the LTC1404 demo board is intended to illustrate the layout and bypassing techniques required to obtain optimum performance from this part. The LTC1404 demo board is designed to be easy to use and requires only ±7V to ±15V supplies, a conversion-start signal and an analog input signal. As shown in the Board Photo, the LTC1404 is a very space efficient solution for A/D users. By combining a 12-bit A/D, sample-and-hold, reference and clock circuitry into a single SO package, all the data acquisition circuitry, including the bypass caps, can be placed into an area of only 0.19 inch^2. The LTC1404 is intended for applications in telecommunications, digital signal processing, imaging or any high speed, high resolution data acquisition application.

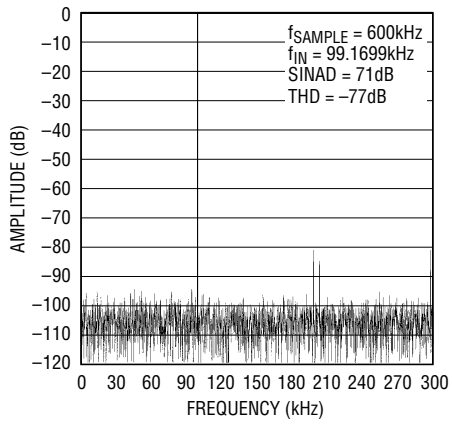
This manual shows how to use the demo board. Included are timing diagrams, power supply requirements and analog input range information. Additionally, a schematic, parts list, drawings and dimensions of all the PC board layers are included. An explanation of the layout and bypass strategies used in this board is also included so that anyone designing a PC board using the LTC1404 will be able to get the maximum performance from the device. **Gerber files for this circuit board are available. Call the LTC factory.**

Some key features of this demo board include:

- Proven 600ksps 12-bit ADC surface mount layout
- Actual ADC footprint only 0.19 inch^2, including bypass capacitors
- 72dB SINAD and –80dB THD at 100kHz inputs (Typ)

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

4096 Point FFT of LTC1404 Demo Board



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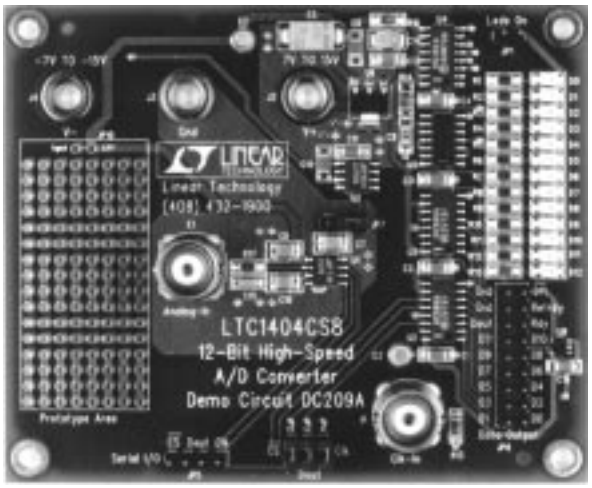
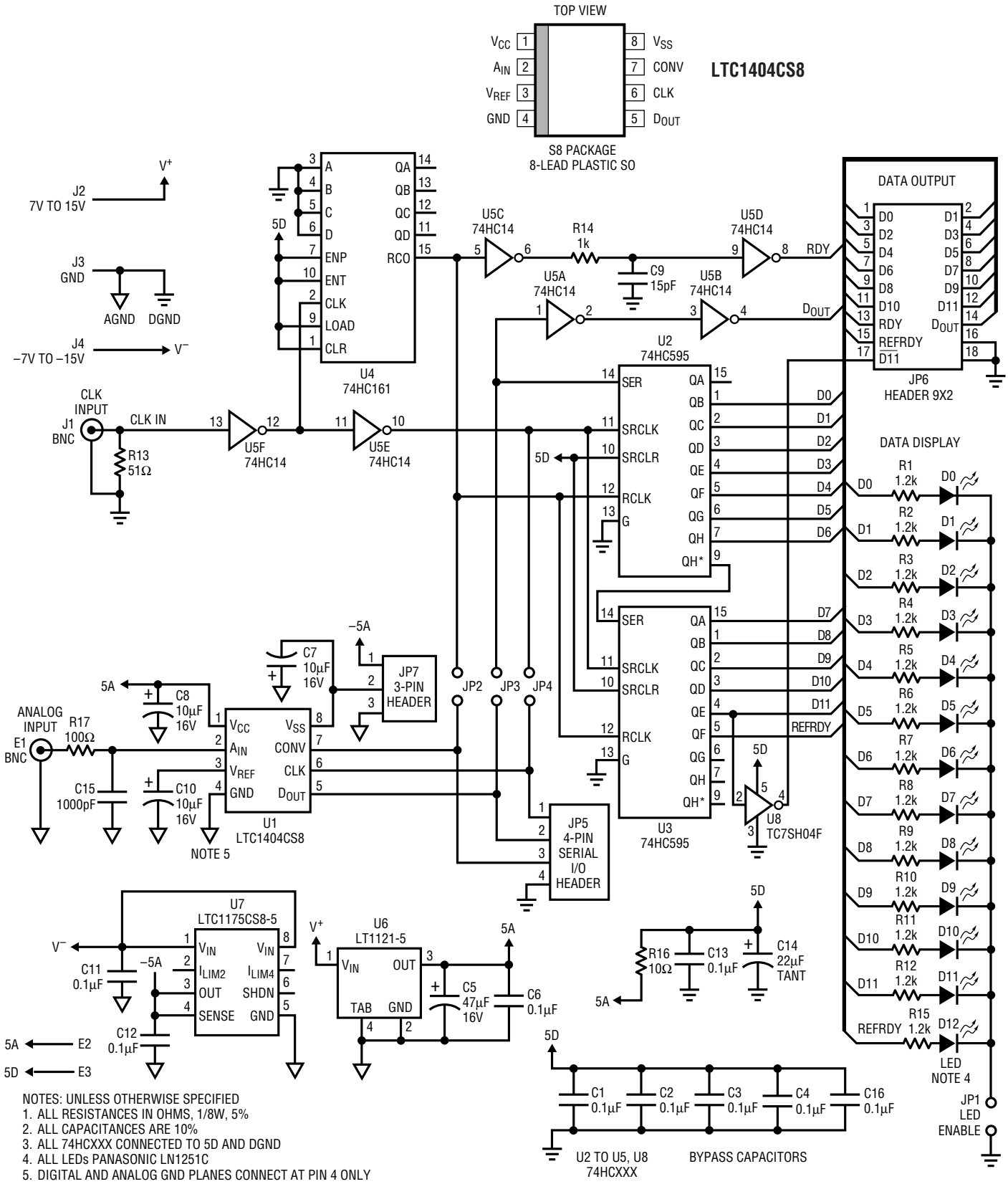
Board Photo



DC209 BP

PACKAGE AND SCHEMATIC DIAGRAMS



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES IN OHMS, 1/8W, 5%
2. ALL CAPACITANCES ARE 10%
3. ALL 74HCXXX CONNECTED TO 5D AND DGND
4. ALL LEDs PANASONIC LN1251C
5. DIGITAL AND ANALOG GND PLANES CONNECT AT PIN 4 ONLY

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1 to C4, C6, C11 to C13, C16	9	12065C104KATM	0.1µF 50V 10% X7R Capacitor	AVX	(843) 946-0362
C5	1	TAJD476K016R	47µF 16V 10% Tantalum Capacitor	AVX	(207) 282-5111
C7, C8, C10	3	GRM235Y5V106Z016	10µF 16V 10% Ceramic Capacitor	Murata Elect.	(814) 237-1431
C9	1	12065C150KATM	15pF 50V 10% X7R Capacitor	AVX	(843) 946-0362
C14	1	TAJB226K06R	22µF 6.3V 10% Tantalum Capacitor	AVX	(207) 282-5111
C15	1	12065A102KATM	1000pF 50V 10% NPO Chip Capacitor	AVX	(843) 946-0362
D0 to D12	13	LN1251C-(TR)	45mW 2.1V Red Surface Mount LED	Panasonic	(201) 348-5217
E1, J1	2	222420-1	50Ω PC-Mount BNC Vert Connector	AMP	(717) 564-0100
E2, E3	2	2501-02	0.094 Noninsulating Terminal	Mill-Max	(516) 922-6000
J2, J3, J4	3	575-4	0.175-ID Banana Jack	Keystone	(718) 956-8900
JP1 to JP4	4	3801S-2-G1	2-Pin Header	Comm Con	(626) 301-4200
JP5	1	3801S-4-G1	4-Pin Header	Comm Con	(626) 301-4200
JP6	1	3201S-18-G1	2-Row 18-Pin Header	Comm Con	(626) 301-4200
JP7	1	3801S-3-G1	3-Pin Header	Comm Con	(626) 301-4200
P2 to P4, P7	4	CCIJ230-G	Shunt	Comm Con	(626) 301-4200
R1 to R12, R15	13	CR18-122JM	1.2k 1.8W 5% Chip Resistor	TAD	(800) 508-1521
R13	1	CR18-510JM	51Ω 1/8W 5% Chip Resistor	TAD	(800) 508-1521
R14	1	CR18-102JM	1k 1/8W 5% Chip Resistor	TAD	(800) 508-1521
R16	1	CR18-100JM	10Ω 1/8W 5% Chip Resistor	TAD	(800) 508-1521
R17	1	CR18-101JM	100Ω 1/8W 5% Chip Resistor	TAD	(800) 508-1521
U1	1	LTC1404CS8	12-Bit High Speed A/D Converter	LTC	(408) 432-1900
U2, U3	2	MC74HC595AD	8-Bit Shift Register IC	Motorola	(800) 441-2447
U4	1	MC74HC161AD	4-Bit Binary Counter IC	Motorola	(800) 441-2447
U5	1	MC74HC14AD	Hex Inverter IC	Motorola	(800) 441-2447
U6	1	LT1121-5	5V Regulator IC	LTC	(408) 432-1900
U7	1	LTC1175CS8-5	–5V Regulator IC	LTC	(408) 432-1900
U8	1	TC7SH04F	Inverter IC	Toshiba	(714) 455-2000

OPERATION

OPERATING THE BOARD

Powering the Board

To use the demo board, apply 7V to 15V to banana jack J2, –7V to –15V to jack J4 and 0V (ground) to J3. Make sure that the power source(s) for these voltages can supply at least 200mA. Be careful to observe the correct polarity. Onboard regulators provide ±5V to the LTC1404. An LT1121-5 regulator provides 5V for analog and digital circuitry and –5V is provided for the A/D and buffer by the LTC1175-5 regulator. A jumper (JP7) allows the ADC to be evaluated with a single 5V supply, if desired.

The Analog Input

Analog signals are applied to the LTC1404 demo board using BNC connector E1. The analog signal input range is ±2.5V. Optimum performance is achieved using a signal source that has low output impedance, low noise and low distortion. Signal generators, such as the B&K Type 1051 Sine Generator, give excellent results. Further, this generator can be configured to operate referenced to a master clock signal, as shown in Figure 1. If this or other low noise

OPERATION

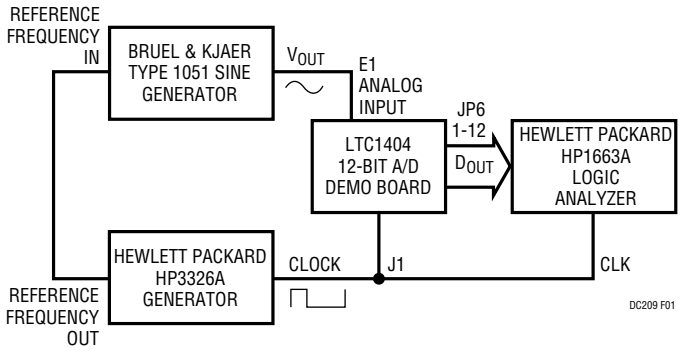


Figure 1. Typical Setup for LTC1404 Demo Board

generators are not available, the LTC1404 demo board has an RC lowpass filter, R17/C15, that reduces signal source noise. This filter is also beneficial when an input signal's bandwidth is less than one-half the sampling frequency. The filter reduces out-of-band noise that could compromise the LTC1404's conversion performance.

The filter is not necessary when the LTC1404 is used in undersampling applications, such as recovering a 50kHz baseband signal modulating a 455kHz carrier. Its wide 5MHz input bandwidth easily allows the LTC1404 to undersample the 455kHz carrier. The 50kHz signal can be recovered from the resultant conversion results.

Applying the Conversion-Start Signal

A conversion is initiated by a rising edge on the LTC1404 CONV input pin. This control signal is generated by U4 and is driven by the clock signal applied to CLK input J1. The CONV signal remains low, as shown in Figure 2, until the conversion is completed. During a conversion, transition of the CONV input can result in errors in the conversion value.

Reading the Output Data

The ADC serial data output is converted to parallel and buffered by the two 74HC595 shift registers and is available on connector JP6. The shift registers are used to drive the LEDs and connector JP6. In a practical circuit, the serial data of the ADC can be read directly. Serial data is available at jumper JP5. The ADC's serial I/O can be driven directly at JP5 by removing jumpers JP2, JP3 and JP4.

The LTC1404 output data is in two's complement format. The data can be converted to offset binary by using $\overline{D11}$ (JP6, Pin 17) instead of D11. Offset binary is used when an FFT is to be performed on the sampled data. A data ready (RDY) line (JP6, Pin 13) is provided to latch the D_{OUT} word. D_{OUT} is valid on the rising edge of Data Ready. Two ground lines are provided on the connector (JP6, Pins 16 and 18) for grounding a receiving system to the board.

The LTC1404 D_{OUT} word can be acquired with a logic analyzer. Conversion data can be stored on a disk and easily transferred to a PC by using a logic analyzer that has a PC-compatible floppy drive (such as an HP1663A). Once the data is transferred to a PC, programs such as MathCAD

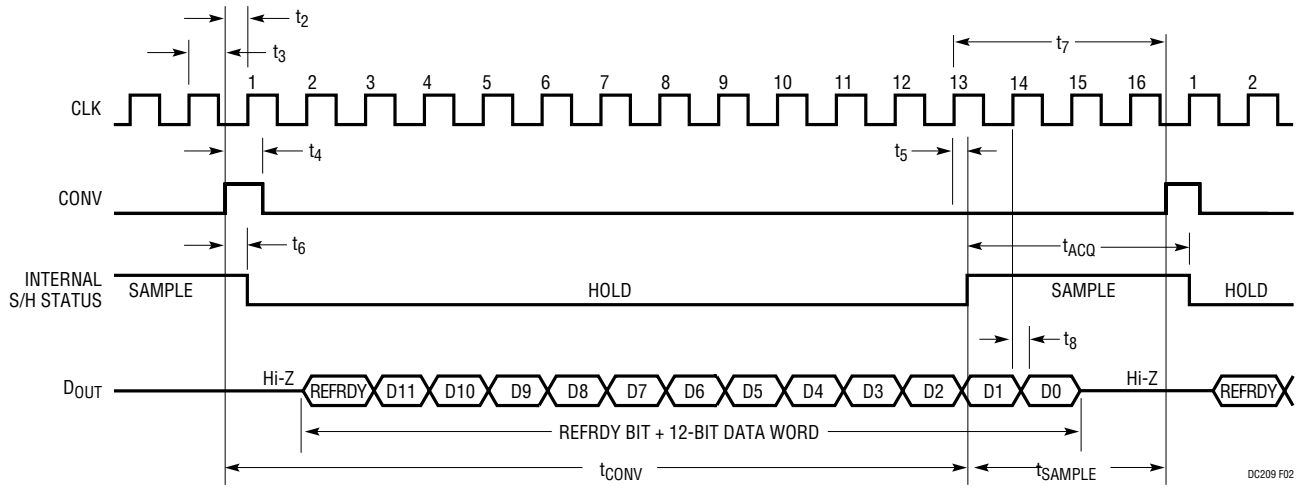


Figure 2. ADC Digital Timing Diagram (Timing Specifications Are Found in the LTC1404 Data Sheet)

OPERATION

or Excel can be used to calculate FFTs. The FFTs can be used to obtain LTC1404 AC specifications, such as signal-to-noise ratio and total harmonic distortion.

LEDs D0 to D11 provide a visual display of the LTC1404 digital output word. D0 is the LSB and D11 is the MSB. Jumper JP1 can be removed to disable the LEDs, reducing supply consumption by up to 36mA.

LAYOUT

The use of separate analog and digital ground planes is a good practice for a well designed PC board using the LTC1404. The proper way to make the analog and digital ground planes can be seen by examining the solder side of the PCB layout. The two ground planes are completely isolated except for one connection near the top of the board. The two ground planes follow the same path on the component and solder sides of the board to reduce coupling between the ground planes. Because any trace that opens a portion of the ground plane may reduce the ground plane's efficiency, the ground plane's solder side has a limited number of plane-breaking traces within it. The analog and digital traces do not cross each other (whether on the board's top or bottom side) or run adjacent to each other. The LTC1404's ground pin (GND) is connected directly to the analog ground plane. This produces the lowest noise condition.

BYPASS

It is important that the supply and reference bypass capacitors for the LTC1404 be placed as close as possible to the supply and reference pins. The ground side of the capacitors should have very short paths to analog ground. The V_{CC} and V_{REF} pins should be bypassed with high quality (low ESR) tantalum capacitors of at least 10µF. V_{SS} is less critical and should be bypassed with a ceramic capacitor of at least 0.1µF.

Table 1

JUMPER	JUMPER NAME	JUMPER CONNECTION
JP1	LED Enable	Shorted to enable LEDs. Open to disable the LEDs
JP2	$\overline{CONV}$ ($\overline{CS}$ on Silkscreen)	Shorted for normal operation. If open, the CONV line can be driven externally to control the start of conversion
JP3	D_{OUT}	Shorted for normal operation. If open, the D_{OUT} serial data output line can be read externally
JP4	CLK	Shorted for normal operation. If open, the CLK line can be driven externally

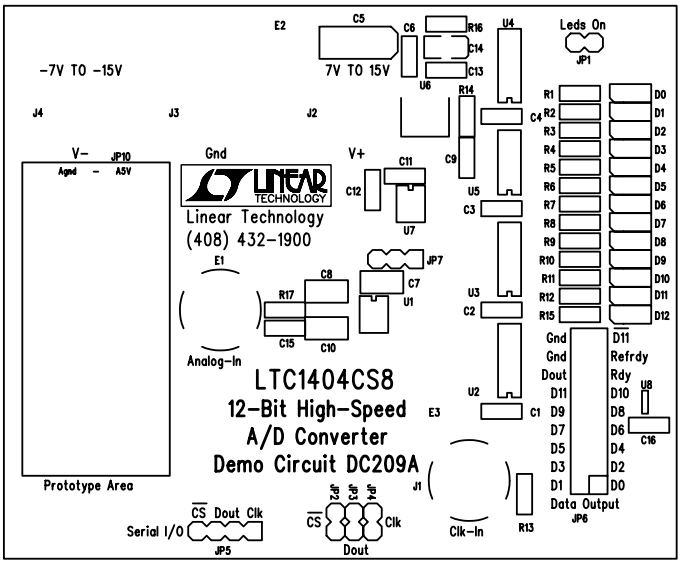
Table 2

INPUT/OUTPUT PIN	FUNCTION
E1	Analog Input: 0V to 4.096V, Unipolor or ±2.048V Bipolar
J1	Serial Clock Input: 0.1MHz to 9.6MHz
J2	7V to 15V at 200mA
J3	Ground
J4	–7V to –15V at 100mA
JP6-1	D_{OUT0} (LSB)
JP6-2	D_{OUT1}
JP6-3	D_{OUT2}
JP6-4	D_{OUT3}
JP6-5	D_{OUT4}
JP6-6	D_{OUT5}

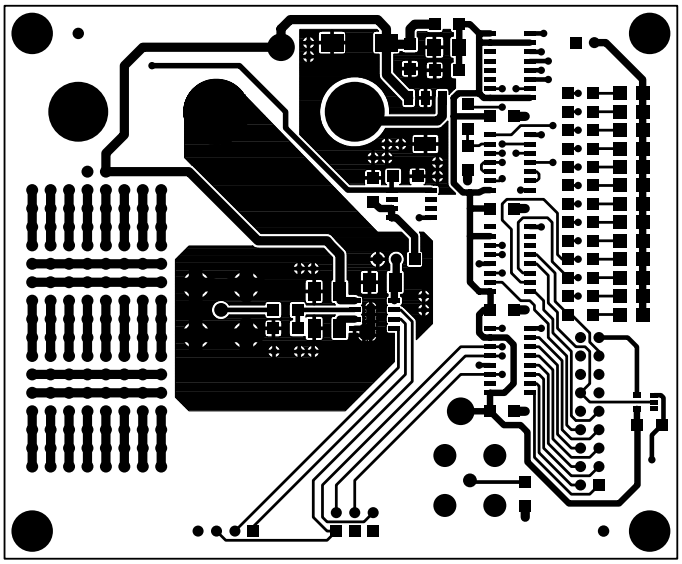
INPUT/OUTPUT PIN	FUNCTION
JP6-7	D_{OUT6}
JP6-8	D_{OUT7}
JP6-9	D_{OUT8}
JP6-10	D_{OUT9}
JP6-11	D_{OUT10}
JP6-12	D_{OUT11} (MSB)
JP6-13	RDY*
JP6-14	D_{OUT} (Serial Data)
JP6-15	REFRDY (Logic High = Stable Reference)
JP6-16	Digital GND
JP6-17	Inverted D_{OUT11}
JP6-18	Digital GND

* Can be used by an external system to latch the ADC's output. Latch data on the rising edge.

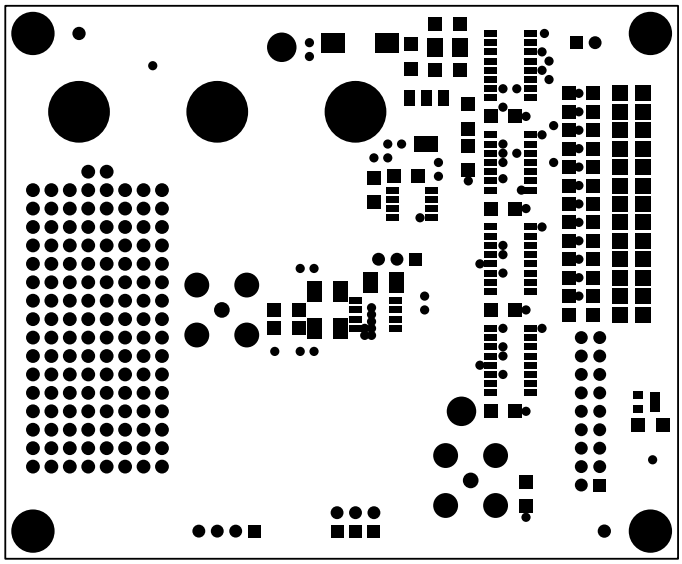
PCB LAYOUT AND FILM



Component Side Silkscreen

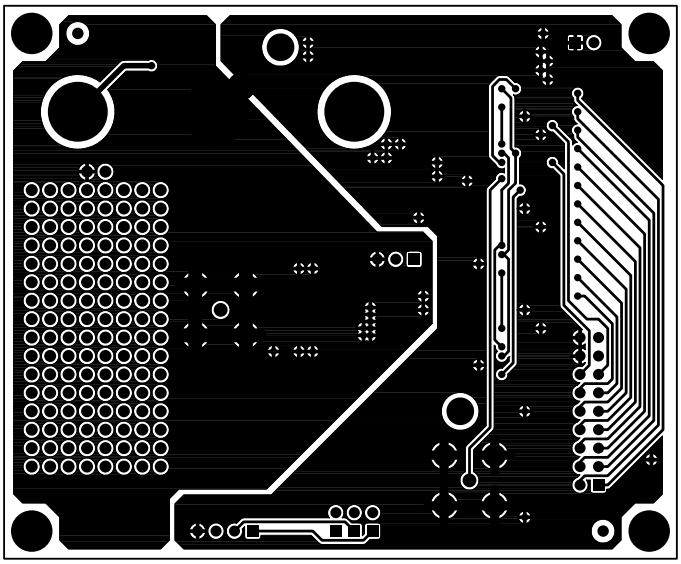


Component Side

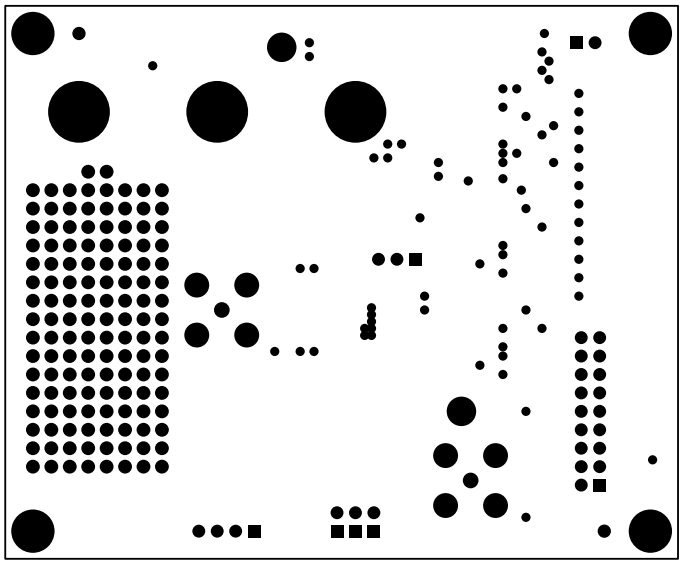


Component Side Solder Mask

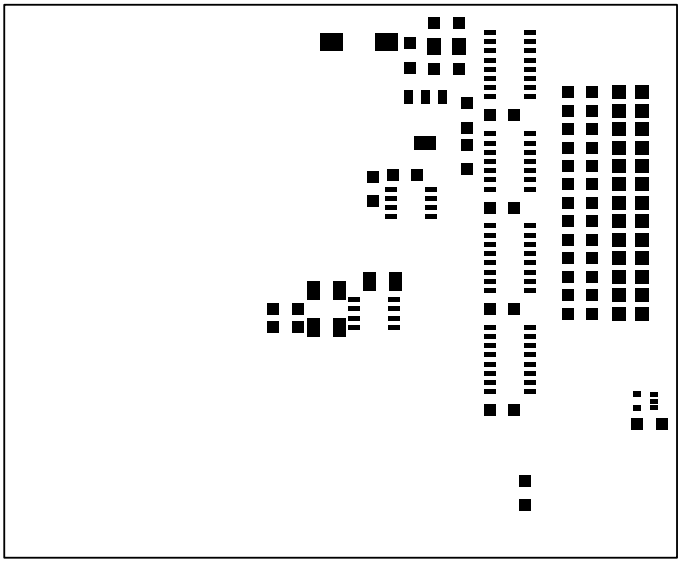
PCB LAYOUT AND FILM



Solder Side

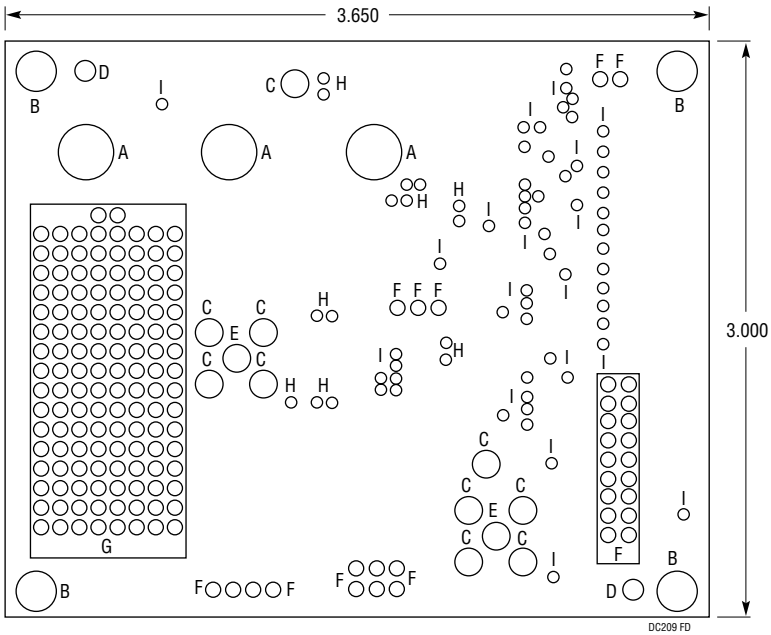


Solder Side Solder Mask



Pastemask Top

PC FAB DRAWING



NOTES:

1. MATERIAL: FR4 2 OZ COPPER CLAD THICKNESS
   0.062 ±0.006 TOTAL OF 2 LAYERS
2. FINISH: ALL PLATED HOLES 0.001 MIN/0.0015 MAX
   COPPER PLATE ELECTRODEPOSITED TIN-LEAD
   COMPOSITION BEFORE REFLOW, SOLDER
   MASK OVER BARE COPPER (SMOBC)
3. SOLDER MASK: BOTH SIDES USING GREEN SR1020 OR EQUIVALENT
4. SILKSCREEN: USING WHITE NONCONDUCTIVE EPOXY INK
5. ALL DIMENSIONS ARE IN INCHES

SYMBOL	DIAMETER	NUMBER OF HOLES	PLATED
A	0.207	3	YES
B	0.125	4	YES
C	0.095	10	YES
D	0.072	2	NO
E	0.052	2	YES
F	0.040	33	YES
G	0.032	130	YES
H	0.025	15	YES
I	0.020	56	YES

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
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