

Evaluating the **ADMV4530** Dual-Mode, Ka Band Upconverter With Integrated Fractional-N PLL and VCO

FEATURES

Fully featured evaluation board for the **ADMV4530**
On-board system demonstration platform (**SDP-S**) connector for SPI

5 V operation through LDO

ACE software interface for SPI control

EQUIPMENT NEEDED

5 V dc power supply

Baseband signal generator(s)

Spectrum analyzer

USB cable

SDP-S controller board

DOCUMENTS NEEDED

ADMV4530 data sheet

SOFTWARE NEEDED

ACE software

GENERAL DESCRIPTION

The **ADMV4530IQ-EVALZ** and the **ADMV4530IF-EVALZ** are the two evaluation boards available for the **ADMV4530** that work in inphase/quadrature (I/Q) mode and intermediate frequency (IF) mode, respectively. Both boards incorporate the **ADMV4530** Ka band upconverter with low dropout (LDO) regulators and an interface to the **EVAL-SDP-CS1Z (SDP-S)** controller board to allow the simple and efficient evaluation of the **ADMV4530**. The on-board LDO regulators allow the **ADMV4530** to be powered on by a single supply.

The **ADMV4530** is a highly integrated upconverter with an I/Q mixer that is ideally suited for next generation Ka band satellite communications. The chip can be programmed using a 4-wire serial port interface (SPI). The **SDP-S** controller allows the user to interface with the **ADMV4530** SPI through the Analog Devices, Inc., [Analysis, Control Evaluation \(ACE\)](#) software.

EVALUATION BOARD PHOTOGRAPHS

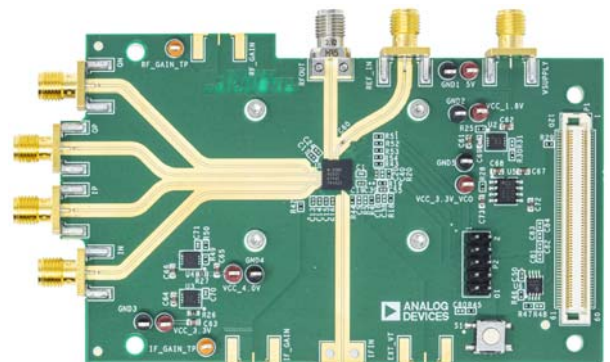


Figure 1. **ADMV4530IQ-EVALZ**

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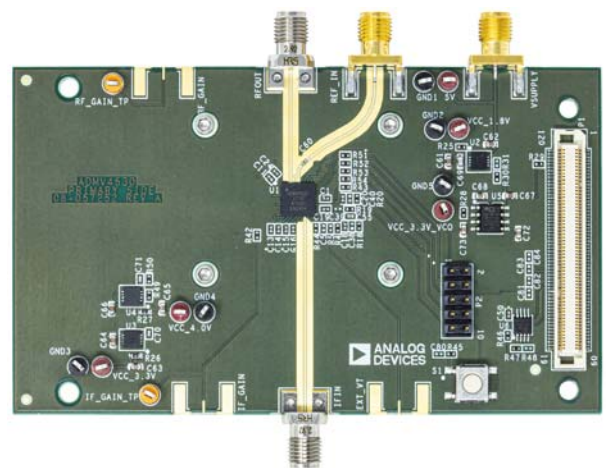


Figure 2. **ADMV4530IF-EVALZ**

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For full details on the **ADMV4530**, see the **ADMV4530** data sheet, which must be consulted in conjunction with this user guide when using the **ADMV4530IQ-EVALZ** and the **ADMV4530IF-EVALZ**.

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REVISION HISTORY

3/2020—Rev. 0 to Rev. A

Change to User Guide Title	1
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3/2020—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

Both the ADMV4530IQ-EVALZ and the ADMV4530IF-EVALZ evaluation boards have on-board ADMV4530 chips. Figure 3 and Figure 4 show lab bench setups for both boards.

For each setup, connect the SDP-S board to the on-board, 120-pin connector and then to the PC through the mini USB connector.

A 5 V dc power supply must be connected to the 5V and GND1 test points. Alternatively, the power supply can be connected to the VSUPPLY Subminiature Version A (SMA) port.

Two signal generators must be connected to the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ evaluation board. One signal generator provides the reference input signal, and the other signal generator provides either the IF input or the I/Q inputs. The IF input is a single-ended configuration, whereas the I/Q inputs are a differential configuration.

To observe the output signal from the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ board, connect a spectrum analyzer (or similar instrument) to the RF output (RFOUT) port.

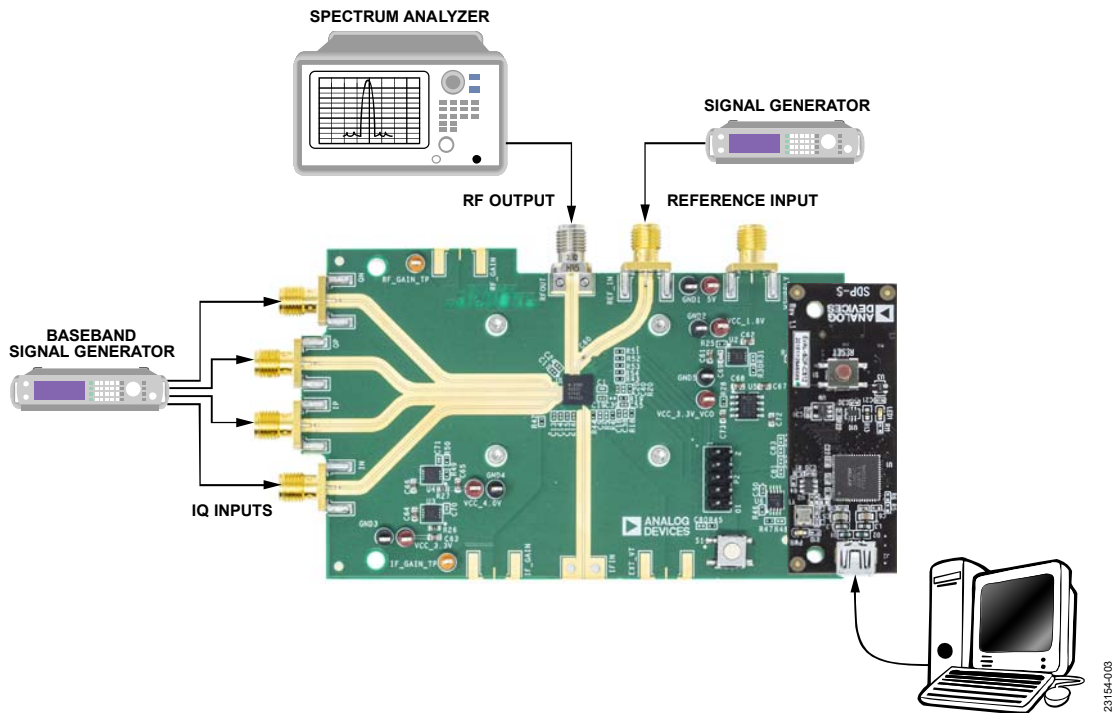


Figure 3. ADMV4530IQ-EVALZ Lab Bench Setup for I/Q Mode

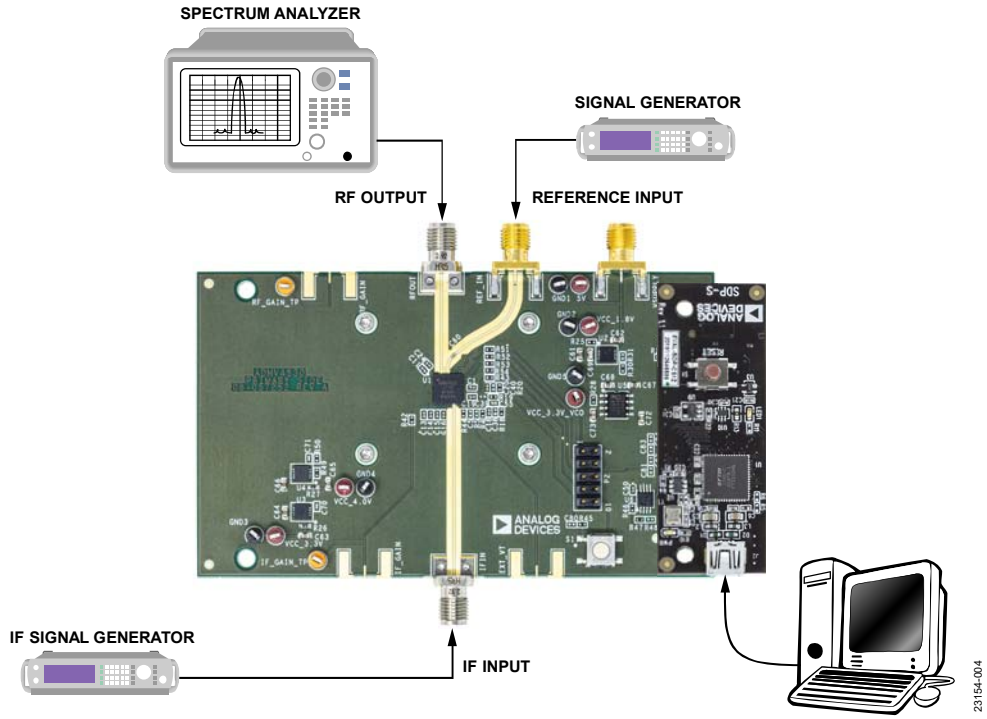


Figure 4. ADMV4530IF-EVALZ Lab Bench Setup for IF Mode

EVALUATION BOARD SOFTWARE

INSTALLING THE ACE SOFTWARE, ADMV4530 PLUG-INS, AND DRIVERS

The ADMV4530IQ-EVALZ and the ADMV4530IF-EVALZ use the Analog Devices Analysis|Control|Evaluation (ACE) software. For instructions on how to install and use the ACE software, go to www.analog.com/ACE.

If the ACE software is already installed on the PC, ensure that the installed software is the latest version, as shown on the www.analog.com/ACE page. If the previously installed software is not the latest version, take the following steps to install the updated ACE software:

1. Uninstall the current version of the ACE software on the PC.
2. Delete the ACE folder found in C:\ProgramData\Analog Devices.
3. Install the latest version of the ACE software. During installation, ensure that the .Net 40 Client, SDP Drivers, the LRF Drivers installations are checked off as well (see Figure 5).

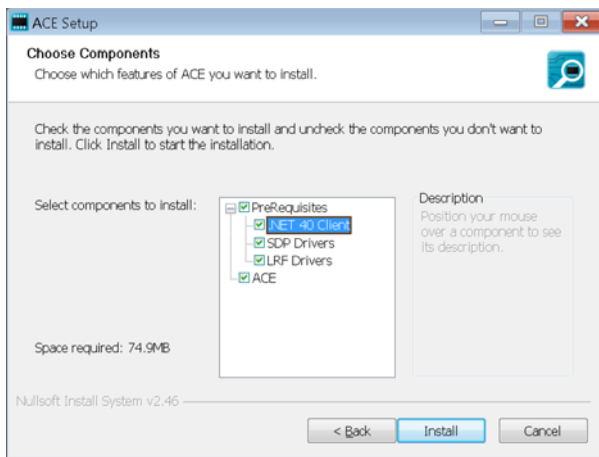


Figure 5. Required Driver Installations with the ACE Software

Once the installation finishes, the ADMV4530 evaluation board plug-in appears when the ACE software is open (see Figure 6).

Note that both the ADMV4530IQ-EVALZ and the ADMV4530IF-EVALZ evaluation boards use the same ACE plug-in, which displays on the main ACE screen as the ADMV4530 Board.

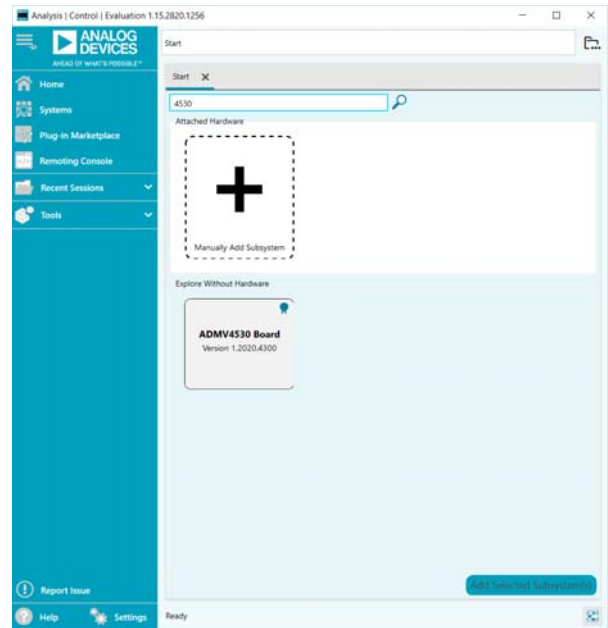


Figure 6. ADMV4530 Board Plug-In Window after Opening the ACE Software

PLUG-IN OVERVIEW

When either the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ is connected to the PC, the **ADMV4530 Board** appears in the **Attached Hardware** section. Double-clicking on the plug-in opens two tabs, the board level plug-in and the chip level plug-in, which are the **ADMV4530 Board** (see Figure 7) and the **ADMV4530** (see Figure 8), respectively.

The **ADMV4530** plug-in has the following functions and features:

- Device initialization
- Mode selection
- Block power downs
- Phase-locked loop (PLL) synthesizer settings
- Mixer settings
- Temperature sensor readback
- VCO core and band readback

Note that the **ACE** software provides a simple tutorial for testing the **ADMV4530**. For a more customized and detailed implementation, refer to **ADMV4530** data sheet for a full description of each block, register, and the corresponding settings.

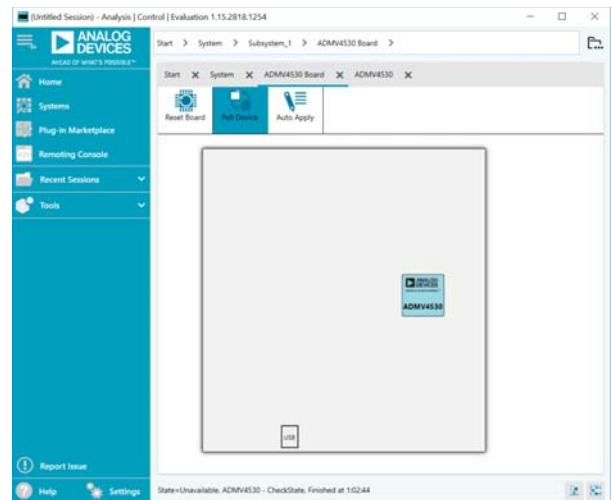


Figure 7. ADMV4530 Board Plug-In View

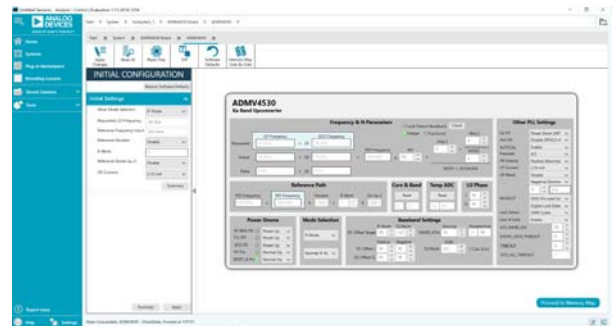


Figure 8. ADMV4530 Chip Block Diagram

PLUG-IN DETAILS

The full screen ADMV4530 user interface with labels is shown in Figure 9. The labels correspond to items listed in Table 1, which describes the functionality of each block. For additional detailed programming, refer to the ADMV4530 data sheet.

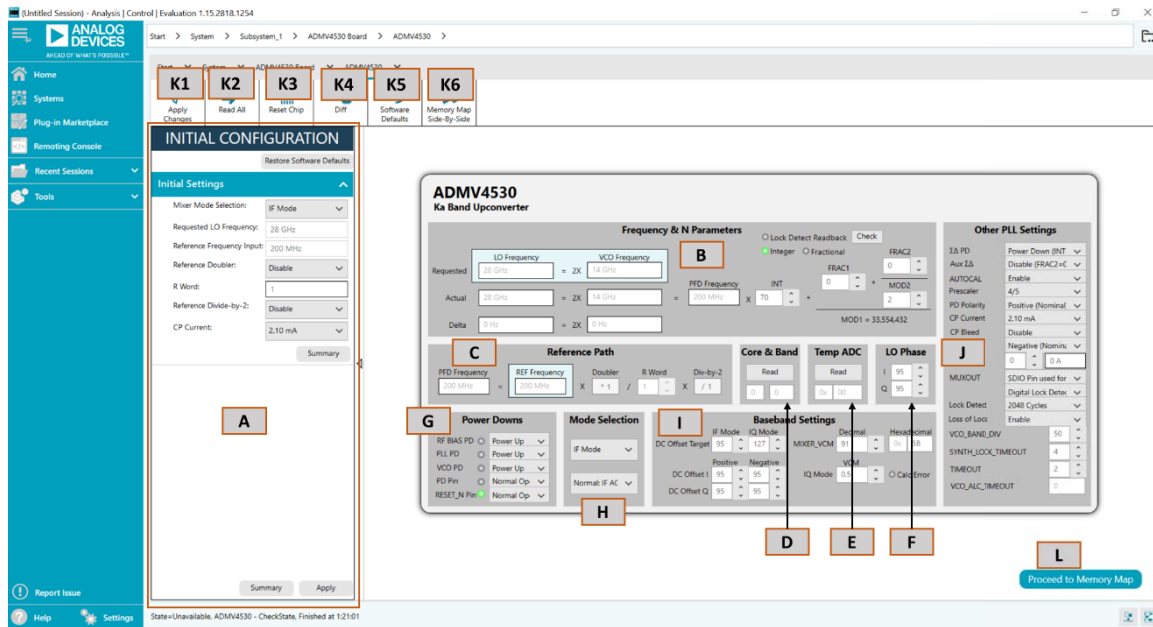


Figure 9. ADMV4530 Block Diagram with Labels

Table 1. ADMV4530 Block Diagram Label Functions (See Figure 9)

Label	Function
A	Use the Initial Configuration to initialize the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ evaluation board. Set the following under the Initial Settings section: Mixer Mode Selection: select IF, I/Q, or user defined mode. Requested LO Frequency: enter the requested local oscillator (LO) frequency. Reference Frequency Input: enter the reference input frequency. Reference Doubler: use the dropdown menu to disable or enable the reference doubler. R Word: enter the R word value. Reference Divide-by-2: use the dropdown menu to disable or enable the reference divide by 2. CP Current: use the dropdown menu to select the charge pump (CP) current. Summary: click this button to review the settings for the initial setup. Apply: click this button to apply the initial settings. The settings are reflected in the right sections. Note that clicking Apply Changes (Label K1) does not update the changes in this section.

Label	Function
B	<p>Use the Frequency & N Parameters section to change settings for the LO frequency after applying the initial settings in the Initial Configuration (Label A) section. This section includes the following:</p> <p>Requested LO Frequency and VCO Frequency: enter values in these two text boxes to trigger the INT, FRAC1, FRAC2, and MOD2 calculations.</p> <p>INT, FRAC1, FRAC2, and MOD2: calculations based on the requested LO or VCO frequency. Changing these values directly changes the actual LO and VCO frequency accordingly but does not change the requested LO and VCO frequency text boxes.</p> <p>PFD Frequency: calculation based on the Reference Path (Label C) section.</p> <p>Actual LO Frequency and VCO Frequency: the actual LO frequency and the actual VCO frequency are calculated from the PFD frequency, INT, FRAC1, FRAC2, MOD1, and MOD2 parameters shown on the right side of the equation (see Figure 9).</p> <p>Delta LO Frequency and VCO Frequency: the delta is computed from the difference between the requested and actual frequencies, which is useful for detecting if there is any residual frequency error due to limitations caused by synthesizer resolution.</p> <p>Lock Detect Readback: click the check button next to this option to check whether the PLL is locked.</p> <p>Integer and Fractional indication light: indicates if the chip is in integer or fractional mode.</p>
C	<p>Use the Reference Path section to change the reference parameters and PFD frequency after applying the initial settings in the Initial Configuration (Label A) section. This section includes the following:</p> <p>PFD Frequency: the calculated PFD frequency based on the equation on right (see Figure 9).</p> <p>REF Frequency: enter the reference input frequency.</p> <p>Doubler: click this button to enable or disable the doubler.</p> <p>R Word: scroll up and down to change the R word values, ranging from 1 to 32.</p> <p>Div-by-2: click this button to enable or disable the reference divide by 2 function.</p>
D	Click the Read button in the Core & Band section to read back the chip core and band values.
E	Click the Read button in the Temp ADC section to read back the chip temperature sensor values.
F	I and Q : scroll up and down to adjust the I and Q phase value in the LO Phase section.
G	<p>Use the Power Downs section to configure the different blocks power conditions in the chip. This section includes the following:</p> <p>RF BIAS PD, PLL PD, and VCO PD: scroll up and down to power up or power down these blocks in the chip.</p> <p>PD pin: scroll up and down to select normal operation or to power down the chip.</p> <p>RESET_N Pin: scroll up and down to select normal operation or to reset the power-on state.</p>
H	Use the Mode Selection section to select the mixer mode and configure the automatic gain control (AGC).
I	<p>Use the Baseband Settings section to configure the dc settings for both IF and I/Q mode and the mixer common-mode settings. This section includes the following:</p> <p>DC Offset Target: scroll up and down to set the target dc offset. Changing the values result in changes in DC Offset I and DC Offset Q values accordingly.</p> <p>DC Offset I, DC Offset Q: bidirectional calculation associated with DC Offset Target. Scroll up and down to change these values. The DC Offset Target changes accordingly.</p> <p>MIXER_VCM: scroll up and down to change the mixer common-mode voltage. The hexadecimal value is shown to the right.</p> <p>IQ Mode: scroll up and down to change the I/Q mode common-mode voltage (VCM).</p> <p>Calc Error light: this light illuminates if there is a calculation error when MIXER_VCM is changed to a value outside of the nominal equations. Refer to the ADMV4530 data sheet and Register 0x103 for more details.</p>
J	<p>The Other PLL Settings section consists of the following:</p> <p>ΣΔ PD: click the dropdown menu to power down or power up the Σ-Δ function. For integer mode, power ΣΔ PD down. For fractional mode, power ΣΔ PD up.</p> <p>Aux ΣΔ: click the dropdown menu to enable or disable this function.</p> <p>AUTOCAL: click the dropdown menu to enable or disable the auto calibration function.</p> <p>Prescaler: click the dropdown menu to select the prescaler.</p> <p>PD Polarity: click the dropdown menu to select the PD polarity.</p> <p>CP Current: click the dropdown menu to select the charge pump current.</p> <p>CP Bleed: click the dropdown menu to enable or disable the charge pump bleed.</p> <p>MUXOUT: click the dropdown menu to configure the MUXOUT signal, which can output to the SDO pin.</p>

Label	Function
	<p>Lock Detect: click the dropdown menu to change the counting cycles for lock detect.</p> <p>Loss of Lock: click the dropdown menu to enable or disable the loss of lock function.</p> <p>VCO_BAND_DIV, SYNTNH_LOCK_TIMEOUT, TIMEOUT, and VCO_ALC_TIMEOUT: use these text boxes to configure the parameters.</p>
K1	All changes, except within the Initial Configuration section, do not take effect until the Apply Changes button is clicked. If Auto Apply is highlighted in the ADMV4530 Board tab, the Apply Changes feature continuously runs every few seconds, and the Apply Changes button does not need to be clicked to apply or read back the block diagram settings.
K2	To read back all of the SPI registers of the device, click Read All .
K3	Click Reset Chip to reset the device.
K4	Click Diff to show registers that are different on the device.
K5	Click Software Defaults to restore the software defaults to the device, and then click Apply Changes .
K6	Click Memory Map Side-By-Side to enable the side by side memory map view.
L	Click Proceed to Memory Map to open the ADMV4530 memory map (see Figure 10)

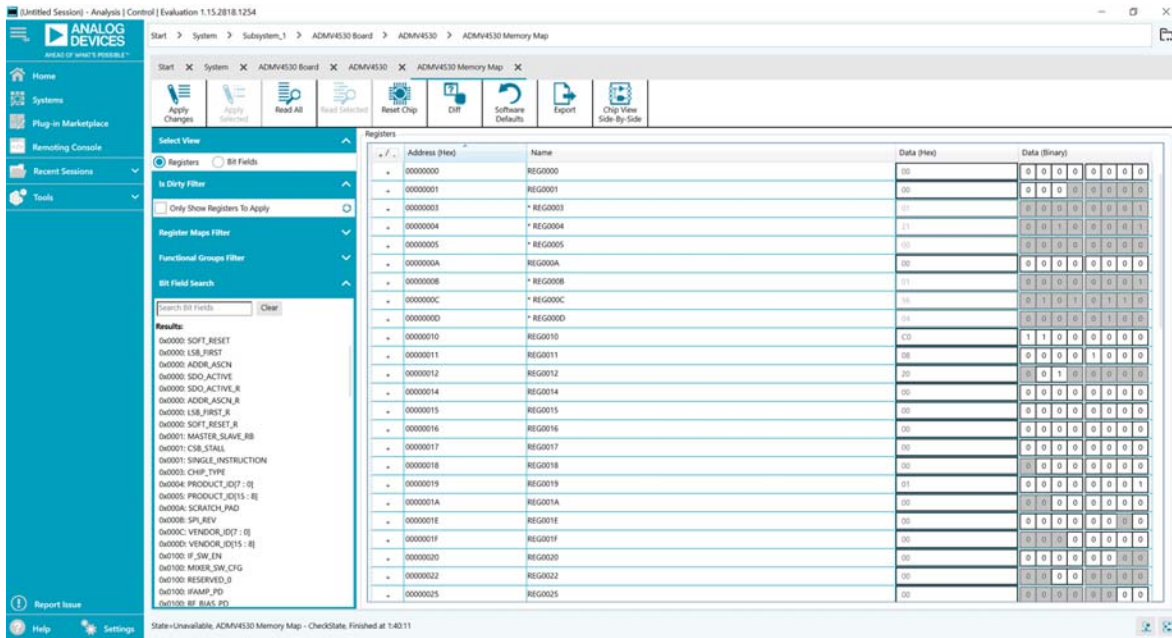


Figure 10. ADMV4530 Memory Map in the ACE Software

PERFORMING EVALUATION

ADMV4530IQ-EVALZ OR ADMV4530IF-EVALZ QUICK START

To set up the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ evaluation board, take the following steps:

1. Connect the [SDP-S](#) to the 120-pin connector on the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ evaluation board.
2. Connect a USB cable to the PC and then to the [SDP-S](#).
3. Connect a 5 V dc power supply to the 5V and GND1 test points. Alternatively, the power supply can be connected to the VSUPPLY SMA port. The power supply current limit must be set to 800 mA.
4. Connect the reference input signal generator to the REF_IN port on the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ evaluation board. Ensure that the board is set to the desired reference input frequency and power level.
5. Depending on which board is being evaluated, connect the signal generator for either IF input or I/Q inputs.
6. Connect a spectrum analyzer (or similar instrument) to the RFOUT port.
7. Open the [ACE](#) software. The **ADMV4530 Board** appears in the **Attached Hardware** section. Double-click on the plug-in to see the chip plug-in **ADMV4530** on screen.
8. Use the **Initial Configuration** in the [ACE](#) software to initialize the chip. Be sure to select the correct mixer mode of operation, either IF or I/Q mode. Additionally, set the desired PLL configuration settings, and then click **Apply** in the **Initial Configuration** section (see Figure 11).

The screenshot shows the 'INITIAL CONFIGURATION' window in the ACE software. It features a 'Restore Software Defaults' button at the top right. Below it, the 'Initial Settings' section is expanded, displaying several configuration parameters with their current values: Mixer Mode Selection is set to 'IF Mode', Requested LO Frequency is '28 GHz', Reference Frequency Input is '200 MHz', Reference Doubler is 'Disable', R Word is '1', Reference Divide-by-2 is 'Disable', and CP Current is '2.10 mA'. At the bottom of the window, there are 'Summary' and 'Apply' buttons.

Figure 11. ADMV4530 Initial Configuration Section

SIGNAL GENERATOR SETTINGS

When evaluating the ADMV4530IQ-EVALZ, a good starting point for configuring the signal generator inputs is as follows:

- Reference input frequency = 200 MHz
- Reference input power = 8 dBm
- I/Q input frequency = 25 MHz
- I/Q common mode voltage = 0.5 V
- In-phase (negative) IN input power = -16 dBm
- In-phase (positive) IP input power = -16 dBm
- Quadrature (positive) QP input power = -16 dBm
- Quadrature (negative) QP input power = -16 dBm

When evaluating the ADMV4530IF-EVALZ, a good starting point for configuring the signal generator inputs is as follows:

- Reference input frequency = 200 MHz
- Reference input power = 8 dBm
- IF input frequency = 2.5 GHz
- IF input power = -40 dBm

RF GAIN CONTROL

To adjust the RF gain control on either the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ evaluation board, take the following steps:

1. Connect a power supply to the RF_GAIN_TP test point and one ground test point on the ADMV4530IQ-EVALZ or ADMV4530IF-EVALZ evaluation board. Alternatively, the power supply can be connected to the RF_GAIN SMA port. The power supply current limit must be set to 1 mA.
2. Adjust the power supply voltage as desired from 0 V to 1.8 V. The maximum gain corresponds to 1.8 V, and the minimum gain corresponds to 0 V. Refer to the [ADMV4530](#) data sheet for more information regarding gain performance.

IF GAIN CONTROL

To adjust the IF gain control on ADMV4530IF-EVALZ evaluation board, take the following steps:

1. Connect a power supply to the IF_GAIN_TP test point and one ground test point on the ADMV4530IF-EVALZ evaluation board. Alternatively, the power supply can be connected to the IF_GAIN SMA port. The power supply current limit must be set to 1 mA.
2. Adjust the power supply voltage as desired from 0 V to 3.3 V. The maximum gain corresponds to 0 V, and the minimum gain corresponds to 3.3 V. Refer to the [ADMV4530](#) data sheet for more information regarding gain performance.

AUTOMATED CHIP RESET

If a reset of the [ADMV4530](#) chip is required on the ADMV4530IQ-EVALZ or ADMV4530IF-EVALZ evaluation board, it is recommended to use the automated reset sequence. Click **Reset Chip** (see Figure 9, Label K3 and Table 1 for additional information). This automated sequence performs the following actions:

- Toggles all **SDP-S** general-purpose input/outputs (GPIOs) to a low state, which sets both the $\overline{\text{RST}}$ and PD pins of the [ADMV4530](#) low.
- Toggles the $\overline{\text{RST}}$ pin high to bring the [ADMV4530](#) chip back to the normal operating state.
- Programs Register 0x00 to 0x81, which also resets the [ADMV4530](#). This step covers legacy boards that did not have the $\overline{\text{RST}}$ pin connected.
- Programs Register 0x00 to 0x18 to enable the SDO pin on the [ADMV4530](#).
- Programs the recommended mixer settings for IF mode.

- Programs the PLL for a 28 GHz LO frequency anticipating a 200 MHz reference input frequency.
- Reads back the register settings of the [ADMV4530](#).

MANUAL CHIP RESET

For manual reset operations, the following outlines various ways to perform a reset.

- There is a reset button (S1) on the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ evaluation board. Pressing this button pulls the $\overline{\text{RST}}$ pin low to initiate a reset to the factory power-up state.
- The $\overline{\text{RST}}$ pin can also be pulled low from within the [ACE](#) software by using the dropdown menu in the lower left corner of Figure 9 (see Label G). When using this option, be sure to return the dropdown menu back to **Normal Operation** after resetting the device.
- Register 0x00 can be programmed to 0x81 to initiate a reset of the [ADMV4530](#).

Regardless of the manual reset option used, it is recommended to perform the following after the device resets:

- Program Register 0x00 to 0x18 to enable the SDO pin on the [ADMV4530](#).
- Read back all registers on the [ADMV4530](#).

LOSS OF BOARD COMMUNICATION

When the [ADMV4530](#) is turned off and then on, or if the USB cable is unplugged and plugged back in while the [ACE](#) software is open, communication with the [ADMV4530](#) may be lost. To regain communication, click the **System** tab, click the USB symbol in the **SDP-S Controller** subsystem, and then click **Acquire**. If this step does not work, restart the [ACE](#) software to reinitiate communication with the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ evaluation board.

REGULATOR BYPASS

Both the ADMV4530IQ-EVALZ and the ADMV4530IF-EVALZ evaluation boards have voltage regulators that allow the user to operate these evaluation boards from a single 5 V dc power supply. The on-board voltage regulators supply several bias voltages to the various supply pins on the chip. If desired, these voltage regulators can be bypassed by removing the 0 Ω registers (R25 to R28) from the ADMV4530IQ-EVALZ or the ADMV4530IF-EVALZ evaluation board and then by injecting each voltage independently by using the corresponding test points. See the schematics for details (see Figure 13 and Figure 19).

EVALUATION BOARD SCHEMATICS AND ARTWORK

ADMV4530IQ-EVALZ

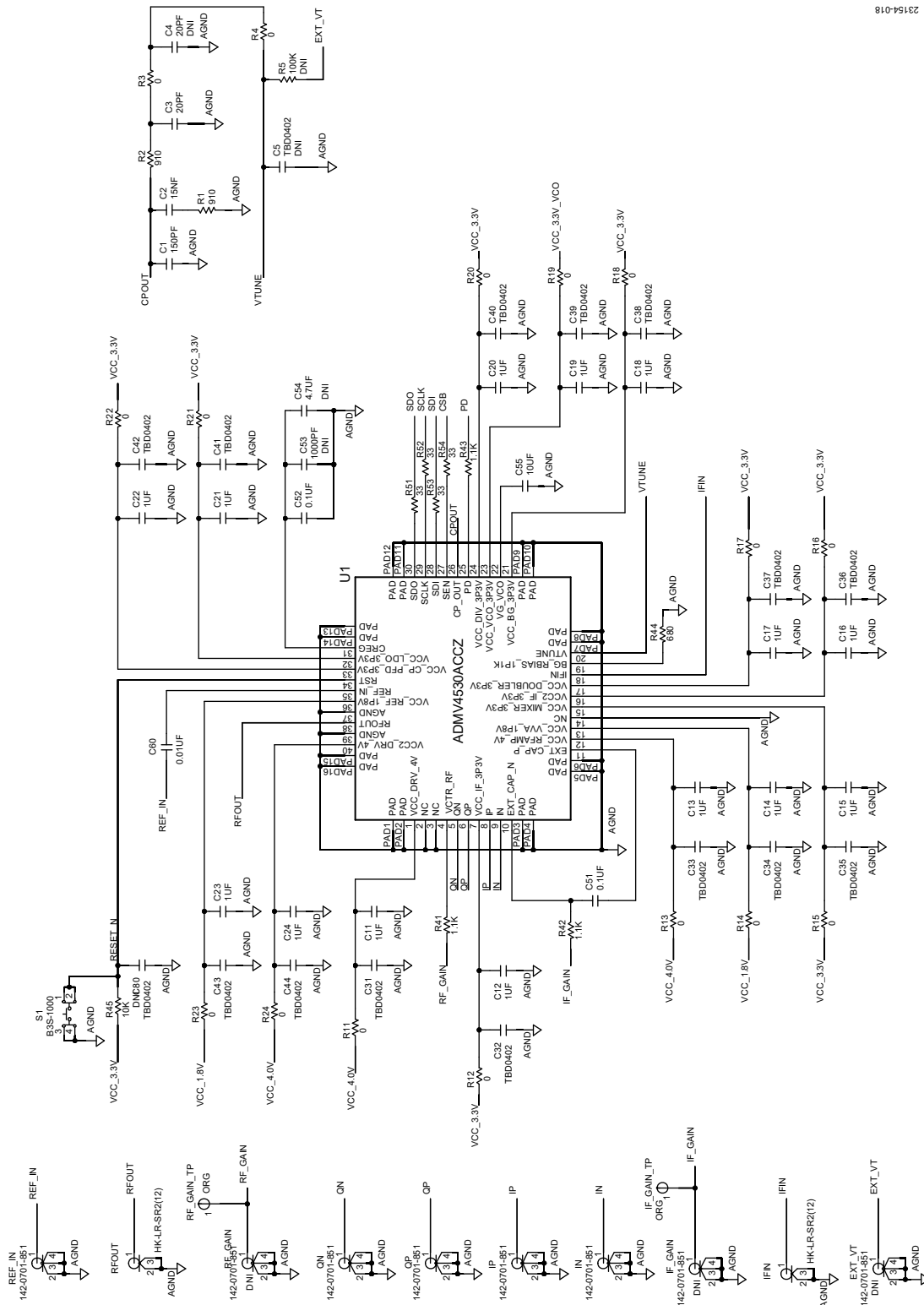


Figure 12. ADMV4530IQ-EVALZ Evaluation Board Schematic, Page 1

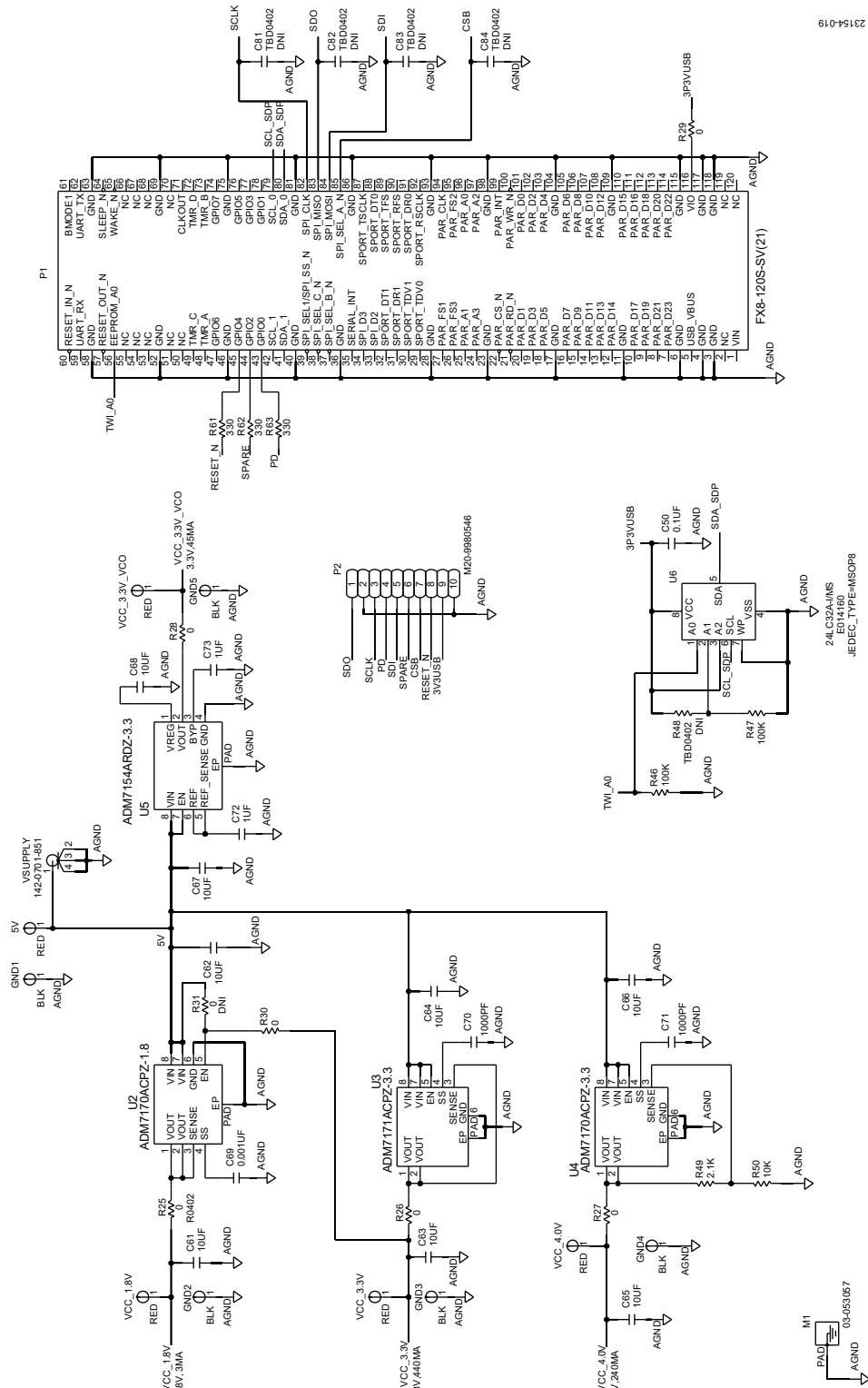


Figure 13. ADMV4530IQ-EVALZ Evaluation Board Schematic, Page 2

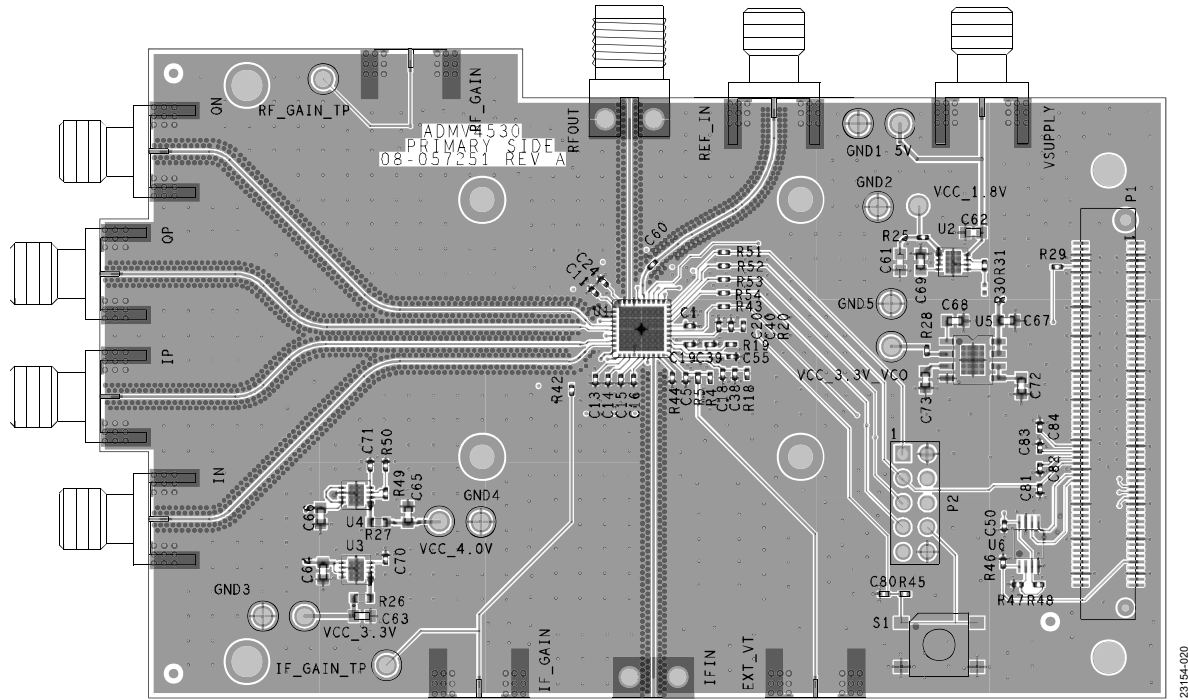


Figure 14. ADMV4530IQ-EVALZ Evaluation Board Layer 1

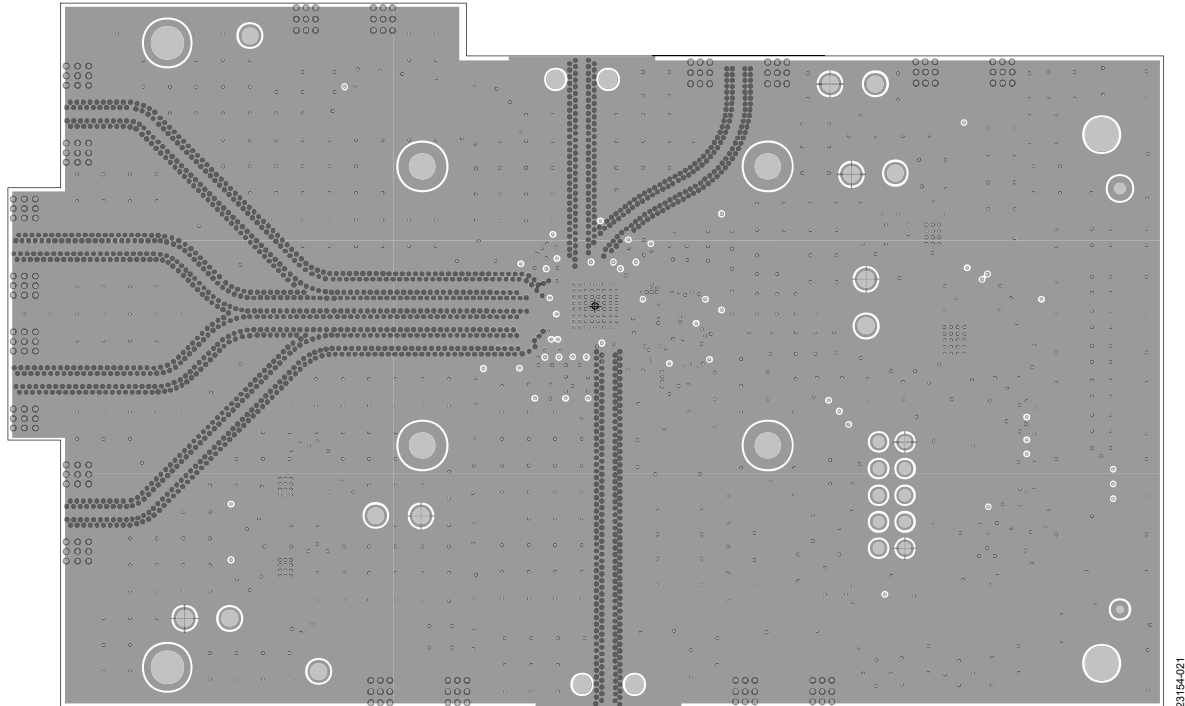
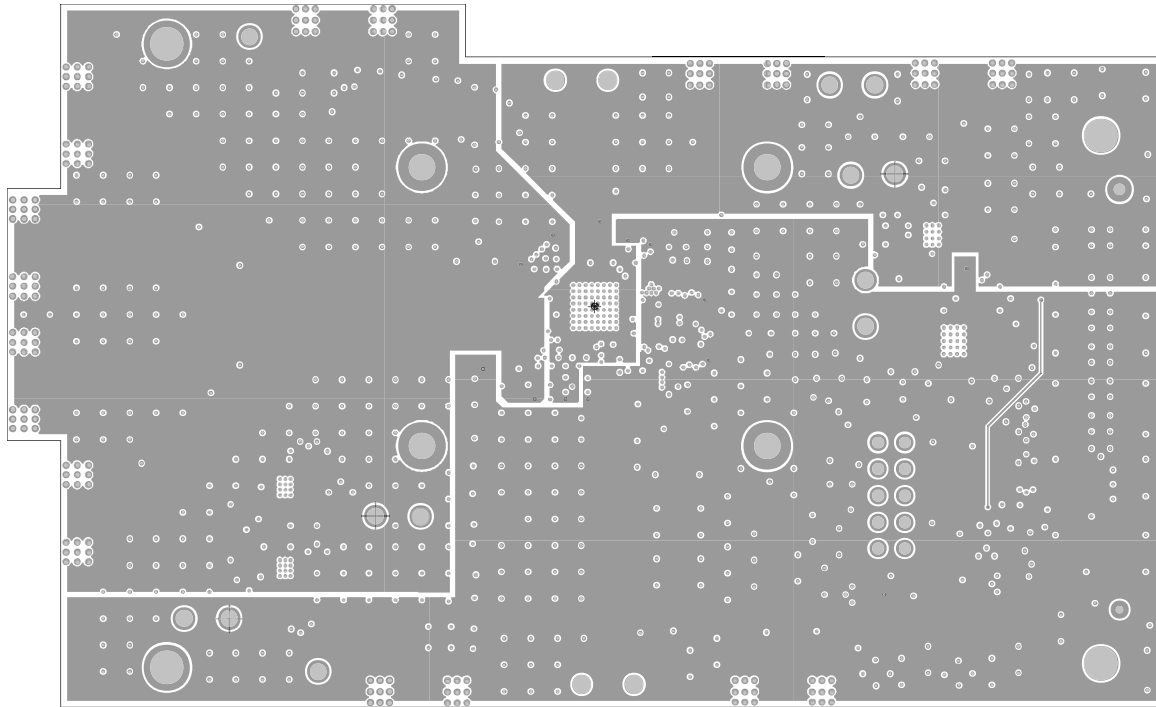
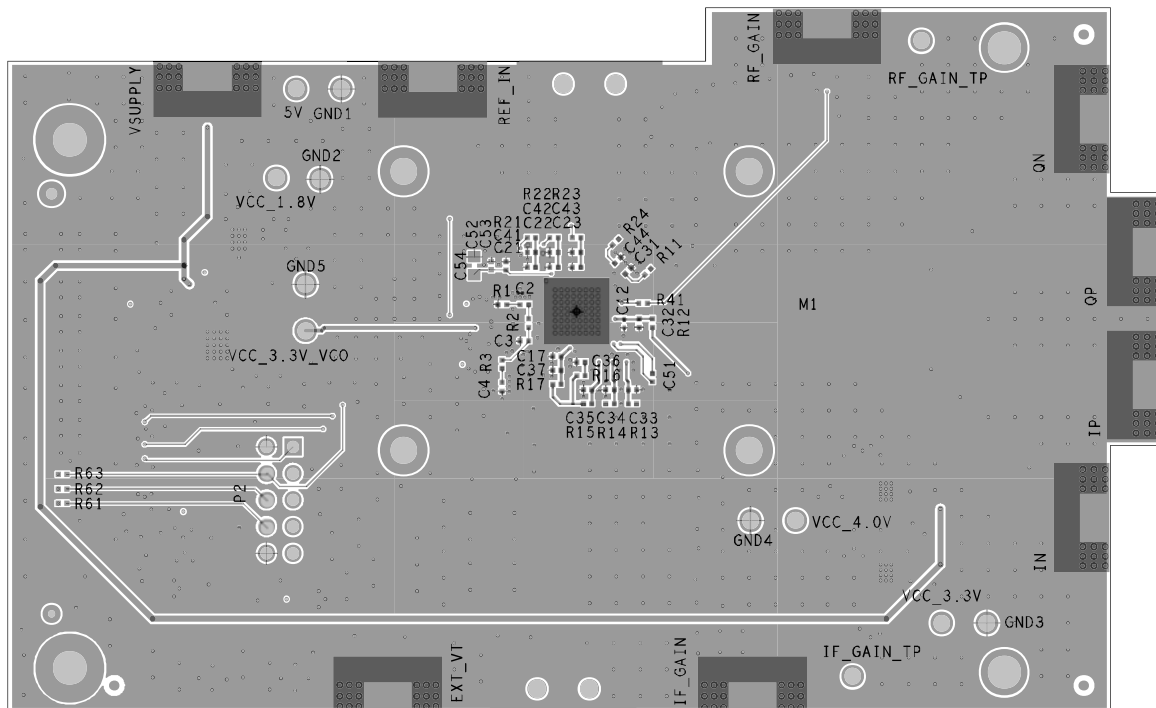


Figure 15. ADMV4530IQ-EVALZ Evaluation Board Layer 2



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Figure 16. ADMV4530IQ-EVALZ Evaluation Board Layer 3



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Figure 17. ADMV4530IQ-EVALZ Evaluation Board Layer 4

ADMV4530IF-EVALZ

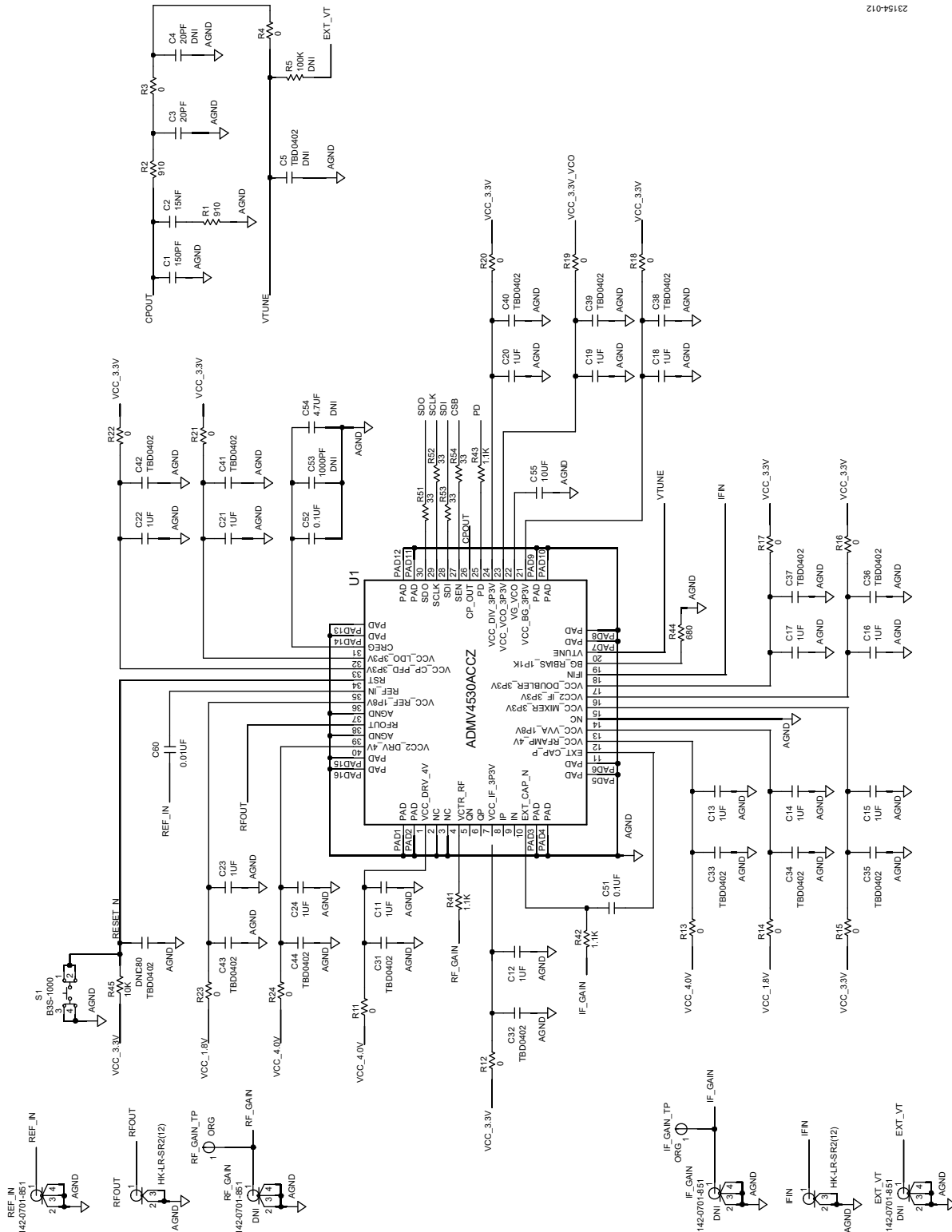


Figure 18. ADMV4530IF-EVALZ Evaluation Board Schematic, Page 1

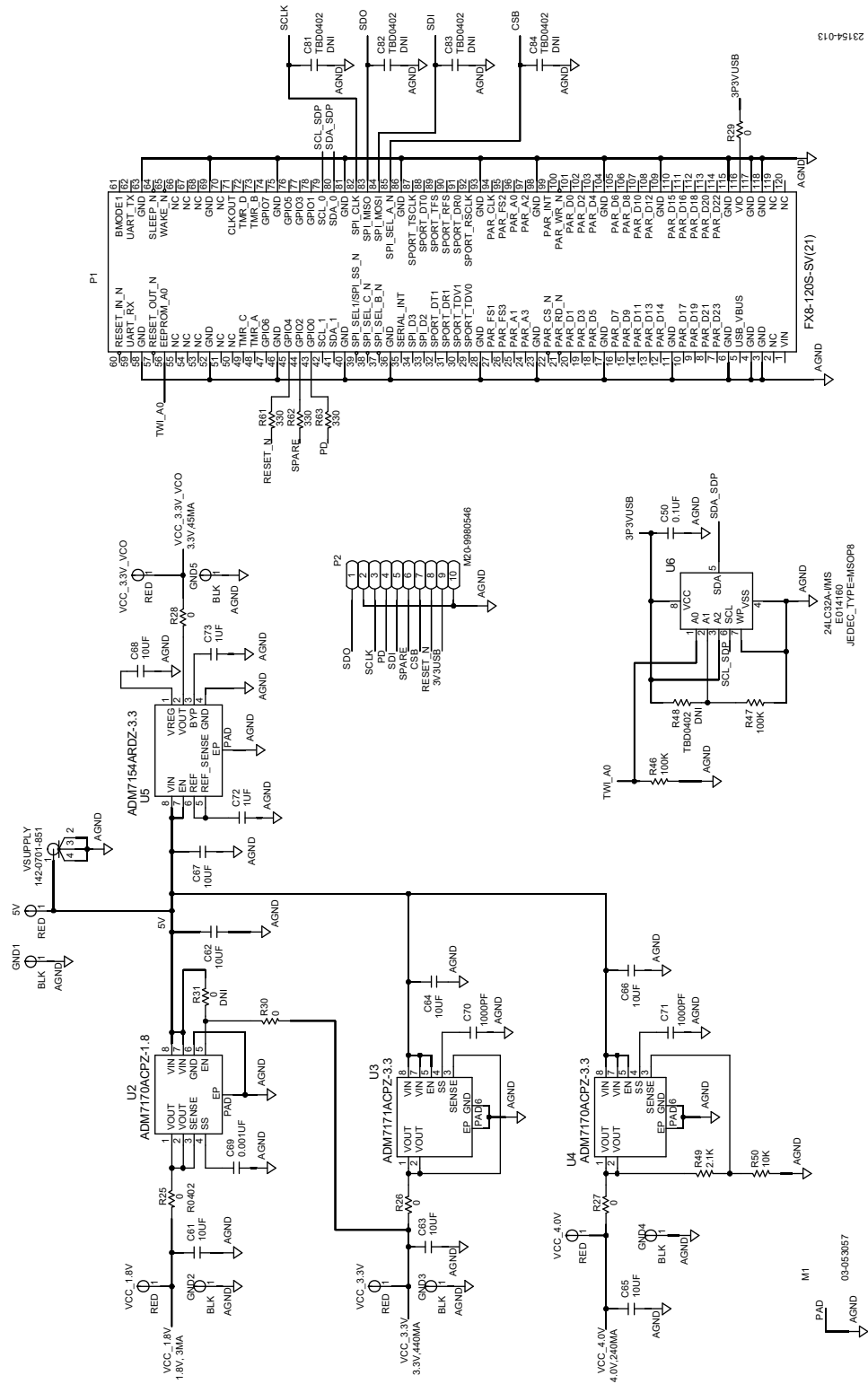


Figure 19. ADMV4530IF-EVALZ Evaluation Board Schematic, Page 2

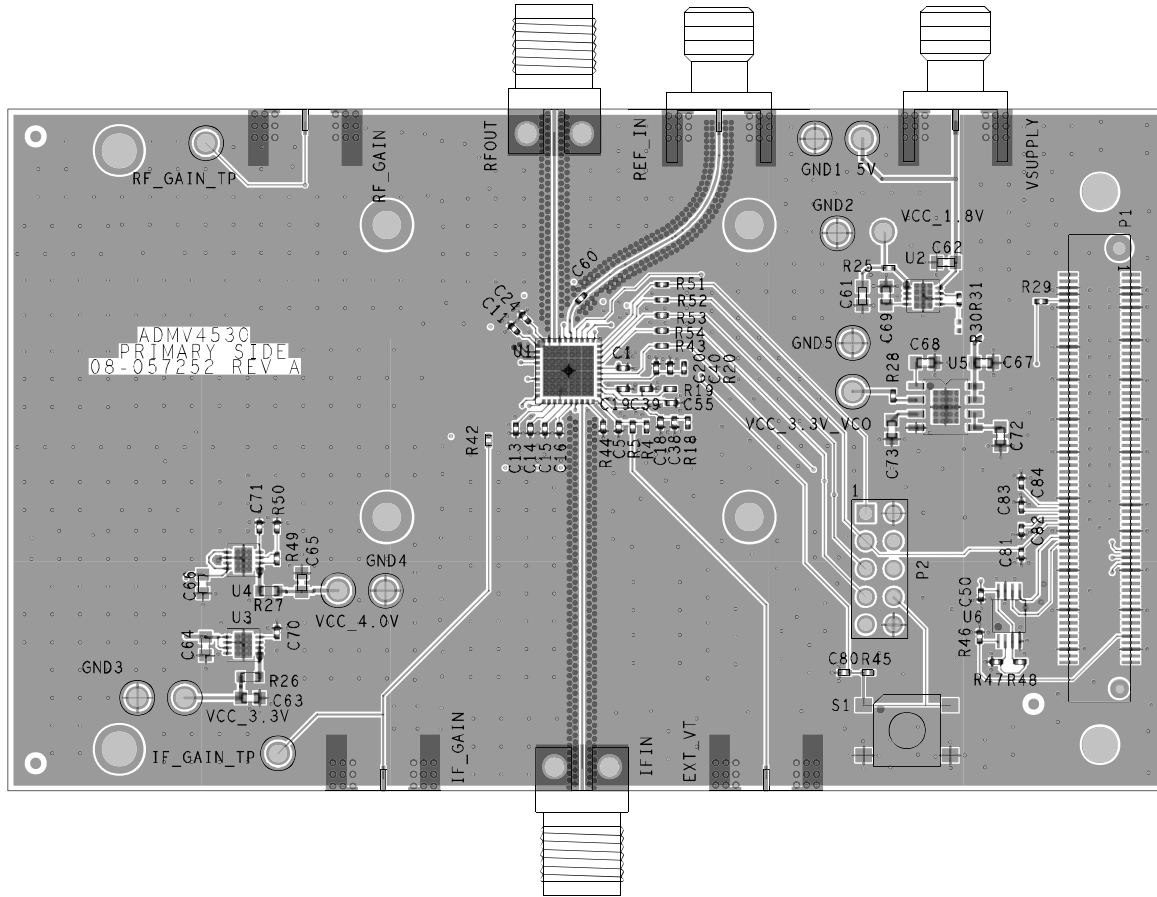


Figure 20. ADMV4530IF-EVALZ Evaluation Board Layer 1

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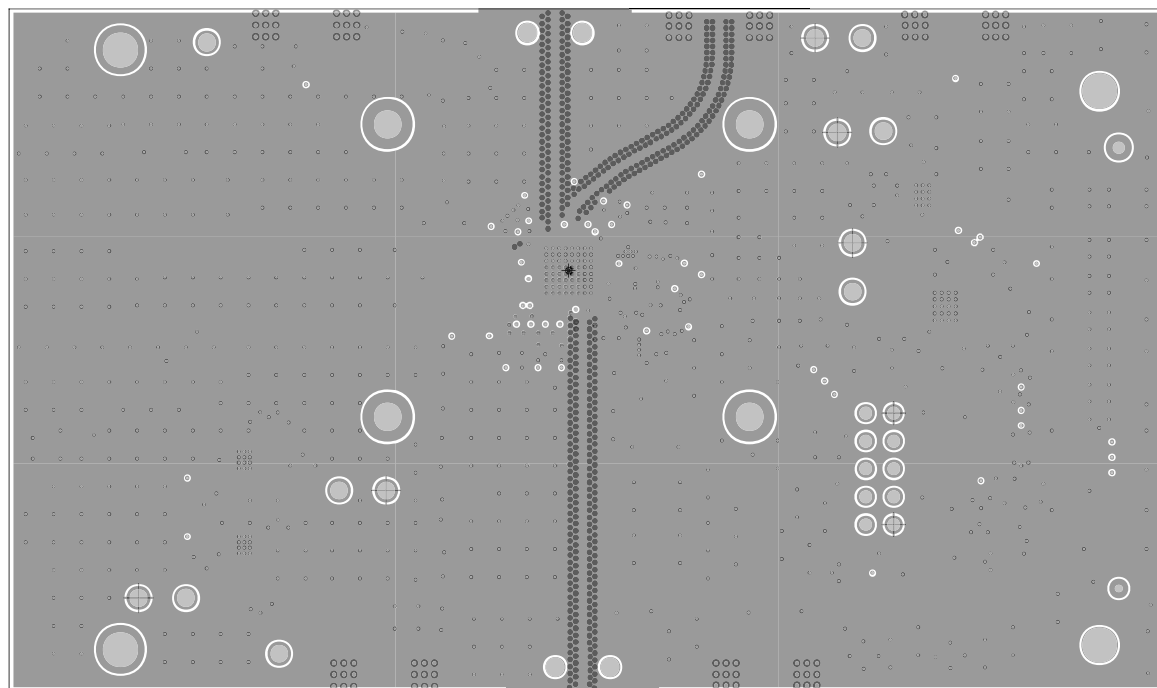


Figure 21. ADMV4530IF-EVALZ Evaluation Board Layer 2

23154-015

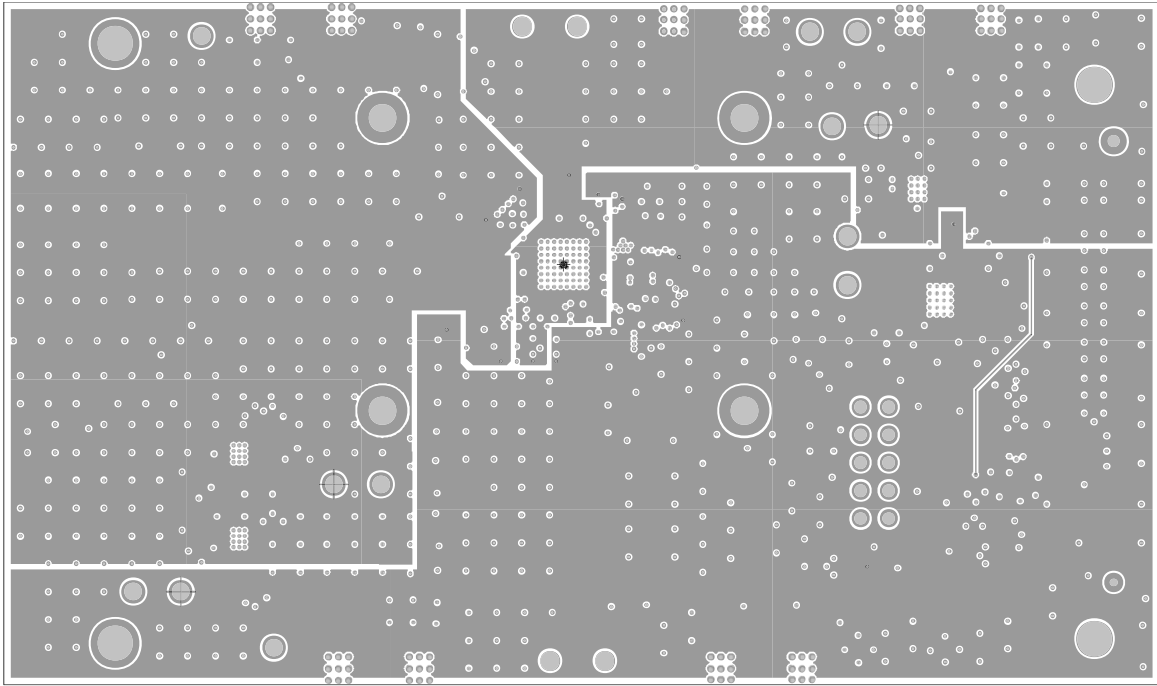


Figure 22. ADMV4530IF-EVALZ Evaluation Board Layer 3

23154-016

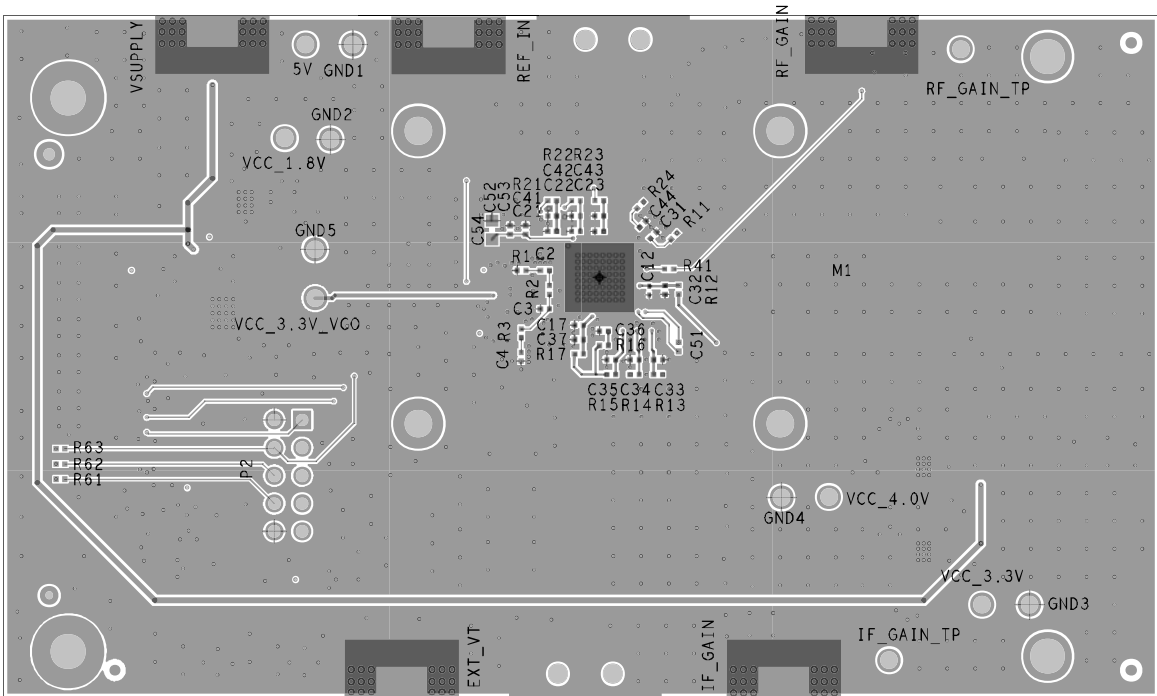


Figure 23. ADMV4530IF-EVALZ Evaluation Board Layer 4

23154-017

ORDERING INFORMATION

BILL OF MATERIALS

The ADMV4530IQ-EVALZ bill of materials is identical to the ADMV4530IF-EVALZ except for one row (see Note 1 of Table 2).

Table 2. ADMV4530IQ-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
5	5V, VCC_1.8V, VCC_3.3V, VCC_3.3V_VCO, VCC_4.0V	Test points, red	Components Corporation	TP-104-01-02
1	C1	Capacitor, 150 pF, 50 V, 5%, 0402	Murata	GRM1555C1H151JA01D
14	C11 to C24	Capacitors, 1 μF, 16 V, 10%, 0402	Yageo	CC0402KRX5R7BB105
1	C2	Capacitor, 15 nF, 35 V, 10%, 0402	TDK	CGA2B3X7R1V153K050BB
1	C3	Capacitor, 20 pF, 16 V, 5%, 0402	AVX Corporation	0402YA200JAT2A
3	C50 to C52	Capacitors, 0.1 μF, 16 V, 10%, 0402	Kemet	C0402C104K4RACTU
1	C55	Capacitor, 10 μF, 6.3 V, 20%, 0402	Samsung	CL05A106MQ5NUNC
1	C60	Capacitor, 0.01 μF, 50 V, 10%, 0402	Murata	GCM155R71H103KA55D
8	C61 to C68	Capacitors, 10 μF, 16 V, 10%, 0603	Murata	GRM188R61C106KAALD
1	C69	Capacitor, 1 nF, 50 V, 5%, 0603	Murata	GRM1885C1H102JA01D
2	C70, C71	Capacitors, 1 nF, 50 V, 5%, 0402	Murata	GRM1555C1H102JA01
2	C72, C73	Capacitors, 1 μF, 16 V, 10%, 0603	TDK	CGA3E1X7R1C105K080AC
5	GND1 to GND5	Test points, black	Components Corporation	TP-104-01-00
1	RFOUT	Connector, 2.92 mm, 40 GHz	Hirose Electric Co.	HK-LR-SR2(12)
2	IF_GAIN_TP, RF_GAIN_TP	Test points, orange	Components Corporation	TP-104-01-03
6	IN, IP, QN, QP, REF_IN, VSUPPLY ¹	Connectors, edge launch, SMA	Cinch Connectivity	142-0701-851
1	P1	Connector, vertical, surface-mount technology (SMT), 120-pin	Hirose Electric Co.	FX8-120S-SV(21)
1	P2	Connector, vertical, header, 10-pin	Harwin Inc.	M20-9980546
2	R1, R2	Resistors, 910 Ω, 1/16 W, 0.1%, 0402	Panasonic	ERA-2AEB911X
20	R3, R4, R11 to R25, R28 to R30	Resistors, 0 Ω, 1/10 W, 0402	Panasonic	ERJ-2GE0R00X
2	R26, R27	Resistors, 0 Ω, 1/10 W, 0603	Panasonic	ERJ-3GEY0R00V
3	R41 to R43	Resistors, 1.1 kΩ, 1/16 W, 1%, 0402	Yageo	RC0402FR-071K1L
1	R44	Resistor, 680 Ω, 1/16 W, 0.1%, 0402	Panasonic	ERA-2ARB681X
2	R45, R50	Resistors, 10 kΩ, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF1002X
2	R46, R47	Resistors, 100 kΩ, 1/16 W, 1%, 0402	Panasonic	ERJ-2RKF1003X
1	R49	Resistor, 2.1 kΩ, 1/16 W, 1%, 0402	Panasonic	ERJ-2RKF2101X
4	R51 to R54	Resistors, 33 Ω, 1/10 W, 5%, 0402	Panasonic	ERJ-2GEJ330X
3	R61 to R63	Resistors, 330 Ω, 1/16 W, 5%, 0402	Panasonic	ERJ-2GEJ331X
1	S1	Switch, mechanical, push button	Omron Electronics Inc.	B3S1000
1	U1	IC, Ka band upconverter	Analog Devices	ADMV4530ACCZ
1	U2	IC, LDO regulator, 1.8 V	Analog Devices	ADM7170ACPZ-1.8-R7
1	U3	IC, LDO regulator, 3.3 V	Analog Devices	ADM7171ACPZ-3.3-R7
1	U4	IC, LDO regulator, 3.3 V	Analog Devices	ADM7170ACPZ-3.3-R7
1	U5	IC, LDO regulator, 3.3 V	Analog Devices	ADM7154ARDZ-3.3-R7
1	U6	IC, 24LC32A, EEPROM, I ² C	Microchip Technology	24LC32A-I/MS
20	C5, C31 to C44, C80 to C84	Capacitors, 0402, do not install (DNI)	Not applicable	Not applicable
1	C4	Capacitor, 20 pF, 16 V, 5%, 0402, DNI	AVX Corporation	0402YA200JAT2A
1	C53	Capacitor, 1 nF, 50 V, 5%, 0402, DNI	Murata	GRM1555C1H102JA01
1	C54	Capacitor, 4.7 μF, 16 V, 10%, 0603, DNI	TDK	C1608X5R1C475K080AC
3	EXT_VT, IF_GAIN, RF_GAIN	Connectors, edge launch, SMA, DNI	Cinch Connectivity	142-0701-851
1	R31	Resistor, 0 Ω, 1/10 W, 0402, DNI	Panasonic	ERJ-2GE0R00X
1	R48	Resistor, 0402, DNI	Not applicable	Not applicable
1	R5	Resistor, 100 kΩ, 1/16 W, 0402, DNI	Panasonic	ERJ-2RKF1003X

¹ For the ADMV4530IF-EVALZ, only REF_IN and VSUPPLY are applicable for this row.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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