CIPOS™ Mini

IFCM15S60GD/IFCM15S60GS

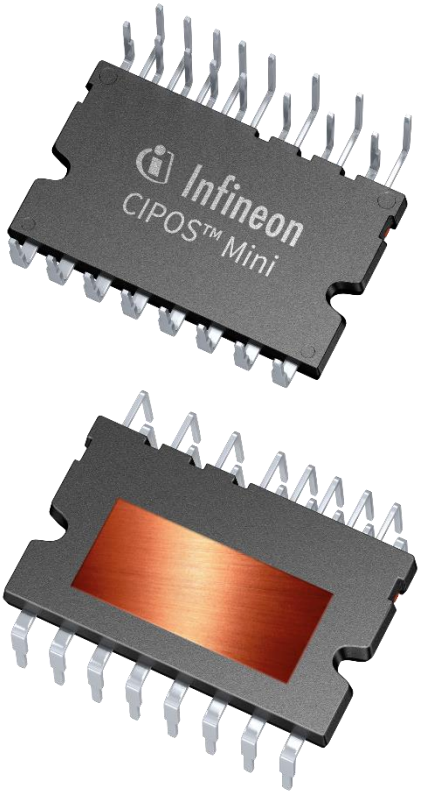
Description

The CIPOS™ Mini family offers the chance for integrating various power and control components of inverter and single boost PFC stages to increase reliability and optimize PCB size and system cost. It is designed to control three-phase motors in variable speed drives for applications such as air-conditioners and pumps. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also less EMI and overload protection. To deliver excellent electrical performance, the CIPOS™ Mini family incorporated Infineon's leading-edge TRENCHSTOP™ IGBTs, anti-parallel diodes, and an optimized SOI gate driver for three-phase inverter stage, and a TRENCHSTOP™ IGBT and a rapid switching emitter controlled diode for single boost PFC stage.

Features

Package

- Fully isolated dual in-line molded module
- Very low thermal resistance due to DCB substrate
- Lead-free terminal plating; RoHS compliant



Inverter

- TRENCHSTOP™ IGBTs for inverter
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative V_S potential up to -11 V for signal transmission at V_{BS} = 15 V
- Integrated bootstrap functionality
- Over-current shutdown
- Built-in NTC thermistor for temperature monitor
- Under-voltage lockout at all channels
- Low-side common emitter
- Cross-conduction prevention
- All of 6 switches turn off during protection

PFC

- TRENCHSTOP™ IGBT for PFC
- Rapid switching emitter controlled diode

Potential applications

- Air-conditioners, fans, pumps, low power motor drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table 1 Product Information

Base Part Number	Package Type	Standard Pack		Remarks
		Form	MOQ	
IFCM15S60GD	DIP 36x21D	14 pcs / Tube	280 pcs	
IFCM15S60GS	DIP 36x21D	14 pcs / Tube	280 pcs	Extended stand-off

Table of Contents

1 Internal Electrical Schematic

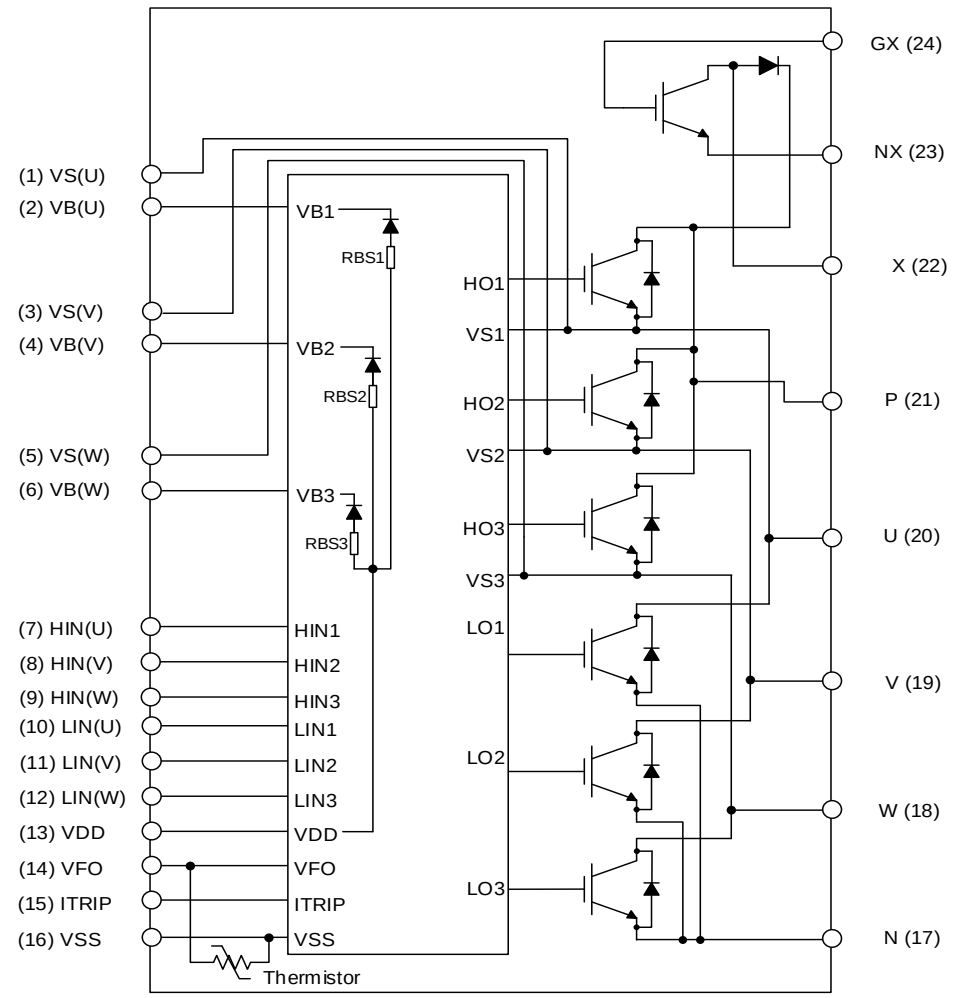


Figure 1 Internal electrical schematic

2 Pin Description

2.1 Pin Assignment

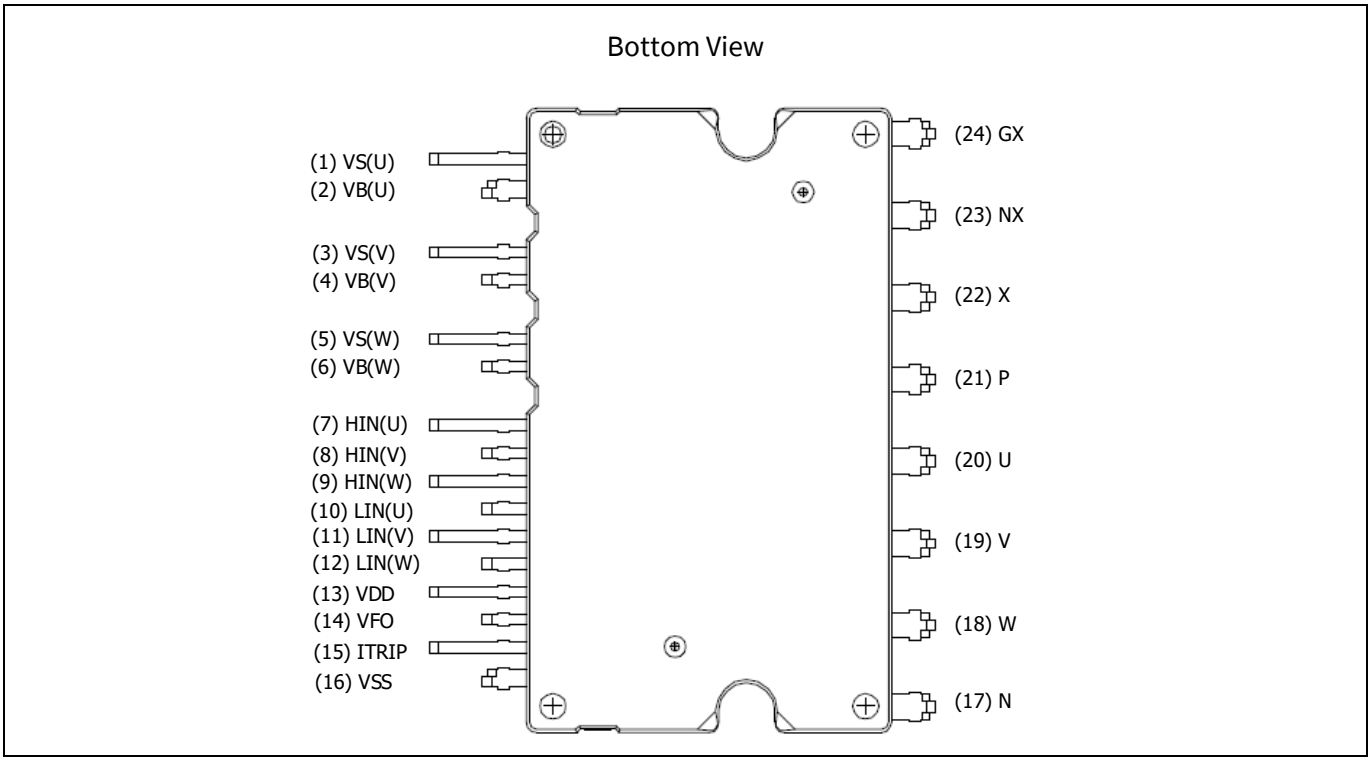


Figure 2 Pin configuration

Table 2 Pin assignment

Pin Number	Pin name	Pin Description
1	V_S(U)	U-phase high-side floating IC supply offset voltage
2	V_B(U)	U-phase high-side floating IC supply voltage
3	V_S(V)	V-phase high-side floating IC supply offset voltage
4	V_B(V)	V-phase high-side floating IC supply voltage
5	V_S(W)	W-phase high-side floating IC supply offset voltage
6	V_B(W)	W-phase high-side floating IC supply voltage
7	HIN(U)	U-phase high-side gate driver input
8	HIN(V)	V-phase high-side gate driver input
9	HIN(W)	W-phase high-side gate driver input
10	LIN(U)	U-phase low-side gate driver input
11	LIN(V)	V-phase low-side gate driver input
12	LIN(W)	W-phase low-side gate driver input
13	V_{DD}	Low-side control supply
14	V_{FO}	Fault output / temperature monitor
15	ITRIP	Over-current shutdown input
16	V_{SS}	Low-side control negative supply
17	N	Low-side emitter

Pin Description

Pin Number	Pin name	Pin Description
18	W	Motor W-phase output
19	V	Motor V-phase output
20	U	Motor U-phase output
21	P	Positive output voltage / positive bus input voltage
22	X	PFC IGBT collector
23	NX	PFC IGBT emitter
24	GX	PFC IGBT gate

2.2 Pin Description

HIN(U, V, W) and LIN(U, V, W) (Low-side and high-side control pins, Pin 7 - 12)

These pins are positive logic and they are responsible for the control of the integrated IGBTs. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. A pull-down resistor of about 5 kΩ is internally provided to pre-bias input during supply start-up, and a zener clamp is provided to protect the pin. Input Schmitt-trigger and noise filter provide noise rejection to short input pulses.

The noise filter suppresses control pulses shoter than the filter time $t_{FIL,IN}$. The Figure 4 describes how the filter works. An input pulse-width shorter than 1 µs is not recommended.

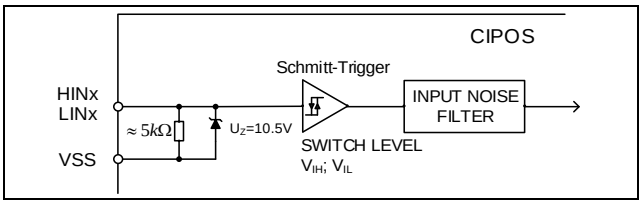


Figure 3 Input pin structure

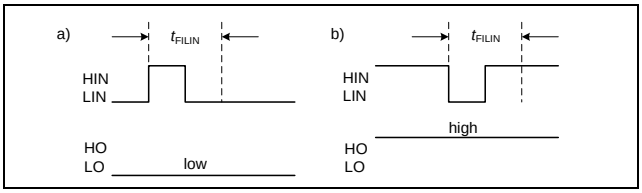


Figure 4 Input filter timing diagram

The integrated gate driver additionally provides a shoot-through prevention capability that avoids the simultaneous on-states of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When both inputs of the same leg are activated, only formerly activated one is remained activated so that the leg is kept steadily in a safe state.
A minimum deadtime insertion of typically 380 ns is also provided by driver, in order to reduce cross-conduction of the IGBTs.

V_{FO} (Fault-output and NTC, Pin 14)

The V_{FO} pin indicates a module failure in case of under-voltage at pin V_{DD} or in case of triggered over-current detection at ITRIP. The same pin provides direct access to the NTC, which is referenced to V_{SS}. An external pull-up resistor is required to bias the NTC.

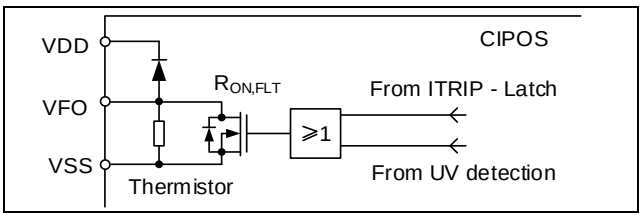


Figure 5 Internal circuit at pin V_{FO}

ITRIP (Over-current detection function, Pin 15)

The CIPOS™ Mini family provides an over-current detection function by connecting the ITRIP input with the IGBT current feedback. The ITRIP comparator threshold (typ. 0.47 V) is referenced to V_{SS}. An input noise filter ($t_{ITRIPMIN}$ = typ. 530 ns) prevents the driver to detect false over-current events.
Over-current detection generates a shutdown of outputs of the gate driver after the shuntdown propagation delay of typically 1000 ns. The fault-clear time is set to minimum 40 µs.

Pin Description

V_{DD}, V_{SS} (Low-side control supply and reference, Pin 13, 16)

V_{DD} is the control supply and it provides power both to input logic and to output stage. Input logic is referenced to V_{SS} ground.
The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 12.1 V is present.
The gate driver shuts down all the outputs, when the V_{DD} supply voltage is below V_{DDUV-} = 10.4 V. This prevents the IGBTs from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

V_B(U, V, W) and V_S(U, V, W) (High-side supplies, Pin 1 - 6)

V_B to V_S is the high-side supply voltage. The high-side circuit can float with respect to V_{SS} following the high-side IGBT emitter voltage.
Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.
The under-voltage detection operates with a rising supply threshold of typical V_{BSUV+} = 12.1 V and a falling threshold of V_{BSUV-} = 10.4 V.

V_S(U, V, W) provide a high robustness against negative voltage in respect of V_{SS} of -50 V transiently. This ensures very stable designs even under harsh conditions.

N (Low-side emitter, Pin 17)

The low-side common emitter is available for current measurement. It is recommended to keep the connection to pin V_{SS} as short as possible to avoid unnecessary inductive voltage drops.

W, V, U (High-side emitter and low-side collector, Pin 18 - 20)

These pins are connected to motor U, V, W input pins.

P (Positive bus input voltage, Pin 21)

The high-side IGBTs and PFC diode cathode are connected to the bus voltage. It is noted that the bus voltage does not exceed 450 V.

X, NX, GX (Single boost PFC, Pins 22-24)

These pins are collector, emitter, and gate of IGBT for single boost PFC stage.

3 Absolute Maximum Ratings

(V_{DD} = 15 V, V_{GE} = 15 V and T_J = 25°C, if not stated otherwise)

3.1 Module Section

Description	Symbol	Condition	Value	Unit
Storage temperature range	T_{STG}		-40 ~ 125	°C
Operating case temperature	T_C	Refer to Figure 7	-40 ~ 125	°C
Operating junction temperature	T_J		-40 ~ 150	°C
Isolation test voltage	V_{ISO}	1 min, RMS, f = 60 Hz	2000	V

3.2 Inverter Section

Description	Symbol	Condition	Value	Unit
Max. blocking voltage	V_{CES}	I_C = 250 µA	600	V
DC link supply voltage of P-N	V_{PN}	Applied between P-N	450	V
DC link supply voltage (surge) of P-N	$V_{PN(surge)}$	Applied between P-N	500	V
Output current	I_C	T_C = 25°C, T_J < 150°C	±15	A
Peak output current	$I_{C(peak)}$	T_C = 25°C, T_J < 150°C less than 1 ms	±30	A
Power dissipation per IGBT	P_{tot}		49.8	W
Short circuit withstand time[1]	t_{SC}	V_{DC} ≤ 400 V, T_J = 150°C	5	µs

3.3 Control Section

Description	Symbol	Condition	Value	Unit
High-side offset voltage	V_S		600	V
Repetitive peak reverse voltage of bootstrap diode	V_{RRM}		600	V
Module supply voltage	V_{DD}		-1 ~ 20	V
High-side floating supply voltage	V_{BS}	V_B reference to V_S	-1 ~ 20	V
Input voltage	V_{IN}	LIN, HIN, ITRIP	-1 ~ 10	V

[1] Allowed number of short circuits: < 1000; time between short circuits: > 1 s.

3.4 PFC Section

Description	Symbol	Condition	Value	Unit
Max. blocking voltage	V_{CES}	V_{GE} = 0 V, I_C = 250 µA	650	V
Gate-emitter voltage	V_{GE}		±20	V
Continuous collector current	I_C	T_C = 25°C, T_J < 150°C	30	A
Maximum peak collector current	$I_{C(peak)}$	T_C = 25°C, T_J < 150°C less than 1 ms	60	A
Power dissipation	P_{tot}	PFC IGBT	105.9	W
Short circuit withstand time[1]	t_{SC}	V_{DC} ≤ 400 V, T_J = 150°C	5	µs
Diode forward current	I_F	T_C = 25°C, T_J ≤ 150°C	20	A
		T_C = 80°C, T_J ≤ 150°C	15	
Diode pulsed current	$I_{F(peak)}$	T_C = 25°C , T_J ≤ 150°C	40	A
Diode non repetitive surge forward current	I_{FSM}	T_C = 25°C, t_p = 10 ms, sine half-wave	110	A

[1] Allowed number of short circuits: < 1000; time between short circuits: > 1 s.

4 Thermal Characteristics

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Single IGBT thermal resistance, junction-case	R_{thJC}	Inverter			2.51	K/W
Single diode thermal resistance, junction-case	$R_{thJC,D}$	Inverter			4.67	K/W
Single IGBT thermal resistance, junction-case	R_{thJC}	PFC			1.18	K/W
Single diode thermal resistance, junction-case	$R_{thJC,D}$	PFC			2.76	K/W

5 Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

Description	Symbol	Value			Unit
		Min.	Typ.	Max.	
DC link supply voltage of P-N	V_{PN}	0	-	450	V
Low-side supply voltage	V_{DD}	14.5	16	18.5	V
High-side floating supply voltage (V_B vs. V_S)	V_{BS}	13.5	-	18.5	V
Logic input voltages LIN, HIN, ITRIP	V_{IN} V_{ITRIP}	0	-	5	V
Inverter PWM carrier frequency	f_{PWM}	-	-	20	kHz
PFC switching frequency	$f_{PWM(PFC)}$	-	-	40	kHz
External deadtime between HIN and LIN	DT	1.5	-	-	µs
Voltage between V_{SS} – N and NX (including surge)	V_{COMP}	-5	-	5	V
Minimum input pulse width	$PW_{IN(ON)}$ $PW_{IN(OFF)}$	1	-	-	µs
Control supply variation	ΔV_{BS}, ΔV_{DD}	-1	- -	1	V/µs
PFC IGBT gate-emitter voltage	V_{GE}	14	-	18	V
PFC IGBT external gate parameters	R_G	-	10	-	Ω
	C_{GE}	-	4.7	-	nF
	R_{GE}	-	10	-	kΩ

6 Static Parameters

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

6.1 Inverter Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter voltage	$V_{CE(Sat)}$	I_C = 10 A, T_J = 25°C I_C = 10 A, T_J = 150°C	- -	1.55 1.8	2.05 -	V
Collector-emitter leakage current	I_{CES}	V_{CE} = 600 V	-	-	1	mA
Diode forward voltage	V_F	I_F = 10 A, T_J = 25°C I_F = 10 A, T_J = 150°C	- -	1.75 1.8	2.45 -	V

6.2 Control Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Logic "1" input voltage (LIN, HIN)	V_{IH}		-	2.1	2.5	V
Logic "0" input voltage (LIN, HIN)	V_{IL}		0.7	0.9	-	V
ITRIP positive going threshold	$V_{IT,TH+}$		400	470	540	mV
ITRIP input hysteresis	$V_{IT,HYS}$		40	70	-	mV
V_{DD} and V_{BS} supply under-voltage positive going threshold	V_{DDUV+} V_{BSUV+}		10.8	12.1	13.0	V
V_{DD} and V_{BS} supply under-voltage negative going threshold	V_{DDUV-} V_{BSUV-}		9.5	10.4	11.2	V
V_{DD} and V_{BS} supply under-voltage lockout hysteresis	V_{DDUVH} V_{BSUVH}		1.0	1.7	-	V
Quiescent V_{Bx} supply current (V_{Bx} only)	I_{QBS}	HIN = 0 V	-	300	500	µA
Quiescent V_{DD} supply current (V_{DD} only)	I_{QDD}	LIN = 0 V, HIN = 5 V	-	370	900	µA
Input bias current for LIN, HIN	I_{IN+}	V_{IN} = 5 V	-	1	1.5	mA
	I_{IN-}	V_{IN} = 0 V	-	2	-	µA
Input bias current for ITRIP	I_{ITRIP+}	V_{ITRIP} = 5 V	-	65	150	µA
Input bias current for V_{FO}	I_{FO}	V_{FO} = 5 V, V_{ITRIP} = 0 V	-	60	-	µA
V_{FO} output voltage	V_{FO}	I_{FO} = 10 mA, V_{ITRIP} = 1 V	-	0.5	-	V
Bootstrap diode forward voltage	V_{F_BSD}	I_F = 0.5 mA	-	1	-	V
Bootstrap resistance	R_{BSD}	Between V_F = 4 V, V_F = 5 V	-	40	-	Ω

6.3 PFC Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter voltage	$V_{CE(Sat)}$	I_C = 30 A, V_{GE} = 15 V, T_J = 25°C I_C = 30 A, V_{GE} = 15 V, T_J = 150°C	- -	2.0 2.55	2.4 -	V
Collector-emitter leakage current	I_{CES}	V_{CE} = 600 V	-	-	1	mA
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C = 0.43 mA, V_{GE} = V_{CE}	4.1	5.1	5.7	V
Gate-emitter leakage current	I_{GES}	V_{CE} = 0 V, V_{GE} = 20 V	-	-	1	µA
Diode forward voltage	V_F	I_F = 30 A, T_J = 25°C I_F = 30 A, T_J = 150°C	- -	1.75 1.65	2.3 -	V
Diode reverse leakage current	I_R	V_R = 650 V	-	-	1	mA

7 Dynamic Parameters

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

7.1 Inverter Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Turn-on propagation delay time	t_{on}	$V_{LIN, HIN}$ = 5 V, I_C = 10 A, V_{DC} = 300 V	-	680	-	ns
Turn-on rise time	t_r		-	30	-	ns
Turn-on switching time	$t_{c(on)}$		-	220	-	ns
Reverse recovery time	t_{rr}		-	60	-	ns
Turn-off propagation delay time	t_{off}	$V_{LIN, HIN}$ = 0 V, I_C = 10 A, V_{DC} = 300 V	-	950	-	ns
Turn-off fall time	t_f		-	55	-	ns
Turn-off switching time	$t_{c(off)}$		-	120	-	ns
Short circuit propagation delay time	t_{SCP}	From $V_{IT,TH+}$ to 10% I_{SC}	-	1250	-	ns
IGBT turn-on energy (includes reverse recovery of diode)	E_{on}	V_{DC} = 300 V, V_{DD} = 15 V, I_C = 10 A T_J = 25°C T_J = 150°C	 - -	 400 490	 - -	µJ
IGBT turn-off energy	E_{off}	V_{DC} = 300 V, V_{DD} = 15 V, I_C = 10 A T_J = 25°C T_J = 150°C	 - -	 190 290	 - -	µJ
Diode recovery energy	E_{rec}	V_{DC} = 300 V, V_{DD} = 15 V, I_C = 10 A T_J = 25°C T_J = 150°C	 - -	 55 70	 - -	µJ

7.2 Control Section

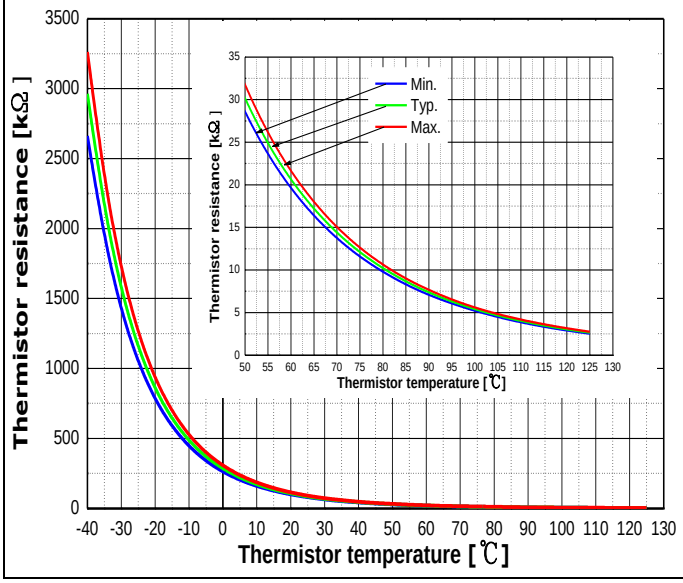
Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Bootstrap diode reverse recovery time	t_{rr_BSD}	I_F = 0.6 A, di/dt = 80 A/µs	-	50	-	ns
Input filter time ITRIP	t_{ITRIP}	V_{ITRIP} = 1 V	-	530	-	ns
Input filter time at LIN, HIN for turn on and off	$t_{FIL,IN}$	$V_{LIN, HIN}$ = 0 V or 5 V	-	290	-	ns
Fault clear time after ITRIP-fault	t_{FLTCLR}		40	65	100	µs
ITRIP to fault propagation delay	t_{FLT}	$V_{LIN, HIN}$ = 0 or $V_{LIN, HIN}$ = 5 V, V_{ITRIP} = 1 V	-	730	1000	ns
Internal deadtime	DT_{IC}		-	380	-	ns
Matching propagation delay time (on and off) all channels	M_T	External dead time > 500 ns	-	20	-	ns

7.3 PFC Section

Description	Symbol	Condition	Value			Unit
			min	typ	max	
Input capacitance	C_{ies}	V_{GE} = 0 V, V_{CE} = 25 V, f = 1 MHz	-	1900	-	pF
Output capacitance	C_{oes}		-	107	-	
Reverse transfer capacitance	C_{res}		-	55	-	
Gate charge	Q_G	V_{DC} = 520 V, I_C = 30 A, V_{GE} = 15 V	-	165	-	nC
Turn-on delay time	$t_{d(on)}$	V_{DC} = 400 V, I_C = 30 A, R_G = 10 Ω, C_{GE} = 4.7 nF, R_{GE} = 10 kΩ, T_J = 25°C	-	20	-	ns
Turn-on rise time	t_r		-	90	-	ns
Turn-off delay time	$t_{d(off)}$		-	205	-	ns
Turn-off fall time	t_f		-	30	-	ns
Reverse recovery time	t_{rr}		-	100	-	ns
Turn-on energy	E_{on}	V_{DC} = 400 V, I_C = 30 A, R_G = 10 Ω, C_{GE} = 4.7 nF, R_{GE} = 10 kΩ T_J = 25°C T_J = 150°C	- -	1540 2025	- -	µJ
Turn-off energy	E_{off}	V_{DC} = 400 V, I_C = 30 A, R_G = 10 Ω, C_{GE} = 4.7 nF, R_{GE} = 10 kΩ T_J = 25°C T_J = 150°C	- -	510 600	- -	µJ
Diode recovery energy	E_{rec}	V_{DC} = 400 V, I_C = 30 A, R_G = 10 Ω, C_{GE} = 4.7 nF, R_{GE} = 10 kΩ T_J = 25°C T_J = 150°C	- -	50 120	- -	µJ

8 Thermistor

Description	Condition	Symbol	Value			Unit
			Min.	Typ.	Max.	
Resistance	T_{NTC} = 25°C	R_{NTC}	-	85	-	kΩ
B-constant of NTC (Negative Temperature Coefficient)		B(25/100)	-	4092	-	K



T [°C]	Rmin. [kΩ]	Rtyp. [kΩ]	Rmax. [kΩ]
50	28.400	29.972	31.545
60	19.517	20.515	21.514
70	13.670	14.315	14.960
80	9.745	10.169	10.593
90	7.062	7.345	7.628
100	5.199	5.388	5.576
110	3.856	4.009	4.163
120	2.900	3.024	3.149
125	2.527	2.639	2.751

Figure 6 Thermistor resistance – temperature curve and table
(For more information, please refer to the application note 'AN2016-10 CIPOS Mini Technical description')

9 Mechanical Characteristics and Ratings

Description	Condition	Value			Unit
		Min.	Typ.	Max.	
Comparative Tracking Index (CTI)		600	-	-	V
Mounting torque	M3 screw and washer	0.49	-	0.78	Nm
Backside Curvature	Refer to Figure 8	-50	-	100	µm
Weight		-	6.83	-	g

10 Qualification Information

UL Certification	File number: E314539	
RoHS Compliant	Yes (Lead-free terminal plating)	
ESD	HBM(Human Body Model) Class	2
	CDM(Charged Device Model) Class	C3

11 Diagrams and Tables

11.1 T_C Measurement Point

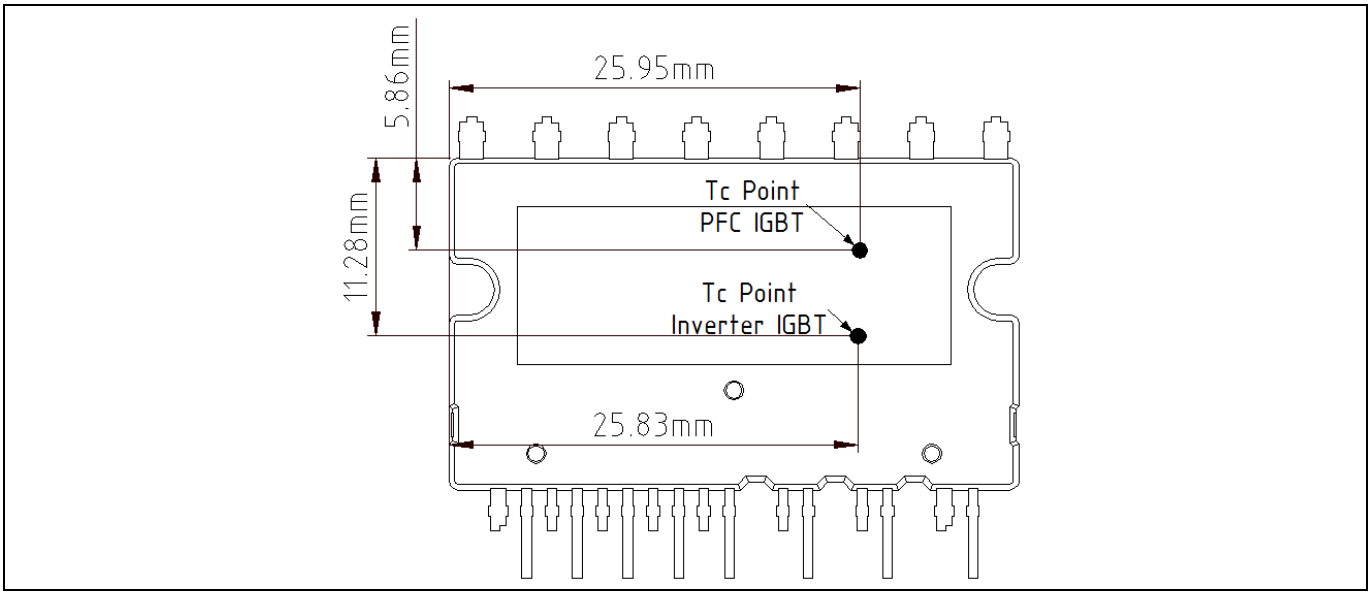


Figure 7 T_C measurement point[1]

11.2 Backside Curvature Measurment Point

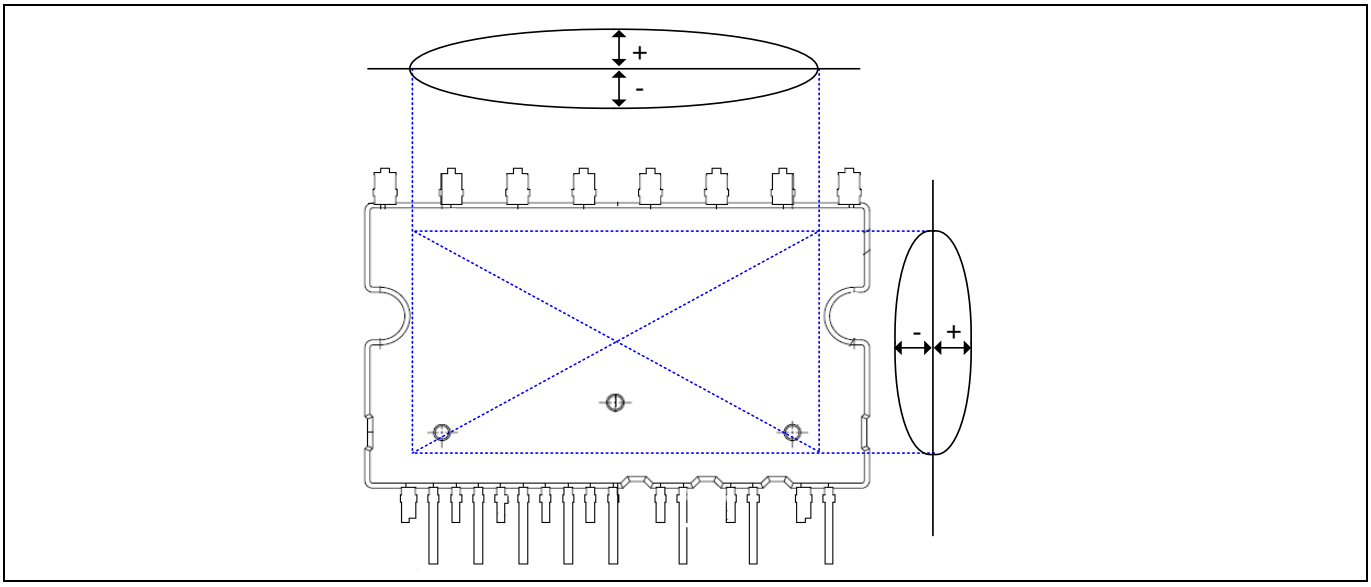


Figure 8 Backside curvature measurement position

[1]Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.

11.3 Switching Time Definition

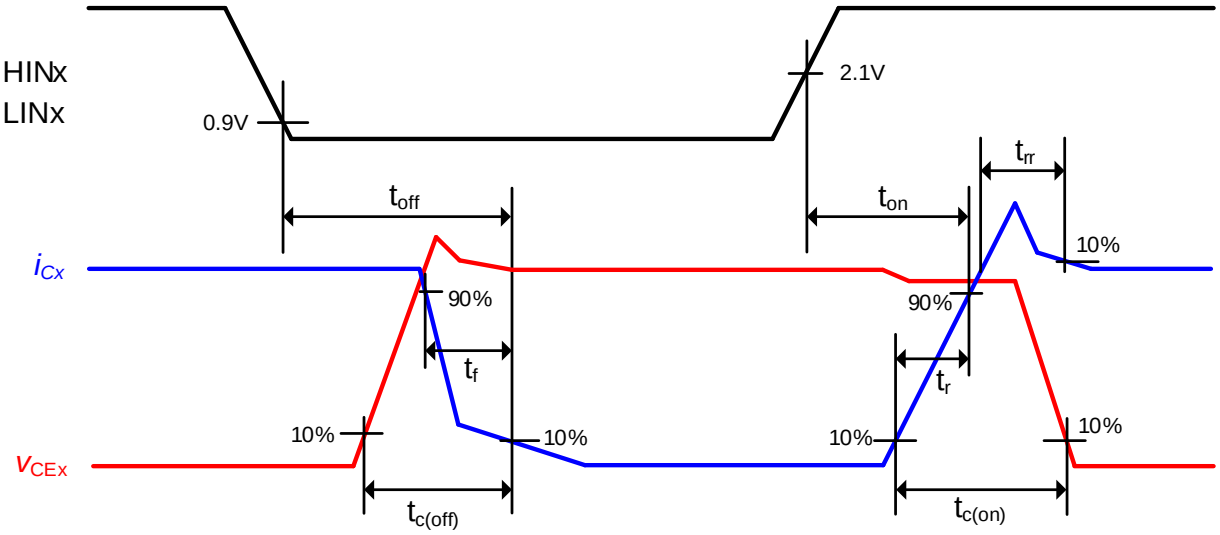


Figure 9 Switching times definition of inverter part

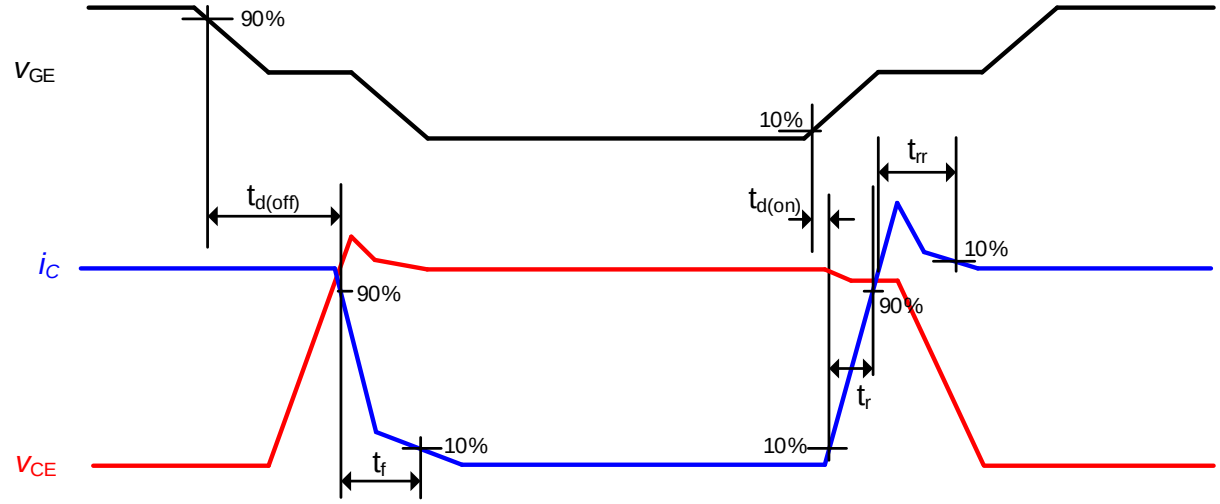


Figure 10 Switching times definition of PFC part

12 Application Guide

12.1 Typical Application Schematic

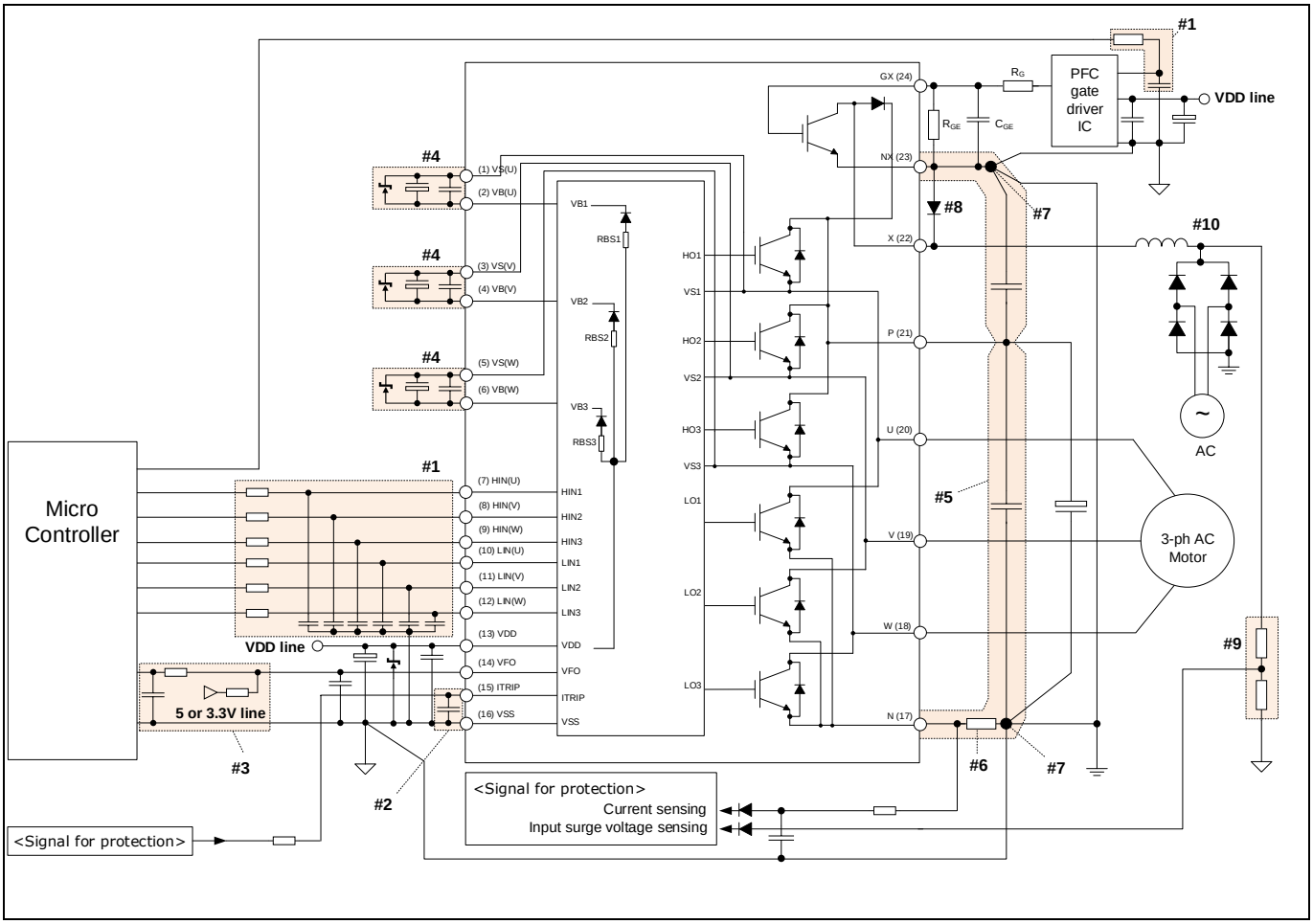


Figure 11 Typical application circuit

- #1 Input circuit
  - RC filter can be used to reduce input signal noise. (100 Ω, 1 nF)
  - The capacitors should be located close to the IPM (to V_{SS} terminal especially).
- #2 Itrip circuit
  - To prevent protection function erros, RC filter is recommended.
  - The capacitor should be located close to Itrip and V_{SS} terminals.
- #3 V_{FO} circuit
  - V_{FO} pin is open drain configuration. This terminal should be pulled up to the bias voltage of the 5 V/3.3 V through a proper resistor.
  - It is recommended that RC filter is placed close to the controller.
- #4 V_B-V_S circuit
  - Capacitors for high-side floating supply voltage should be placed close to V_B and V_S terminals.
- #5 Snubber capacitor
  - The wiring among the IPM, snubber capacitor and shunt resistors should be short as possible.
- #6 Shunt resistor

- SMD type shunt resistors are strongly recommended to minimize its internal stray inductance.

- #7 Ground pattern
  - Pattern overlap of power ground and signal ground should be minimized. The patterns should be connected at one end of shunt resistor only for the same potential.
- #8 Anti-parallel diode
  - It is required to connect anti-parallel diode to PFC IGBT. (2 A, voltage rating higher than 650 V)
- #9 Input surge voltage protection circuit
  - This protection circuit can be added to protect PFC IGBT from excessive surge voltage.
- #10 Inrush current protection circuit
  - Proper inrush current protection circuit has to be considered.
  - Additional components such as thermistor, relay, or bypass diode may be required depending on the system design and the operating conditions including grid fluctuation.

12.2 Performance Chart

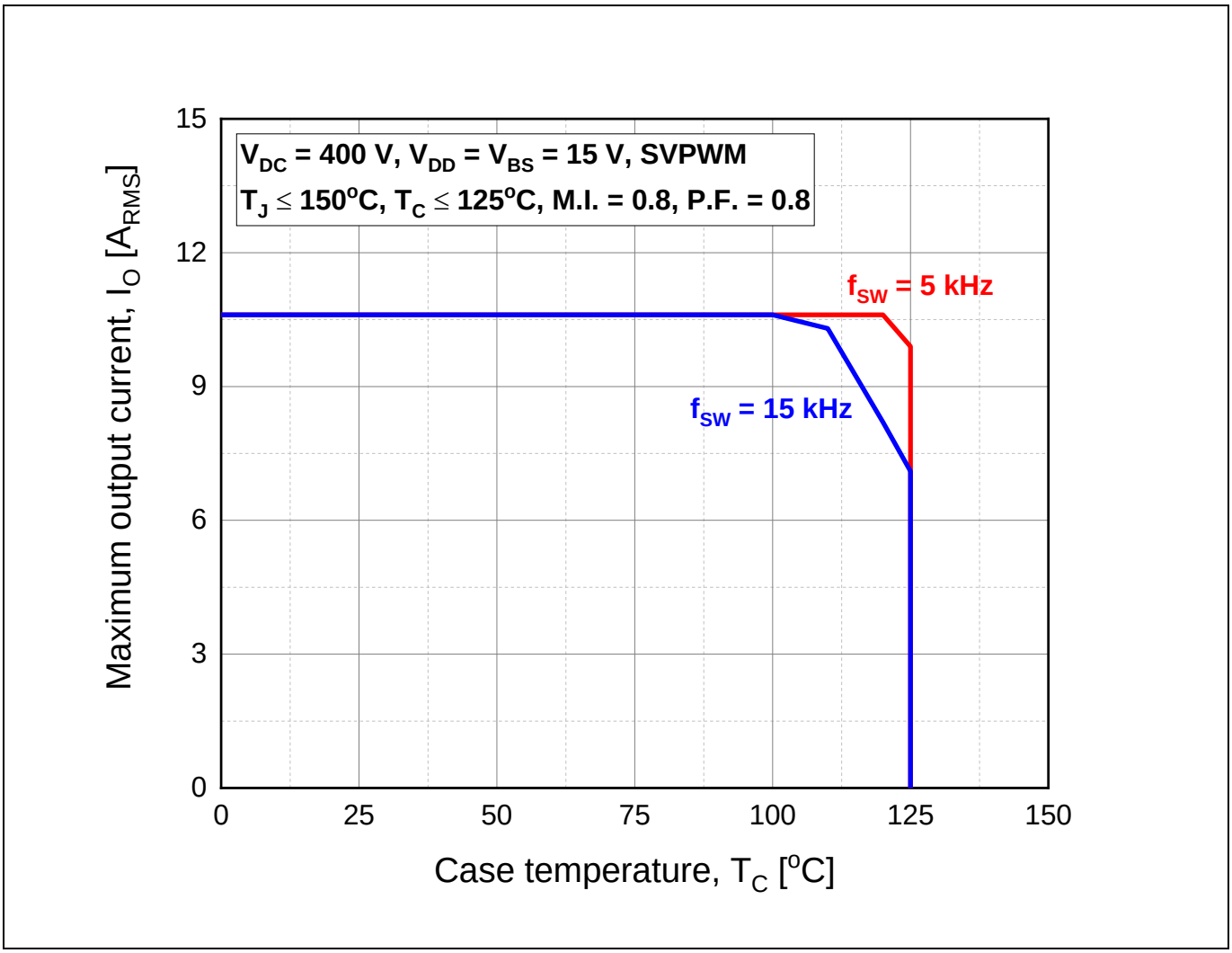


Figure 12 Maximum operating current SOA of inverter part[1]

[1]This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be changed by each user's actual operating conditions.

13 Package Outline

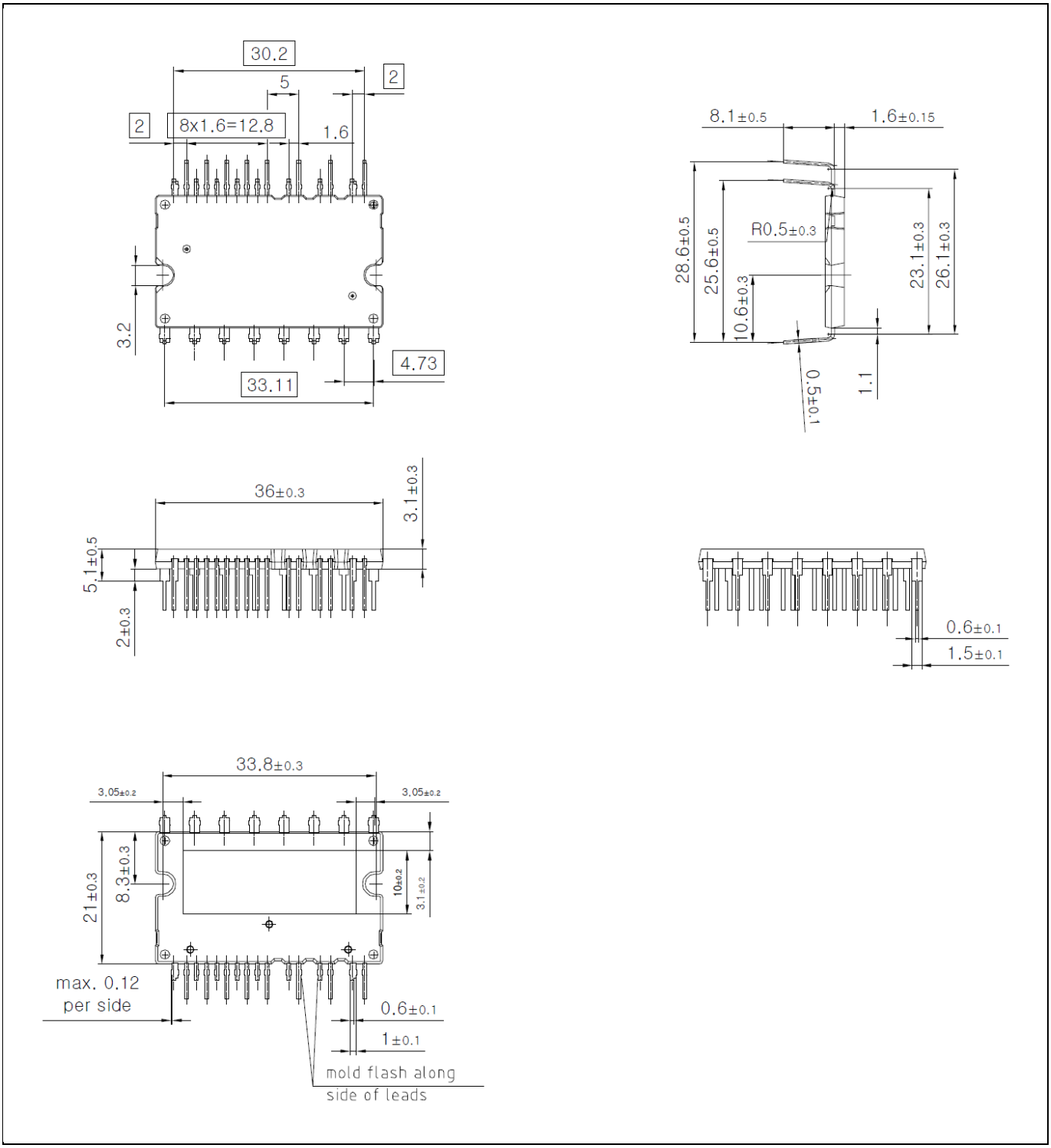


Figure 13 IFCM15S60GD

Package Outline

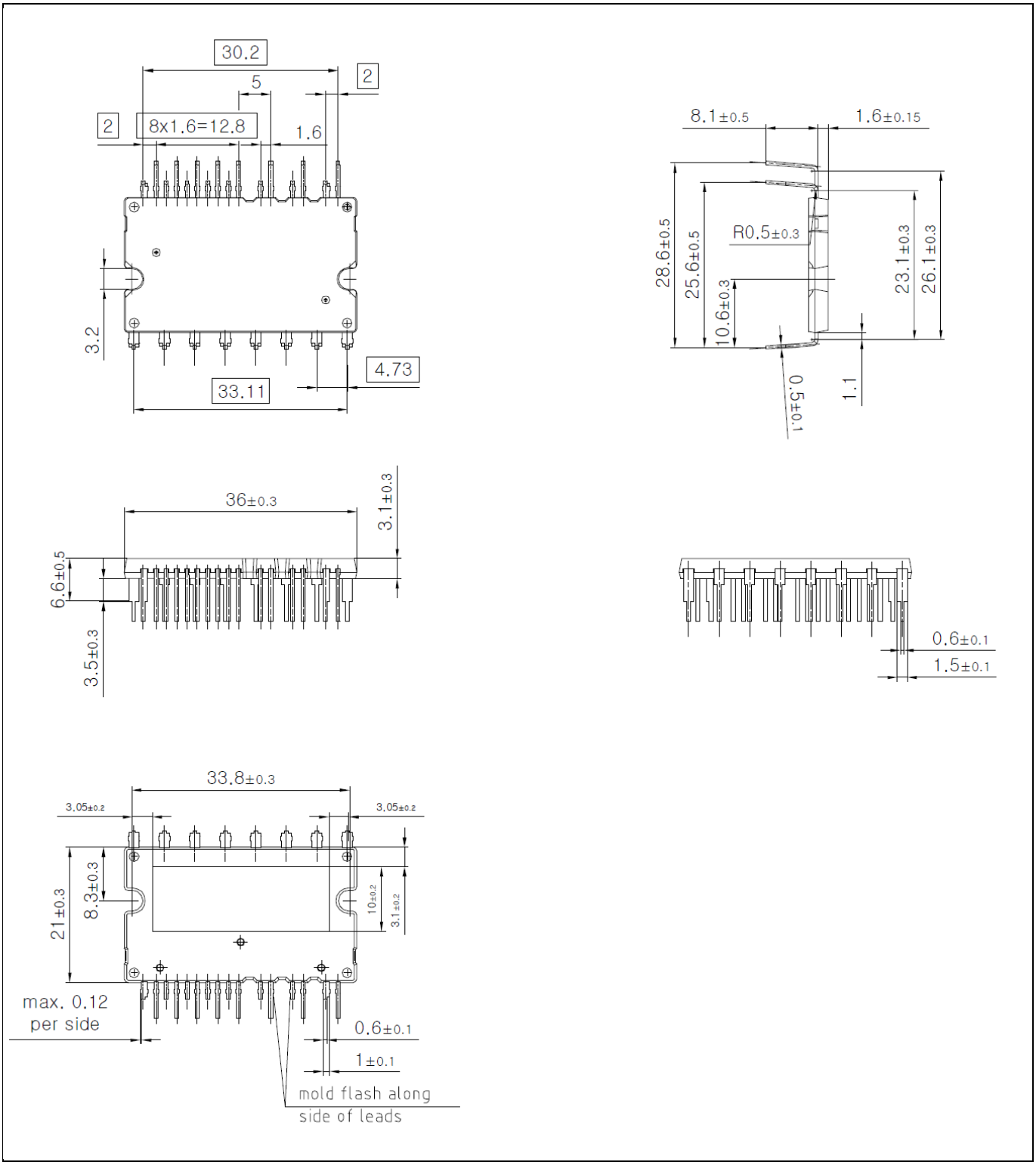


Figure 14 IFCM15S60GS

Revision history

Document version	Date of release	Description of changes
V 2.0	2017-04-20	Initial release
V 2.1	2017-08-02	Updated package outline and application circuit
V 2.2	2017-09-06	Maximum operating case temperature, T_C = 125°C
V 2.3	2020-06-15	Added extended stand-off package outline
V 2.4	2021-12-21	Updated 3.4 PFC section

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Edition 2021-12-21

Published by

Infineon Technologies AG

81726 München, Germany

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Document reference

ifx1

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