DRV3256-Q1 Integrated 3-Phase 48-V Automotive Gate Driver Unit (GDU) with Advanced Protection and Diagnostics

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device ambient temperature grade 0: –40°C to +150°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Functional Safety-Compliant targeted
  - Developed for functional safety applications
  - Documentation to aid ISO 26262 system design will be available upon production release
  - Systematic capability up to ASIL D targeted
- Three N-Channel half-bridge gate driver
  - 2-A/2.5-A max peak gate drive current
  - Power architecture optimized for 48-V applications
  - 12-V/48-V split supply architecture
  - 95-V transient absolute maximum rating of DC link power supply (DHCP)
  - 105-V Bootstrap voltage to support 90-V MOSFET operating voltage range
  - Bootstrap with charge pump for 100% duty cycle
- Integrated 1x (DRV3256A-Q1) or 3x (DRV3256-Q1) current shunt amplifiers
- Integrated configurable Active Short Circuit (ASC) function
  - Low-side (DRV3256A-Q1) or Low-side and High-side (DRV3256-Q1/DRV3256B-Q1) ASC support
  - Low-side and High-side ASC support
  - Device pin control available
  - Fault handling capability
- Serial peripheral interface (SPI) with CRC
- Supports 3.3-V and 5-V logic inputs
- Advanced protection features
  - Battery voltage monitors
  - MOSFET V_{DS} overcurrent monitors
  - R_{shunt} overcurrent monitors
  - MOSFET V_{GS} gate fault monitors
  - Analog built in self test
  - Internal regulator and clock monitors
  - Device thermal warning and shutdown
  - Fault condition indicator pins

2 Applications

- Automotive 48-V Motor Drive Systems
  - Belt and integrated starter generators, and Motor generators
  - Electrical Power Steering
  - eTurbos and eBoosters
  - Transmission control and actuation
  - Oil, transmission, and water pumps
  - HVAC compressors and fans

3 Description

The DRV3256-Q1 family of devices are highly-integrated three phase gate drivers for 48-V automotive motor drive applications. These devices are specifically designed to support high-power motor drive applications by providing 2-A peak source and 2.5-A peak sink gate drive currents, and 90-V MOSFET transient over voltage support. A highly efficient bootstrap architecture is used to minimize power losses and self-heating of the gate drivers. A charge pump allows for the gate drivers to support 100% PWM duty cycle control.

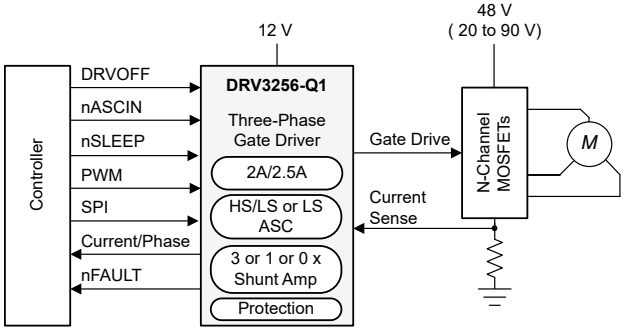
A wide range of diagnostics, monitoring, and protection features supports a robust motor drive system design. A highly configurable Active Short Circuit (ASC) function which enables selected external MOSFETs is integrated to achieve the fast response to system faults and to eliminate the needs of external components.

Three or single low-side current shunt amplifiers are optionally provided to support resistor based low-side current sensing.

Package Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
DRV3256-Q1(2)	HTQFP (64)	10.00 mm × 10.00 mm

(1) See the orderable addendum at the end of the data sheet.
(2) For all available device variants, see the device comparison table.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2022) to Revision C (December 2022)	Page
• Added DRV3256P-Q1 device variant in the Device Comparison Table and packaging information tables	0

Changes from Revision A (July 2022) to Revision B (August 2022)	Page
• Updated the device status for DRV3256B-Q1	1

Changes from Revision * (June 2022) to Revision A (July 2022)	Page
• Updated the device status for DRV3256-Q1	1

Device Comparison Table

PART NUMBER	DEVICE VARIANT	MAX GATE DRIVE CURRENT	SHUNT AMPLIFIERS	Active Short Circuit (HS = High-Side, LS = Low-Side)
DRV3256-Q1	DRV3256A-Q1	2 A or 2.5 A	1	LS only
	DRV3256B-Q1	2 A or 2.5 A	0	HS and LS
	DRV3256-Q1	2 A or 2.5 A	3	HS and LS
	DRV3256P-Q1(1)	2 A or 2.5 A	3	HS and LS

(1) DRV3256P-Q1 supports Watchdog Timer function, VGLPU_CTRL, PVDD_UV2_LVL2, SD_MODE_SEL register bits in addition to the features of the device variant DRV3256-Q1.

5 Device and Documentation Support

5.1 Device Support

5.1.1 Device Nomenclature

Device Nomenclature shows a legend for reading the complete orderable device name for the DRV3256-Q1 device

5.2 Documentation Support

For related documentation see the following:

- Texas Instruments, *How to Build a Small, Functionally Safe 48-V, 30-kW MHEV Motor-Drive System* White paper
- Texas Instruments, *How to optimize a motor-driver design for 48-V starter generators* Technical article
- Texas Instruments, *System Design Considerations for High-Power Motor Driver Applications* Application note
- Texas Instruments, *Driving parallel MOSFETs using the DRV3255-Q1* Application brief
- Texas Instruments, *A basic brushless gate driver design – part 3: integrated vs. discrete half bridges* Technical article
- Texas Instruments,*PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments,*PowerPAD™ Made Easy* application report
- Texas Instruments,*Sensored 3-Phase BLDC Motor Control Using MSP430* application report

5.2.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.4 Trademarks

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All trademarks are the property of their respective owners.

5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

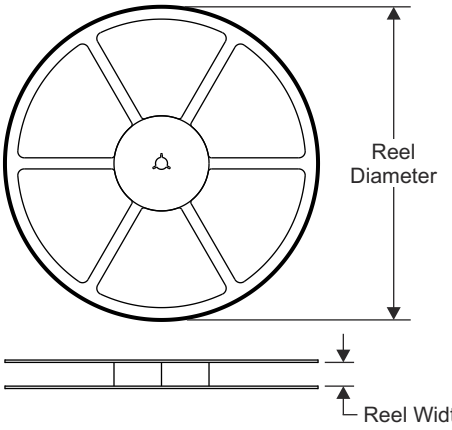
6.1 Package Option Addendum

Packaging Information

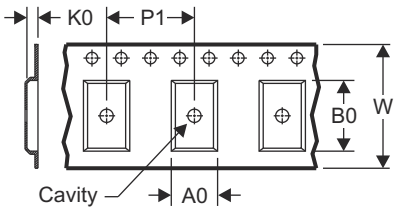
Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking
DRV3256AEPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV3256A
DRV3256EPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV3256
DRV3256BEPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV3256B
DRV3256PEPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV3256P

6.2 Tape and Reel Information

REEL DIMENSIONS



TAPE DIMENSIONS



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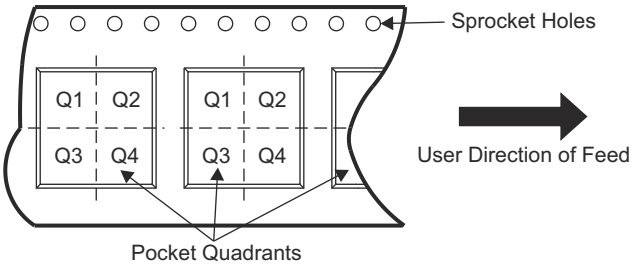
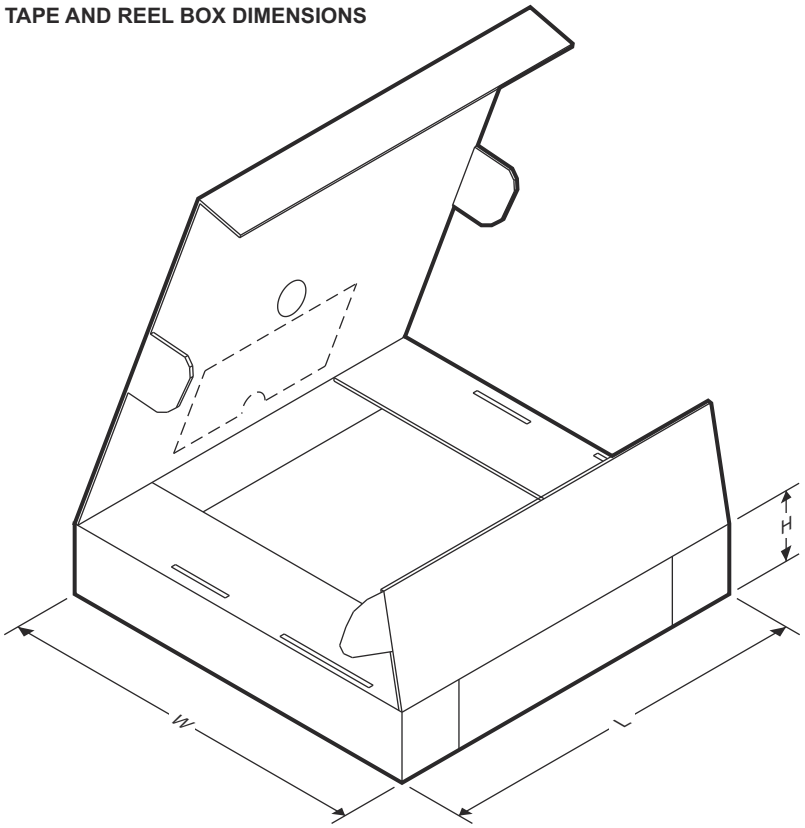
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3256AEPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
DRV3256EPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
DRV3256BEPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
DRV3256PEPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



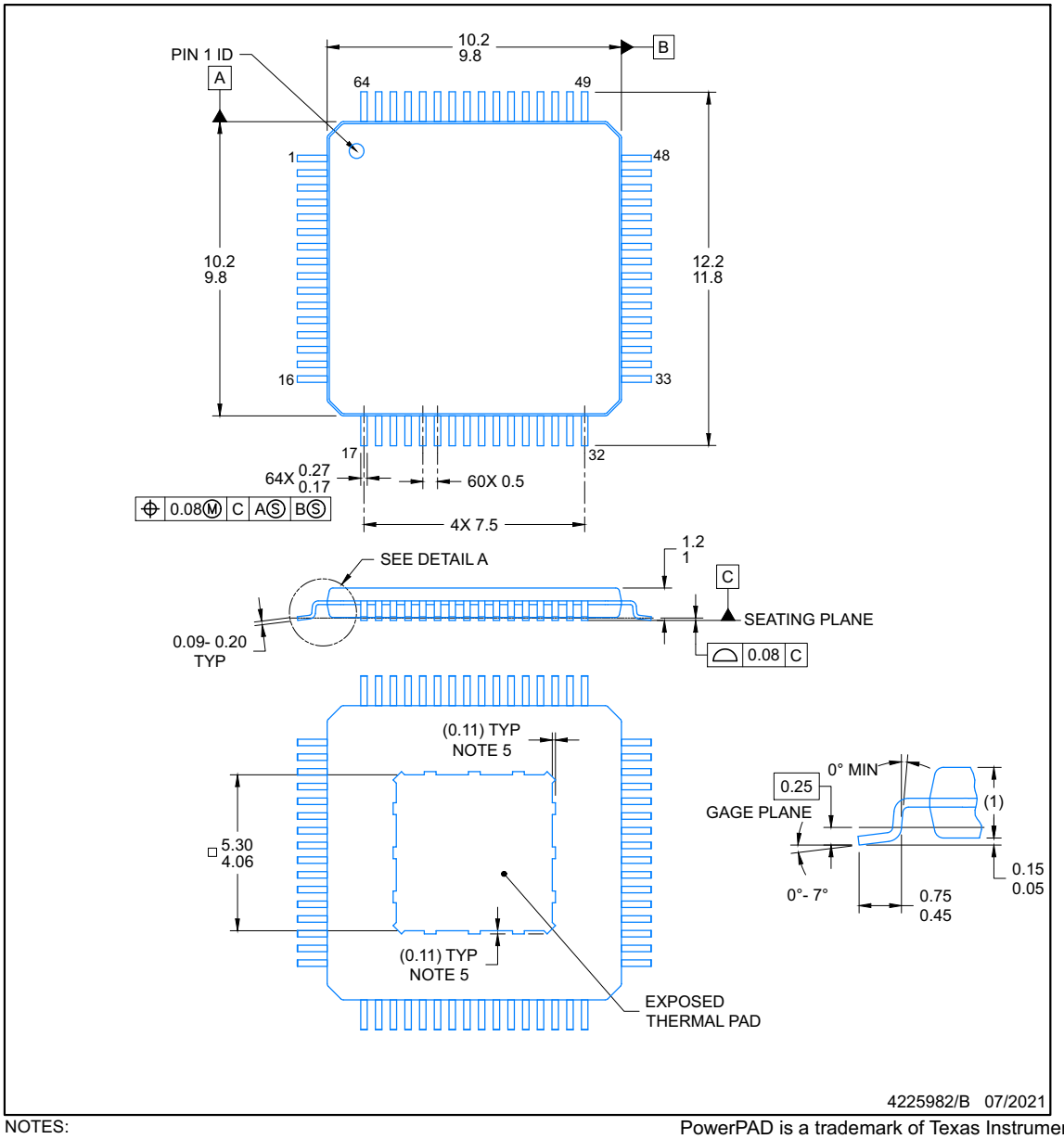
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3256AEPAPRQ1	HTQFP	PAP	64	1000	10.0	10.0	1.0
DRV3256EPAPRQ1	HTQFP	PAP	64	1000	10.0	10.0	1.0
DRV3256BEPAPRQ1	HTQFP	PAP	64	1000	10.0	10.0	1.0
DRV3256PEPAPRQ1	HTQFP	PAP	64	1000	10.0	10.0	1.0

PACKAGE OUTLINE

PAP0064N

HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES:

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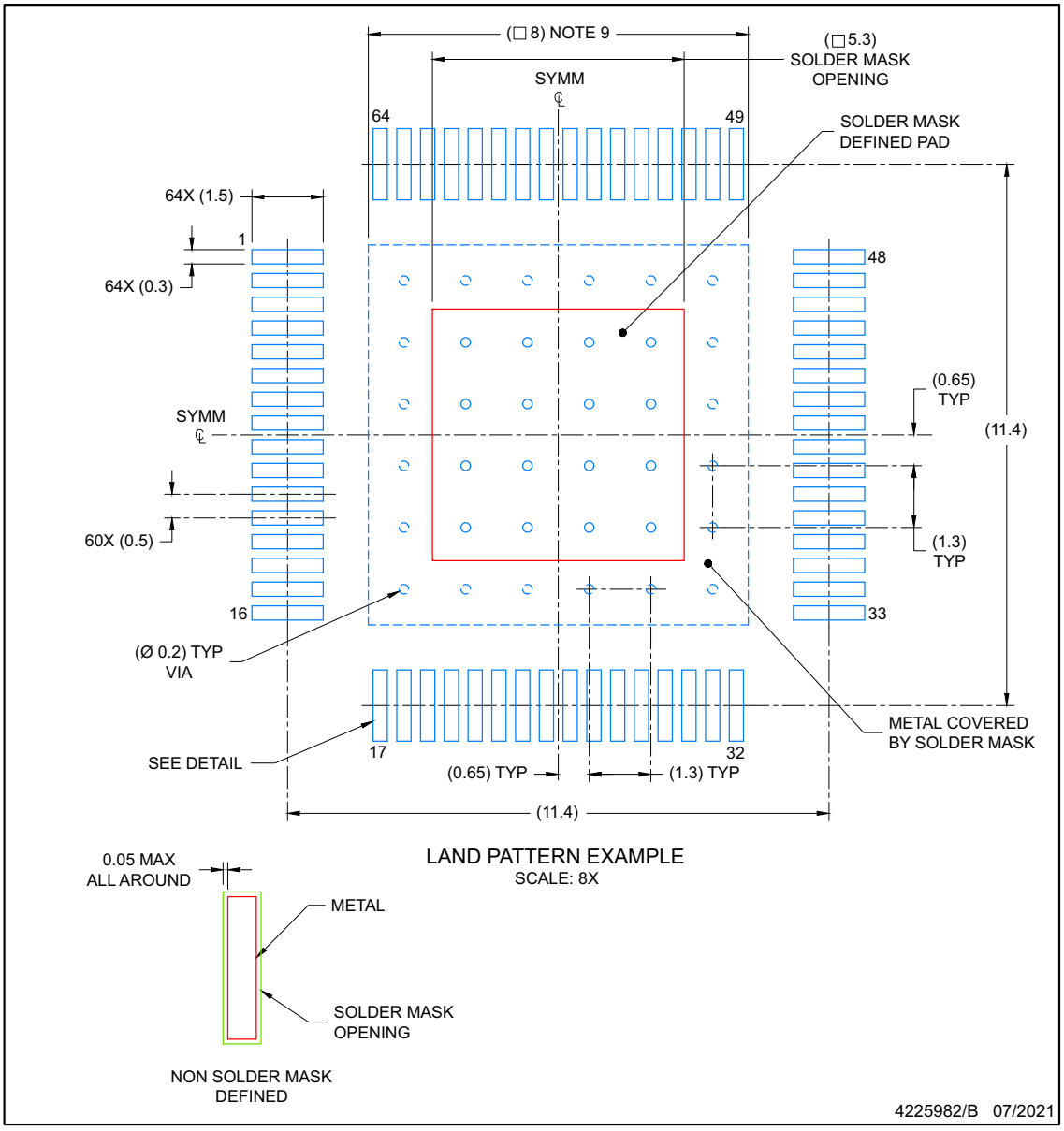
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Strap features may not be present.
6. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

PAP0064N

HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

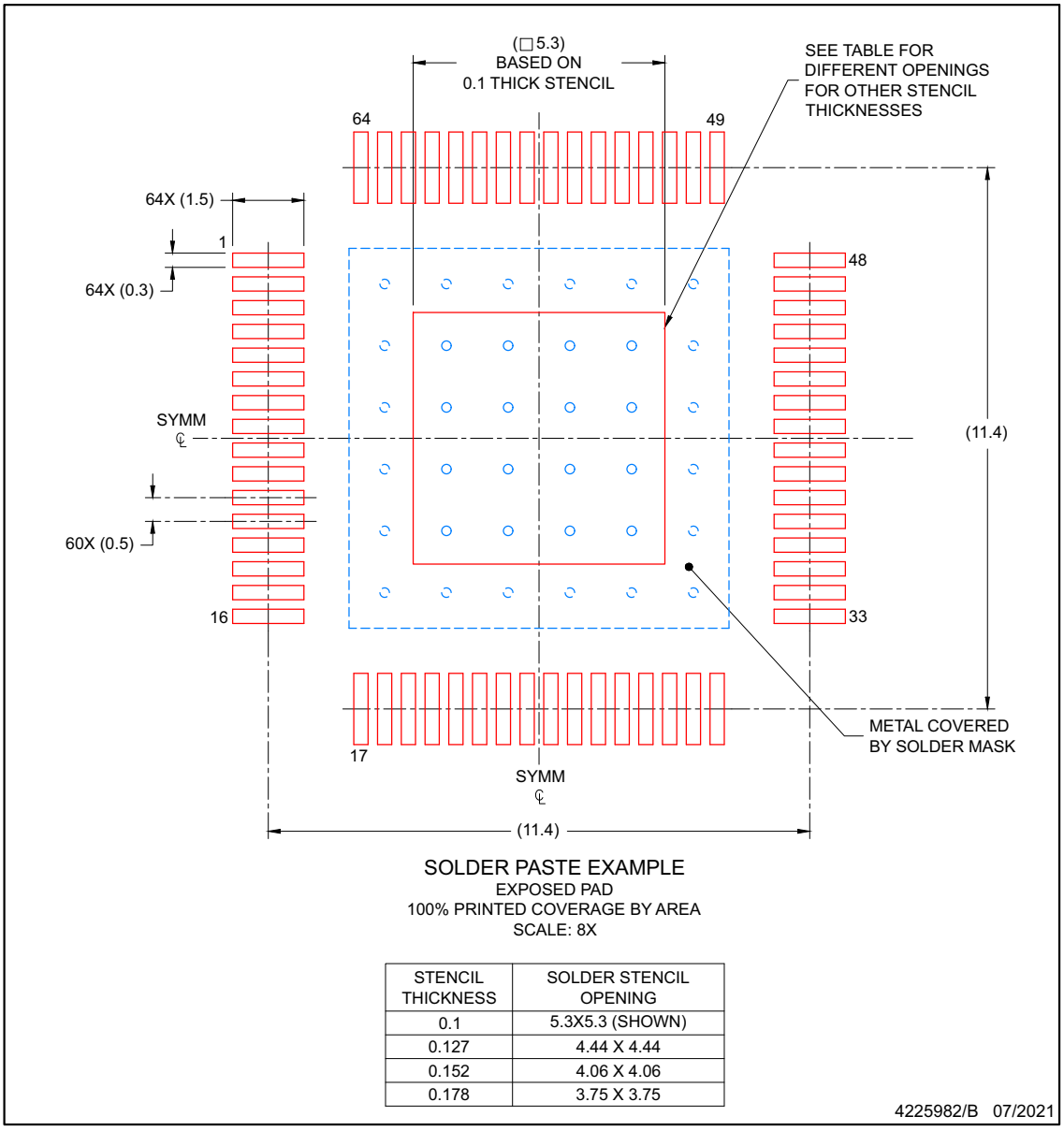
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PAP0064N

HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED COVERAGE BY AREA
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.3X5.3 (SHOWN)
0.127	4.44 X 4.44
0.152	4.06 X 4.06
0.178	3.75 X 3.75

4225982/B 07/2021

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV3256AEPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV3256A Q1	Samples
DRV3256BEPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV3256B Q1	Samples
DRV3256EPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV3256 Q1	Samples
DRV3256PEPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV3256P Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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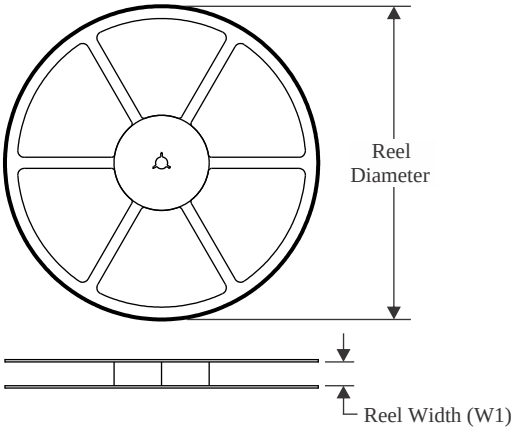
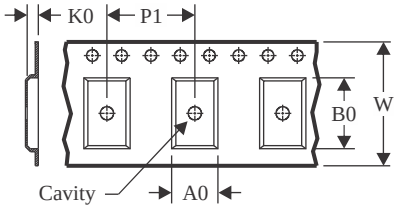
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



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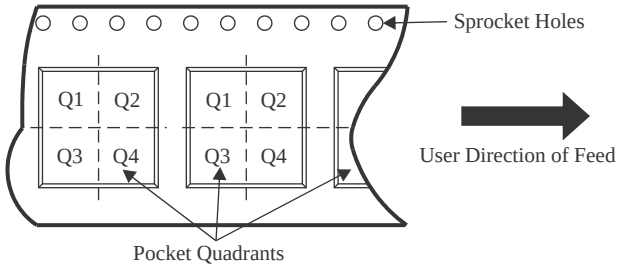

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3256AEPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
DRV3256BEPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
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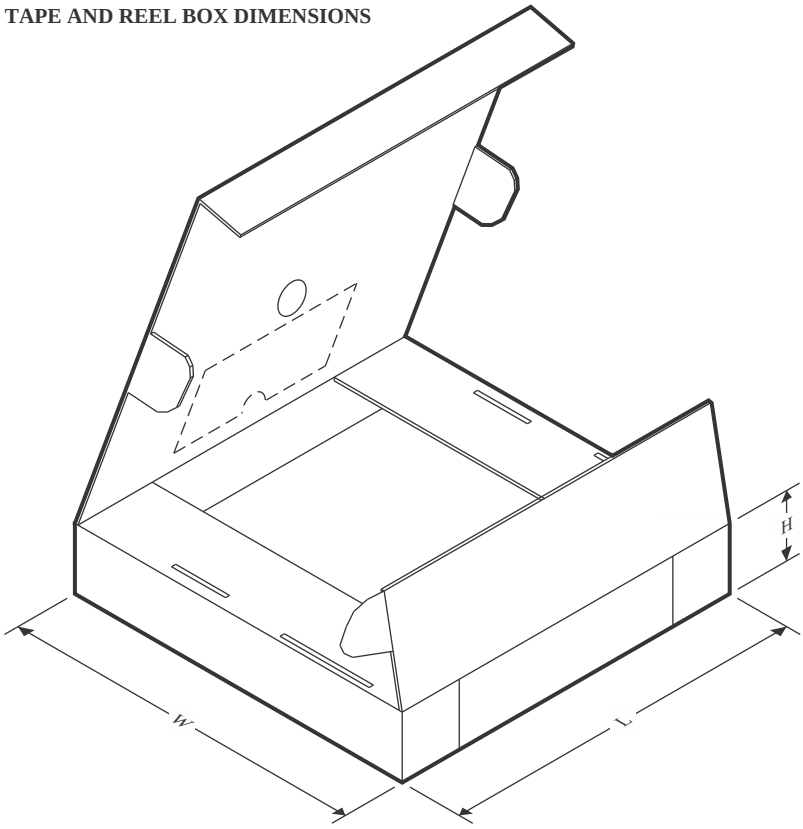
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

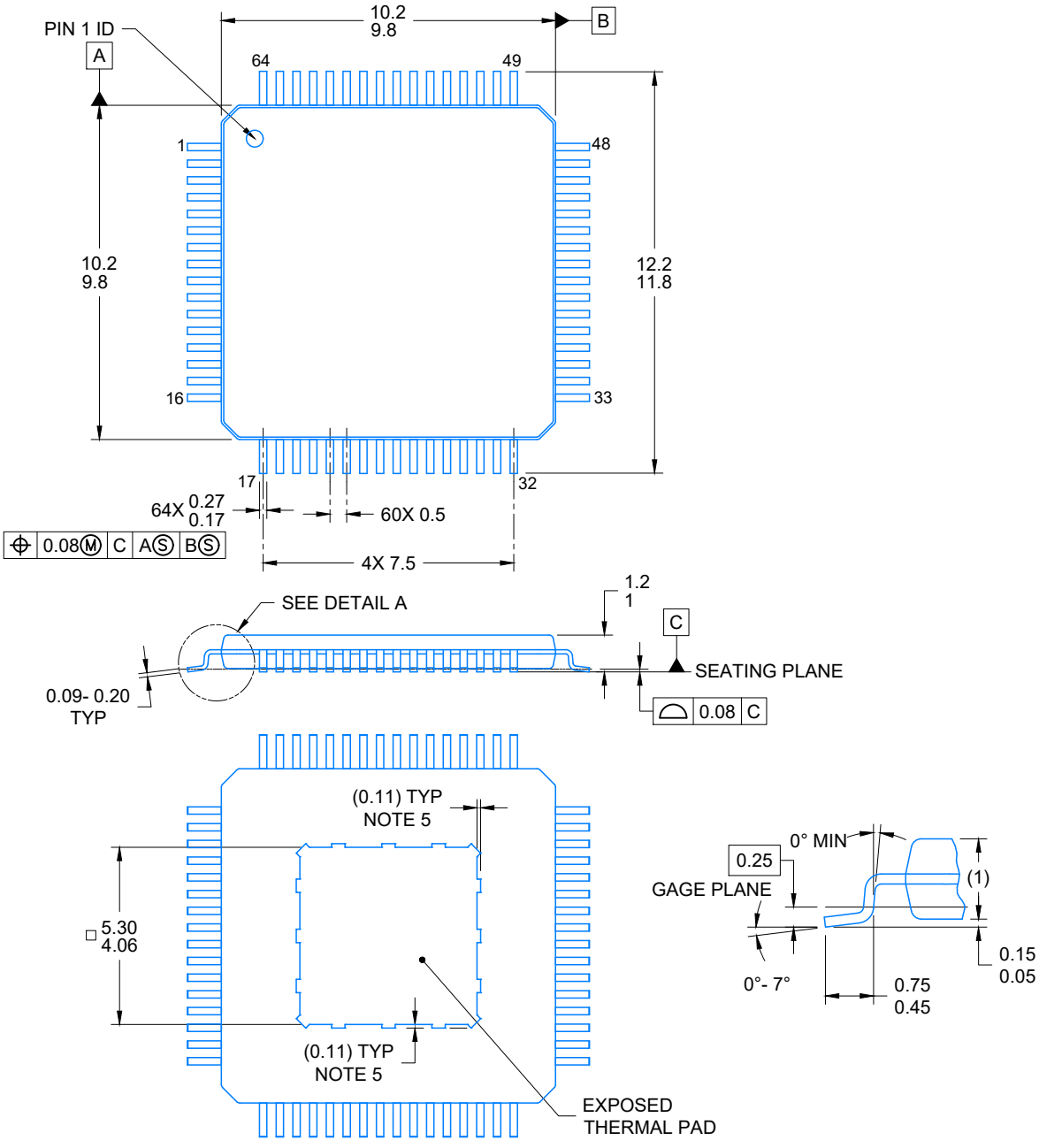
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3256AEPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0
DRV3256BEPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0
DRV3256EPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0

PACKAGE OUTLINE

PAP0064N

HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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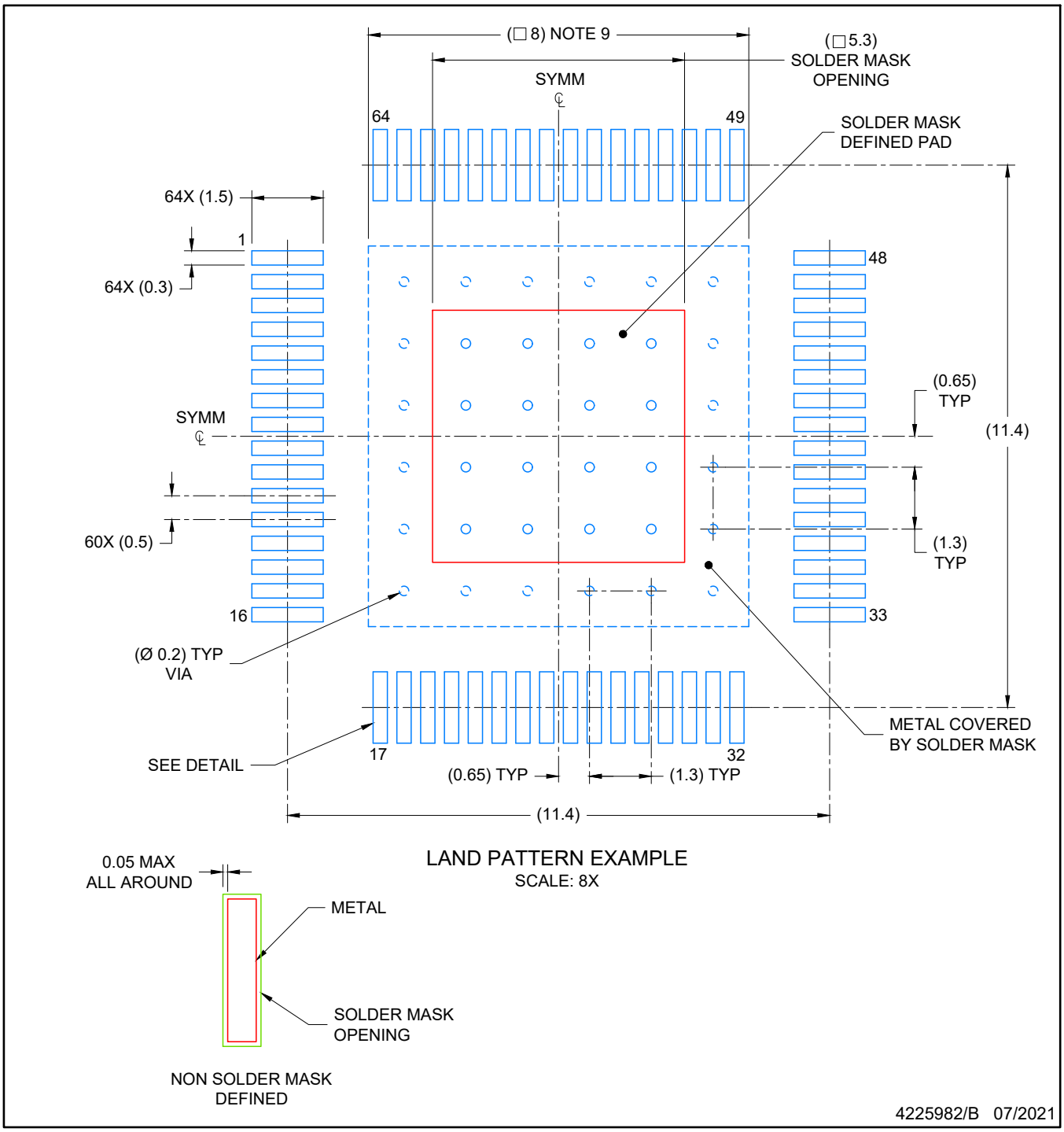

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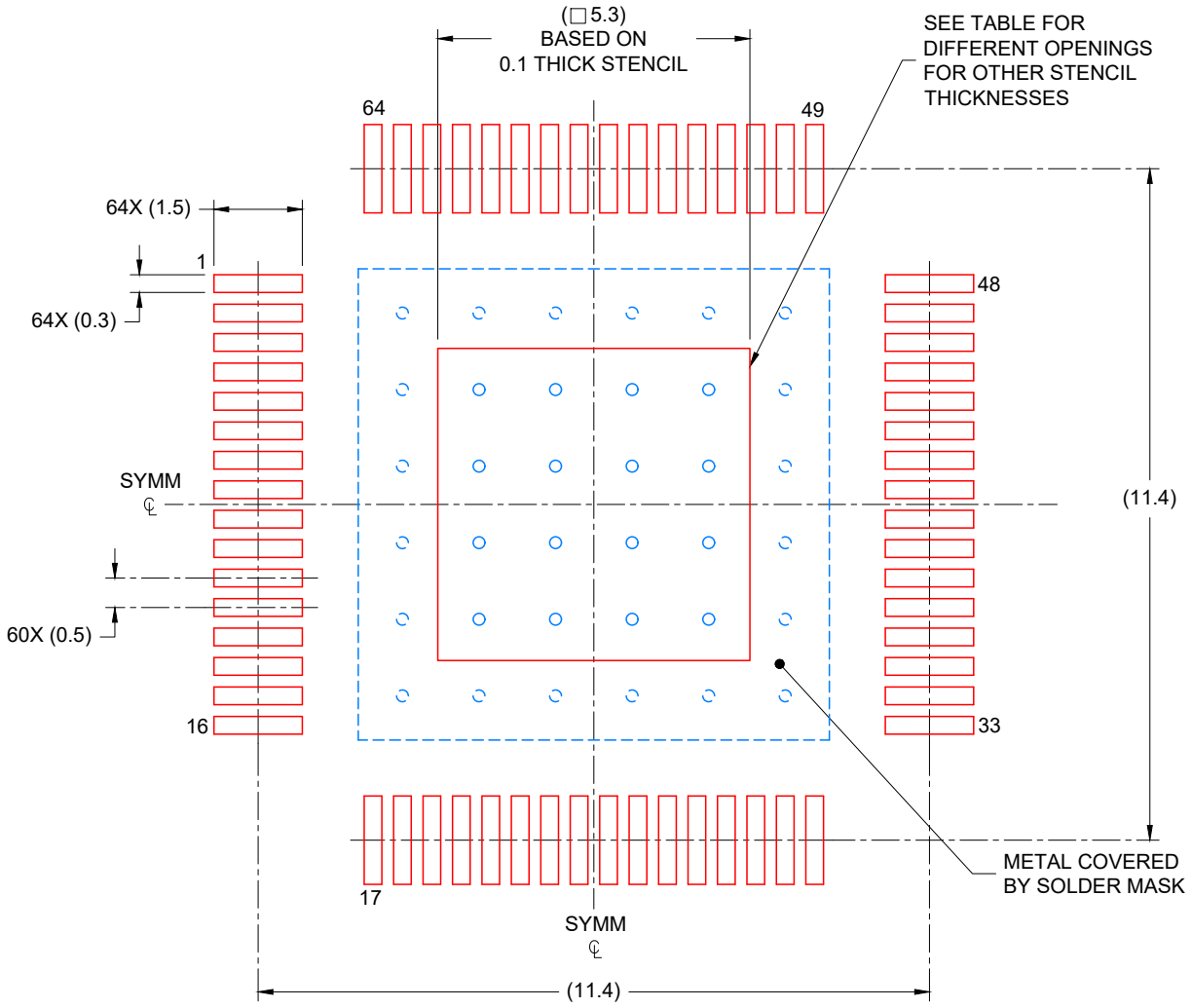

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED COVERAGE BY AREA
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
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