HV57708

64-Channel 32-MHz Serial-to-Parallel Converter with Push-Pull Outputs

Features

- 5V CMOS Logic
- Up to +80V Output Voltage
- Low-Power Level Shifting
- 32 MHz Equivalent Data Rate
- Latched Data Outputs
- Forward and Reverse Shifting Options (DIR pin)
- Diode to V_{PP} allows Efficient Power Recovery
- Outputs may be Hot Switched

Applications

- Vacuum Fluorescent Display Driver
- Inkjet Driver
- 3D Printer Driver
- Microelectromechanical Systems Applications

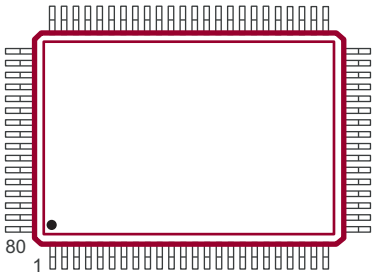
General Description

The HV57708 is a low-voltage to high-voltage serial-to-parallel converter with push-pull outputs. The device is designed as a driver for EL displays. It can also be used in any application requiring multiple-output high-voltage current sourcing and sinking capability such as driving plasma panels, vacuum fluorescent displays and large matrix LCD displays.

The device has four parallel 16-bit registers, permitting data rates four times the speed of the clock frequency. There are also 64 latches and a control logic to perform the polarity select and blanking of the outputs. The $HV_{OUT}1$ is connected to the first stage of the first Shift register through the polarity and blanking logic. Data is shifted through the Shift registers on the logic low-to-high transition of the clock. The DIR pin causes counter-clockwise shifting when connected to GND and clockwise shifting when connected to V_{DD}. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register, $HV_{OUT}64$. The operation of the Shift register is not affected by the latch enable ($\overline{LE}$), blanking ($\overline{BL}$) and polarity ($\overline{POL}$) inputs. The transfer of data from the Shift registers to the latches occurs when the $\overline{LE}$ input is high. The data in the latches is stored when $\overline{LE}$ is low.

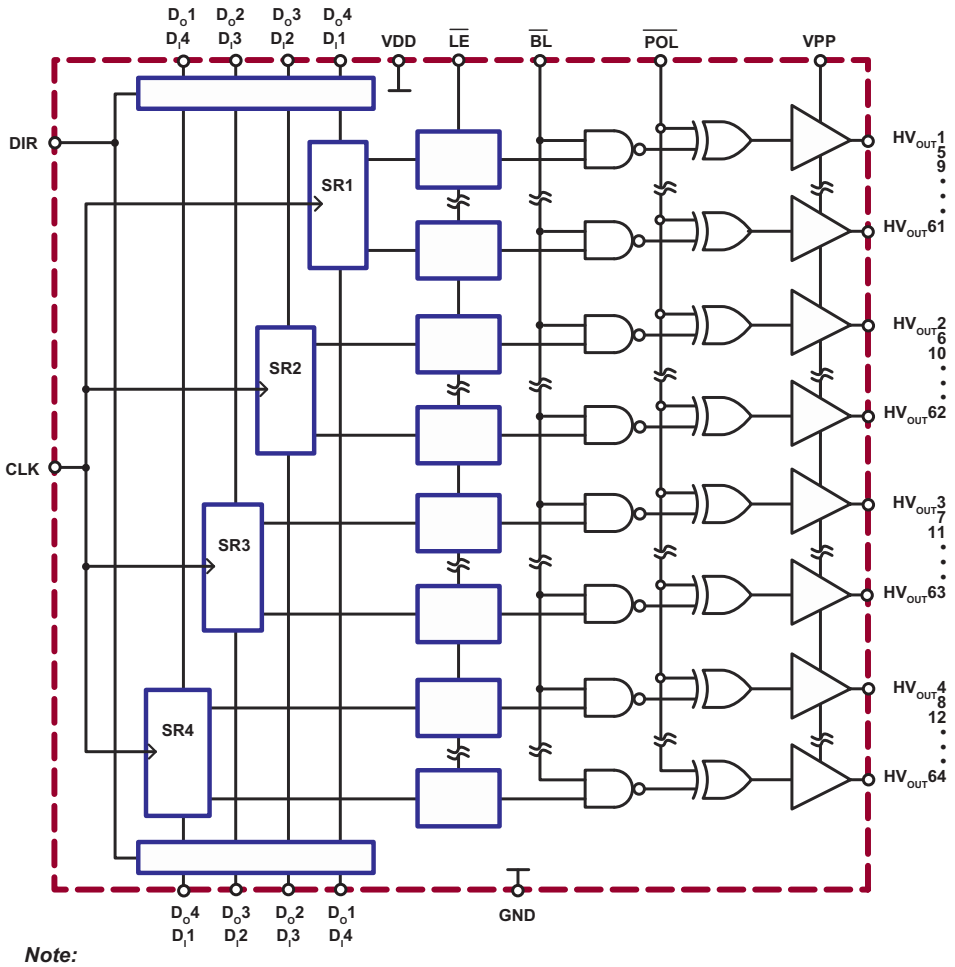
Package Type

80-lead PQFP
(Top view)



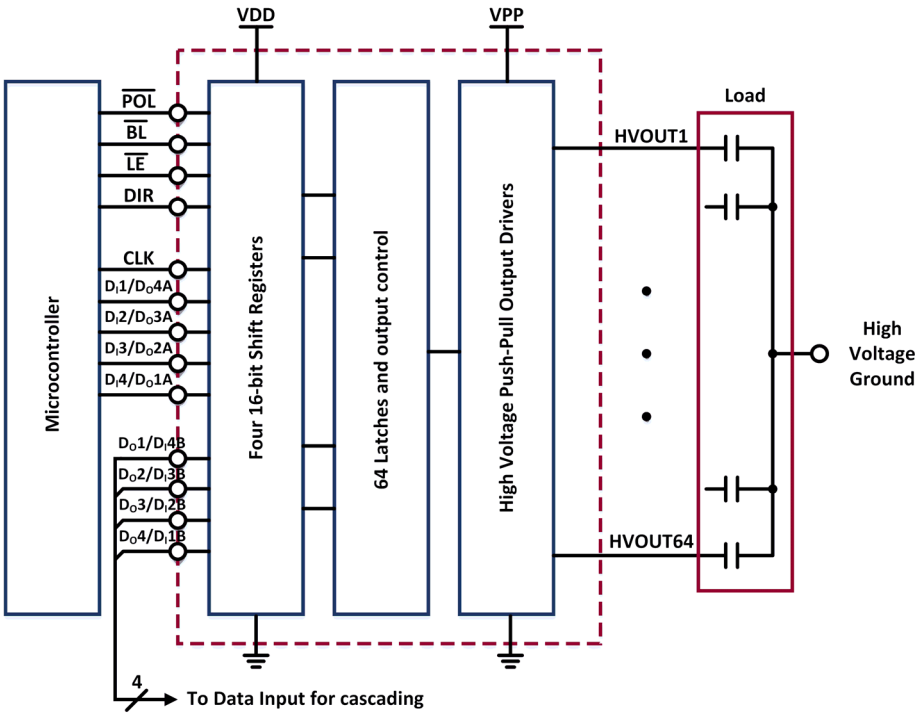
See Table 2-1 for pin information.

Functional Block Diagram



Note:
Each SR (shift register) provides 16 outputs. SR1 supplies every fourth output starting with 1; SR2 supplies every fourth output with 2, etc.

Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, V_{DD} ..... –0.5V to +7.5V
Output Voltage, V_{PP} ..... –0.5V to +90V
Logic Input Levels ..... –0.3V to V_{DD} +0.3V
Ground Current (**Note 1**) 1.5A
Maximum Junction Temperature, $T_{J(MAX)}$ ..... +125°C
Storage Temperature, T_S ..... –65°C to +150°C
Continuous Total Power Dissipation:
80-lead PQFP (**Note 2**) ..... 1200 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Limited by the total power dissipated in the package
2: For operations above 25°C ambient, derate linearly to the maximum operating temperature at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	—	5.5	V	
Output Voltage	V_{PP}	8	—	80	V	
High-Level Input Voltage	V_{IH}	V_{DD}–0.5V	—	—	V	
Low-Level Input Voltage	V_{IL}	0	—	0.5	V	
Clock Frequency per Register	f_{CLK}	—	—	8	MHz	
Operating Ambient Temperature	T_A	–40	—	+85	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise noted.

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Supply Current		I_{DD}	—	—	15	mA	$V_{DD} = V_{DD}$ maximum, f_{CLK} = 8 MHz
High-Voltage Supply Current		I_{PP}	—	—	100	µA	Outputs high
			—	—	100	µA	Outputs low
Quiescent V_{DD} Supply Current		I_{DDQ}	—	—	100	µA	All $V_{IN} = V_{DD}$
High-Level Output	HV_{OUT}	V_{OH}	65	—	—	V	I_O = –15 mA, V_{PP} = +80V
	Data Out		V_{DD}–0.5V	—	—	V	I_O= –100 µA
Low-Level Output	HV_{OUT}	V_{OL}	—	—	7	V	I_O = 12 mA, V_{PP} = +80V
	Data Out		—	—	0.5	V	I_O = 100 µA
High-Level Logic Input Current		I_{IH}	—	—	1	µA	$V_{IH} = V_{DD}$
Low-Level Logic Input Current		I_{IL}	—	—	–1	µA	V_{IL} = 0V
High-Voltage Clamp Diode		V_{OC}	—	—	1	V	I_{OC} = 1 mA

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 85°C maximum. Logic signal inputs and data inputs have t_r, $t_f \leq$ 5 ns (10% and 90% points).

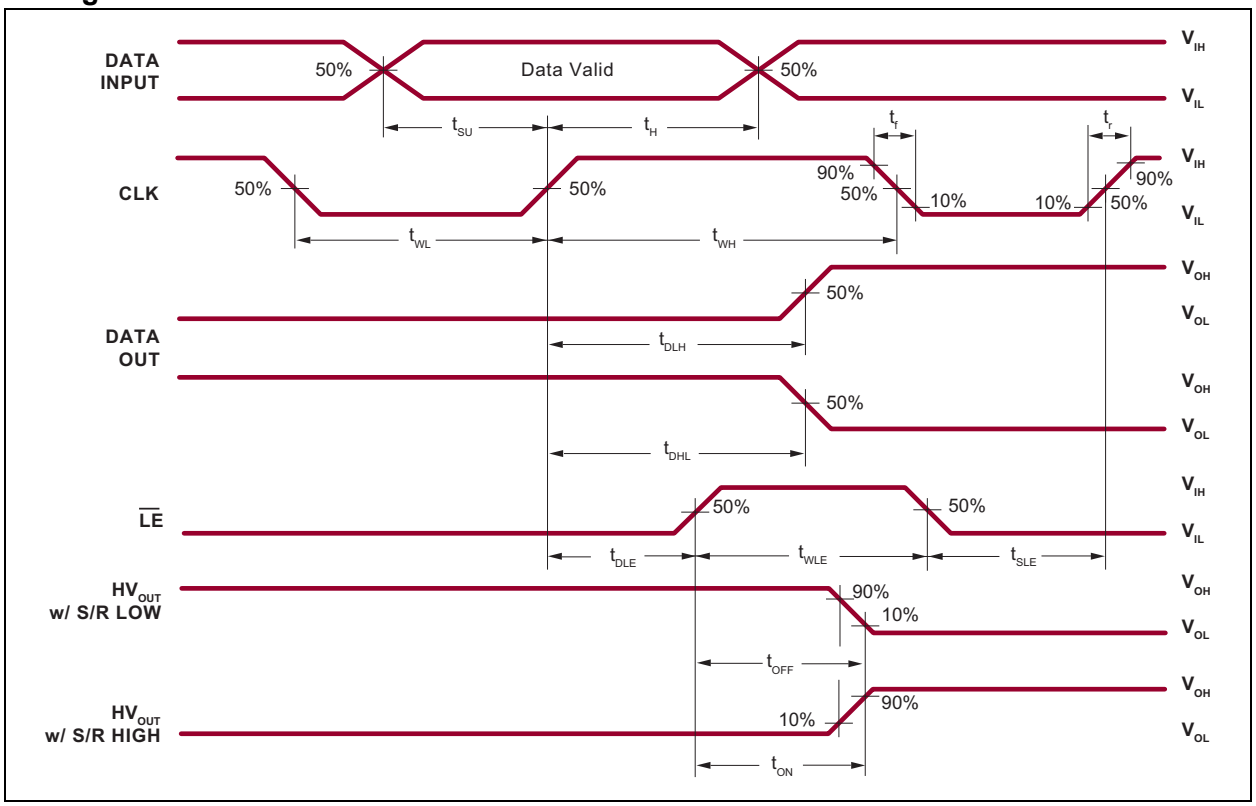
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	f_{CLK}	—	—	8	MHz	Per register
Clock Width High or Low	t_{WL}, t_{WH}	62	—	—	ns	
Data Set-Up Time before Clock Rises	t_{SU}	10	—	—	ns	
Data Hold Time after Clock Rises	t_H	15	—	—	ns	
Time from Latch Enable to HV_{OUT}	t_{ON}, t_{OFF}	—	—	500	ns	C_L = 15 pF
Latch Enable Pulse Width	t_{WLE}	25	—	—	ns	
Delay Time Clock to Latch Enable Low to High	t_{DLE}	25	—	—	ns	**Note 1**
Latch Enable Set-Up Time before Clock Rises	t_{SLE}	0	—	—	ns	
Delay Time Clock to Data Low to High	t_{DLH}	—	—	70	ns	C_L = 15 pF
Delay Time Clock to Data High to Low	t_{DHL}	—	—	70	ns	C_L = 15 pF

Note 1: t_{DLE} is not required but recommended to produce stable high-voltage outputs and thus minimize power dissipation and current spikes. t_{DLE} allows internal SR output to stabilize.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
80-lead PQFP	θ_{JA}	—	37	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV57708 are listed on Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT24/41	High-voltage output
2	HVOUT23/42	High-voltage output
3	HVOUT22/43	High-voltage output
4	HVOUT21/44	High-voltage output
5	HVOUT20/45	High-voltage output
6	HVOUT19/46	High-voltage output
7	HVOUT18/47	High-voltage output
8	HVOUT17/48	High-voltage output
9	HVOUT16/49	High-voltage output
10	HVOUT15/50	High-voltage output
11	HVOUT14/51	High-voltage output
12	HVOUT13/52	High-voltage output
13	HVOUT12/53	High-voltage output
14	HVOUT11/54	High-voltage output
15	HVOUT10/55	High-voltage output
16	HVOUT9/56	High-voltage output
17	HVOUT8/57	High-voltage output
18	HVOUT7/58	High-voltage output
19	HVOUT6/59	High-voltage output
20	HVOUT5/60	High-voltage output
21	HVOUT4/61	High-voltage output
22	HVOUT3/62	High-voltage output
23	HVOUT2/63	High-voltage output
24	HVOUT1/64	High-voltage output
25	DIN1/DOUT4(A)	Data Input 1/Output 4 A pin
26	DIN2/DOUT3(A)	Data Input 2/Output 3 A pin
27	DIN3/DOUT2(A)	Data Input 3/Output 2 A pin
28	DIN4/DOUT1(A)	Data Input 4/Output 1 A pin
29	$\overline{LE}$	Latch enable pin
30	CLK	Clock pin
31	$\overline{BL}$	Blanking pin
32	VDD	Low-voltage supply voltage
33	DIR	Direction pin (**Note**)
34	GND	Ground

Note: Pin designation for DIR = H/L
Example: For DIR = H, pin 41 is HVOUT6
For DIR = L, pin 41 is HVOUT1
For clockwise and counter-clockwise shifts, see Table 3-2 $Q_N \rightarrow Q_{N+1}$.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
35	$\overline{POL}$	Polarity pin
36	DOUT4/DIN1(B)	Data Output 4/Input 1 B pin
37	DOUT3/DIN2(B)	Data Output 3/Input 2 B pin
38	DOUT2/DIN3(B)	Data Output 2/Input 3 B pin
39	DOUT1/DIN4(B)	Data Output 1/Input 4 B pin
40	VPP	High-voltage supply voltage
41	HVOUT64/1	High-voltage output
42	HVOUT63/2	High-voltage output
43	HVOUT62/3	High-voltage output
44	HVOUT61/4	High-voltage output
45	HVOUT60/5	High-voltage output
46	HVOUT59/6	High-voltage output
47	HVOUT58/7	High-voltage output
48	HVOUT57/8	High-voltage output
49	HVOUT56/9	High-voltage output
50	HVOUT55/10	High-voltage output
51	HVOUT54/11	High-voltage output
52	HVOUT53/12	High-voltage output
53	HVOUT52/13	High-voltage output
54	HVOUT51/14	High-voltage output
55	HVOUT50/15	High-voltage output
56	HVOUT49/16	High-voltage output
57	HVOUT48/17	High-voltage output
58	HVOUT47/18	High-voltage output
59	HVOUT46/19	High-voltage output
60	HVOUT45/20	High-voltage output
61	HVOUT44/21	High-voltage output
62	HVOUT43/22	High-voltage output
63	HVOUT42/23	High-voltage output
64	HVOUT41/24	High-voltage output
65	HVOUT40/25	High-voltage output
66	HVOUT39/26	High-voltage output
67	HVOUT38/27	High-voltage output
68	HVOUT37/28	High-voltage output
69	HVOUT36/29	High-voltage output
70	HVOUT35/30	High-voltage output
71	HVOUT34/31	High-voltage output
72	HVOUT33/32	High-voltage output

Note: Pin designation for DIR = H/L
Example: For DIR = H, pin 41 is HVOUT6
For DIR = L, pin 41 is HVOUT1
For clockwise and counter-clockwise shifts, see Table 3-2 $Q_N \rightarrow Q_{N+1}$.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
73	HVOUT32/33	High-voltage output
74	HVOUT31/34	High-voltage output
75	HVOUT30/35	High-voltage output
76	HVOUT29/36	High-voltage output
77	HVOUT28/37	High-voltage output
78	HVOUT27/38	High-voltage output
79	HVOUT26/39	High-voltage output
80	HVOUT25/40	High-voltage output

Note: Pin designation for DIR = H/L
Example: For DIR = H, pin 41 is HVOUT6
For DIR = L, pin 41 is HVOUT1
For clockwise and counter-clockwise shifts, see Table 3-2 $Q_N \rightarrow Q_{N+1}$.

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV57708.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-Up		Power-Down	
Step	**Description**	**Step**	**Description**
1	Connect ground.	1	Remove $V_{PP.}$ (**Note 1**)
2	Apply $V_{DD.}$	2	Remove all inputs.
3	Set all inputs (Data, CLK, Enable, etc.) to a known state.	3	Remove $V_{DD.}$
4	Apply $V_{PP.}$ (**Note 1**)	4	Disconnect ground.

Note 1: The V_{PP} should not drop below V_{DD} or float during operation.

TABLE 3-2: TRUTH FUNCTION TABLE

Function	Inputs						Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Register	High-Voltage Output	Data Out
All O/P High	X	X	X	L	L	X	—	H	—
All O/P Low	X	X	X	L	H	X	—	L	—
O/P Normal	X	X	X	H	H	X	—	No inversion	—
O/P Inverted	X	X	X	H	L	X	—	Inversion	—
Data falls through Transparent Latches	L	↑	H	H	H	X	L	L	—
	H	↑	H	H	H	X	H	H	—
	L	↑	H	H	L	X	L	H	—
	H	↑	H	H	L	X	H	L	—
Data Stored/ Latches Loaded	X	X	L	H	H	X	*	Stored data	—
	X	X	L	H	L	X	*	Inversion of stored data	—
I/O Relation	$D_{I/O}1–4A$	↑	H	H	H	H	$Q_N \rightarrow Q_{N+1}$	New H or L	$D_{I/O}1–4B$
	$D_{I/O}1–4A$	↑	L	H	H	H	$Q_N \rightarrow Q_{N+1}$	Previous H or L	$D_{I/O}1–4B$
	$D_{I/O}1–4B$	↑	L	H	H	L	$Q_N \rightarrow Q_{N–1}$	Previous H or L	$D_{I/O}1–4A$
	$D_{I/O}1–4B$	↑	H	H	H	L	$Q_N \rightarrow Q_{N–1}$	New H or L	$D_{I/O}1–4A$

Note: H = High-logic level
L = Low-logic level
X = Irrelevant
↑ = Low-to-high transition
* = Dependent on the previous stage's state. See Table 2-1 for D_{IN} and D_{OUT} pin designation for clockwise and counter-clockwise shifts.

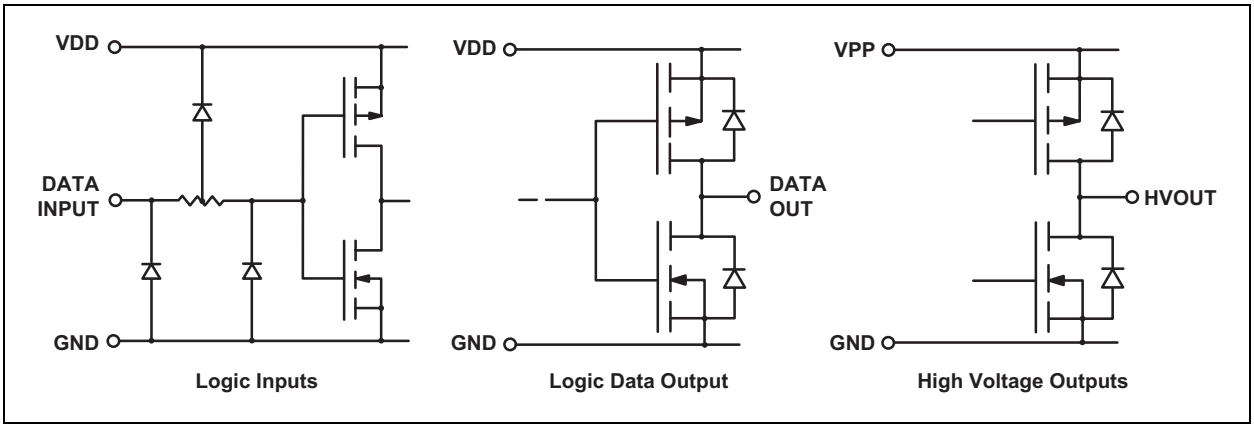


FIGURE 3-1: *Input and Output Equivalent Circuits.*

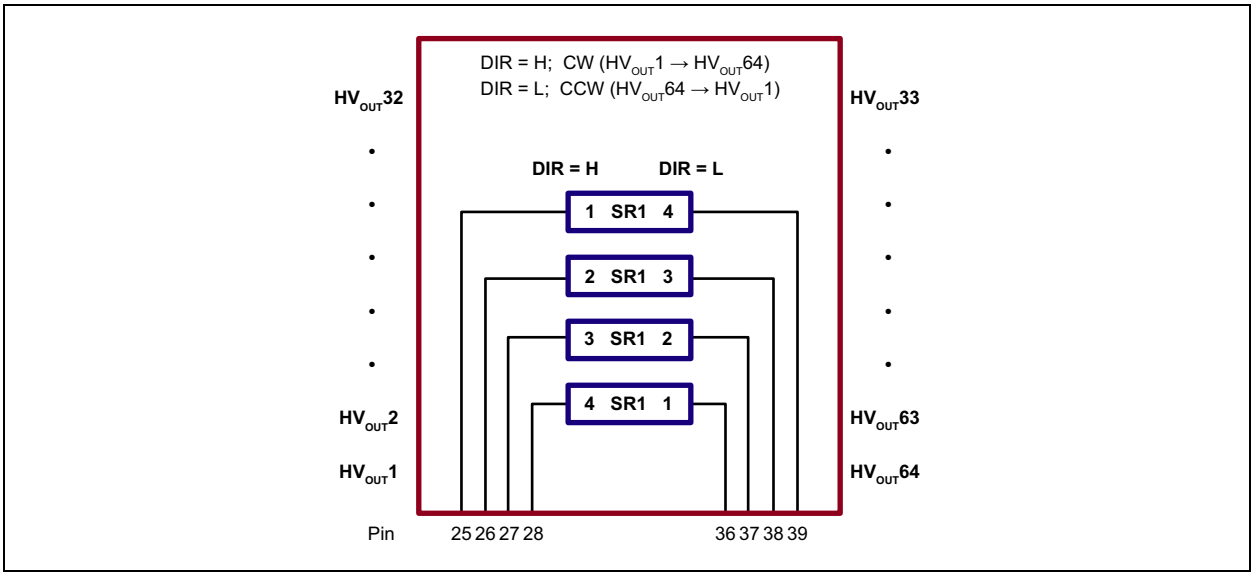
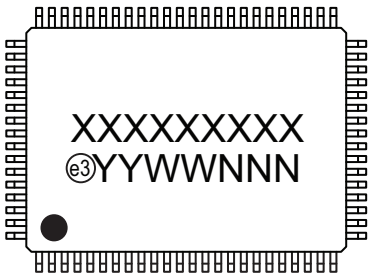


FIGURE 3-2: *Shift Register Operation.*

4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

80-lead PQFP



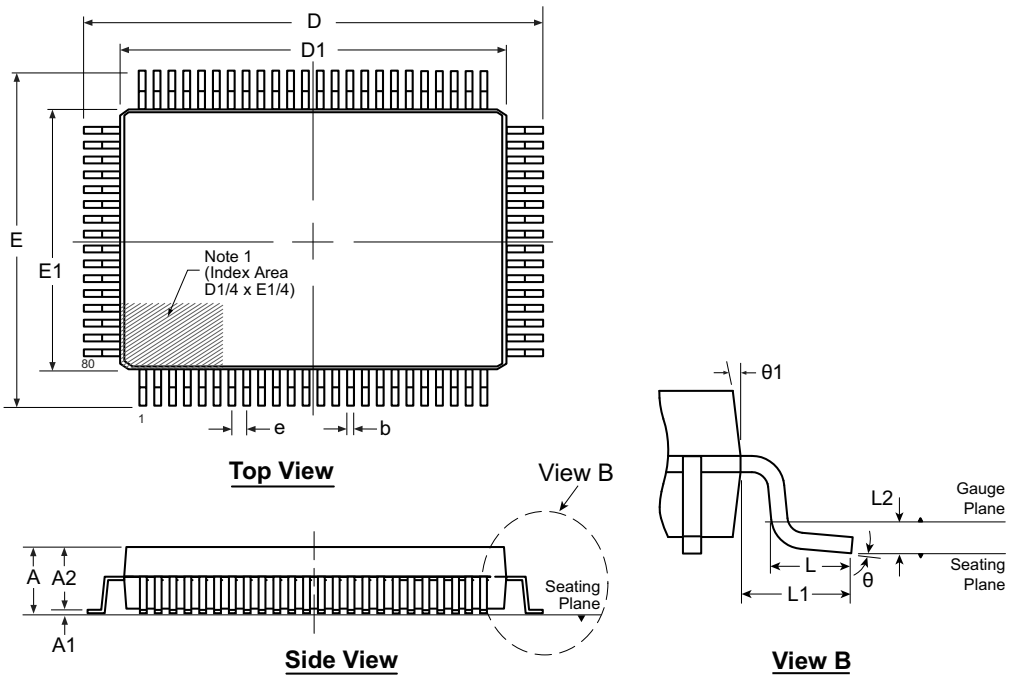
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

80-Lead PQFP Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CB-1, Issue B, Sept.1995.

** This dimension is not specified in the JEDEC drawing.*

Drawings not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2018)

- Converted Supertex Doc # DSFP-HV57708 to Microchip DS20005861A
- Removed “HVCMOS® Technology” in the Features section
- Changed the package marking format
- Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV57708	=	64-Channel 32 MHz Serial-to-Parallel Converter with Push-Pull Outputs
Package:	PG	=	80-lead PQFP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	66/Tray for a PG Package

Example:

a) HV57708PG-G:	64-Channel 32 MHz Serial-to-Parallel Converter with Push-Pull Outputs, 80-lead PQFP, 66/Tray

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