Features

- ESD/EFT/Surge Protection for 1 Line with Bi-directional.
- Provide ESD protection for each line to
  IEC 61000-4-2 (ESD) ±25kV (air / contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 16A (8/20μs)
- Suitable for**, 3.3V and below,** operating voltage applications
- **0201 small CSP package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- Mobile Phones
- Hand Held Portable Applications
- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Port Protection
- Control Signal Lines Protection
- Power Lines on PCB Protection
- Latchup Protection

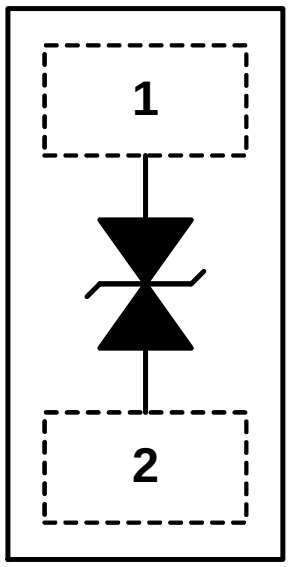
Description

AZ5A83-01B is a design which includes a bi-directional ESD rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ5A83-01B has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ5A83-01B is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5A83-01B may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



CSP0603P2Y (Top View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs)	I_{PP}	16	A
Operating Supply Voltage (pin-1 to pin-2)	V_{DC}	±3.6	V
Pin-1 to pin-2 ESD per IEC 61000-4-2 (Air) Pin-1 to pin-2 ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±25 ±25	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

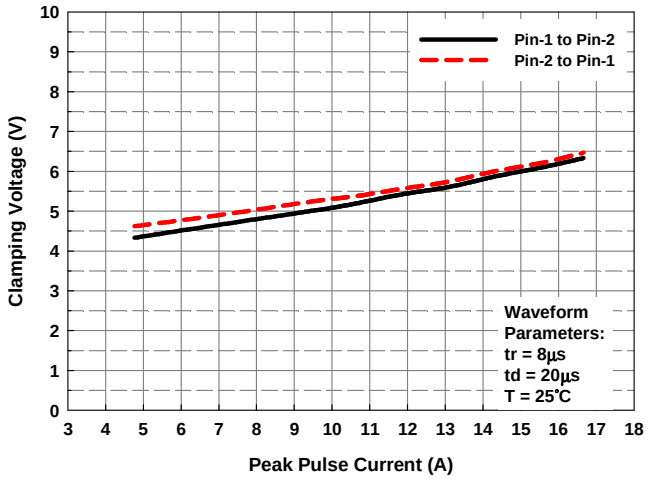
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	T=25 °C.	-3.3		3.3	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = ±3.3V, T=25 °C.			0.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C.	4			V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP}=5A, tp=8/20μs, T=25 °C.		4.5		V
ESD Clamping Voltage (Note 1)	V_{clamp}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), Contact mode, T=25 °C..		5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, T=25 °C, Contact mode.		0.03		Ω
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 °C.		52.5	65	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

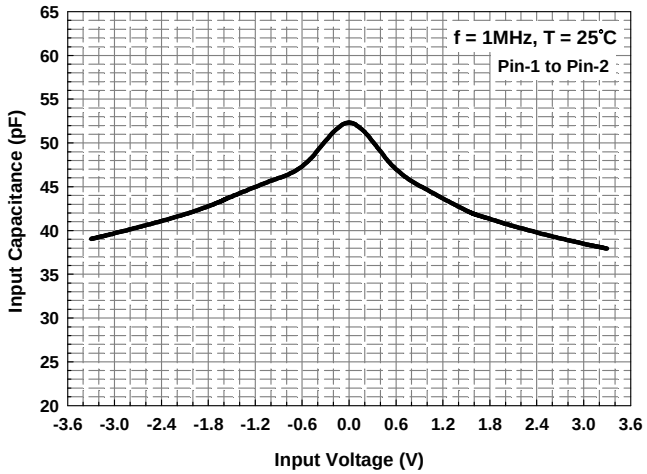
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

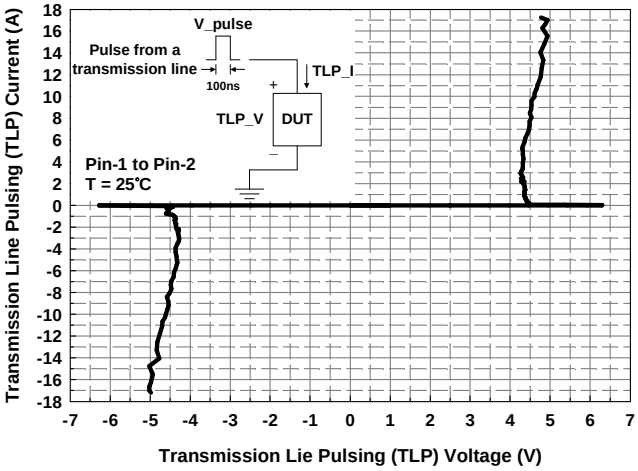
Reverse Clamping Voltage vs. Peak Pulse Current



Typical Variation of C_{IN} vs. V_{IN}



Transmission Line Pulsing (TLP) Measurement



Applications Information

The AZ5A83-01B is designed to protect one line against System ESD/EFT/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5A83-01B is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5A83-01B should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5A83-01B.
- Place the AZ5A83-01B near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

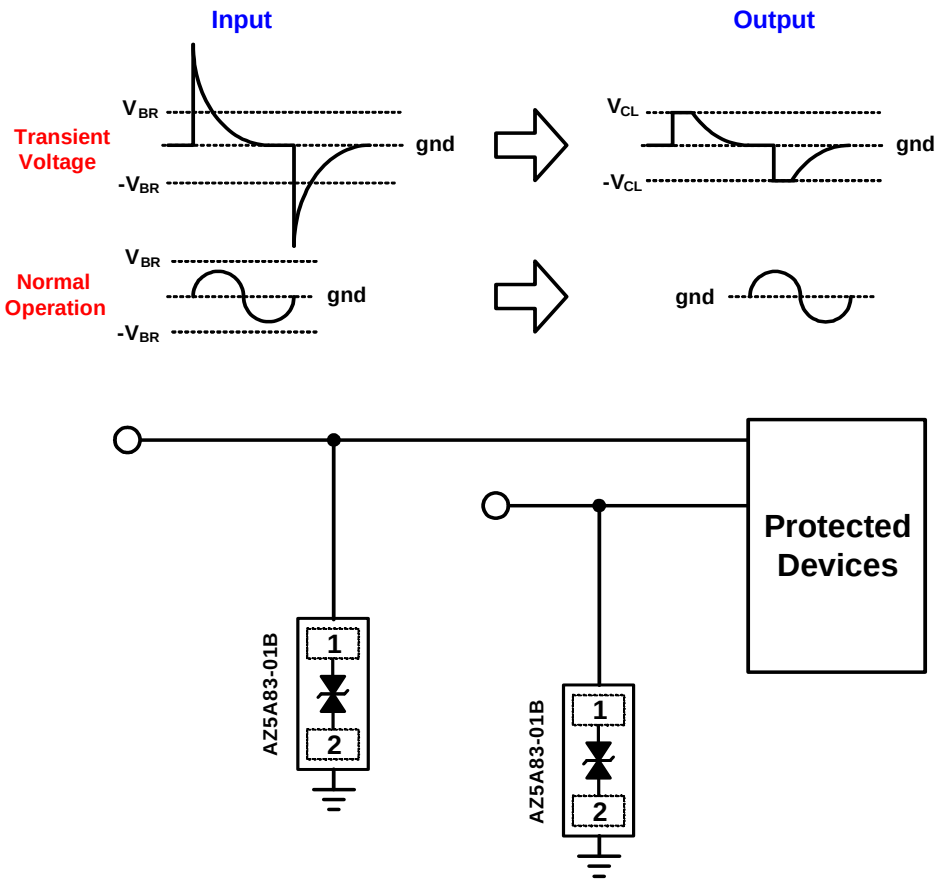


Fig. 1

Fig. 2 shows another simplified example of using AZ5A83-01B to protect the control line, low speed data line, and power line from ESD transient stress.

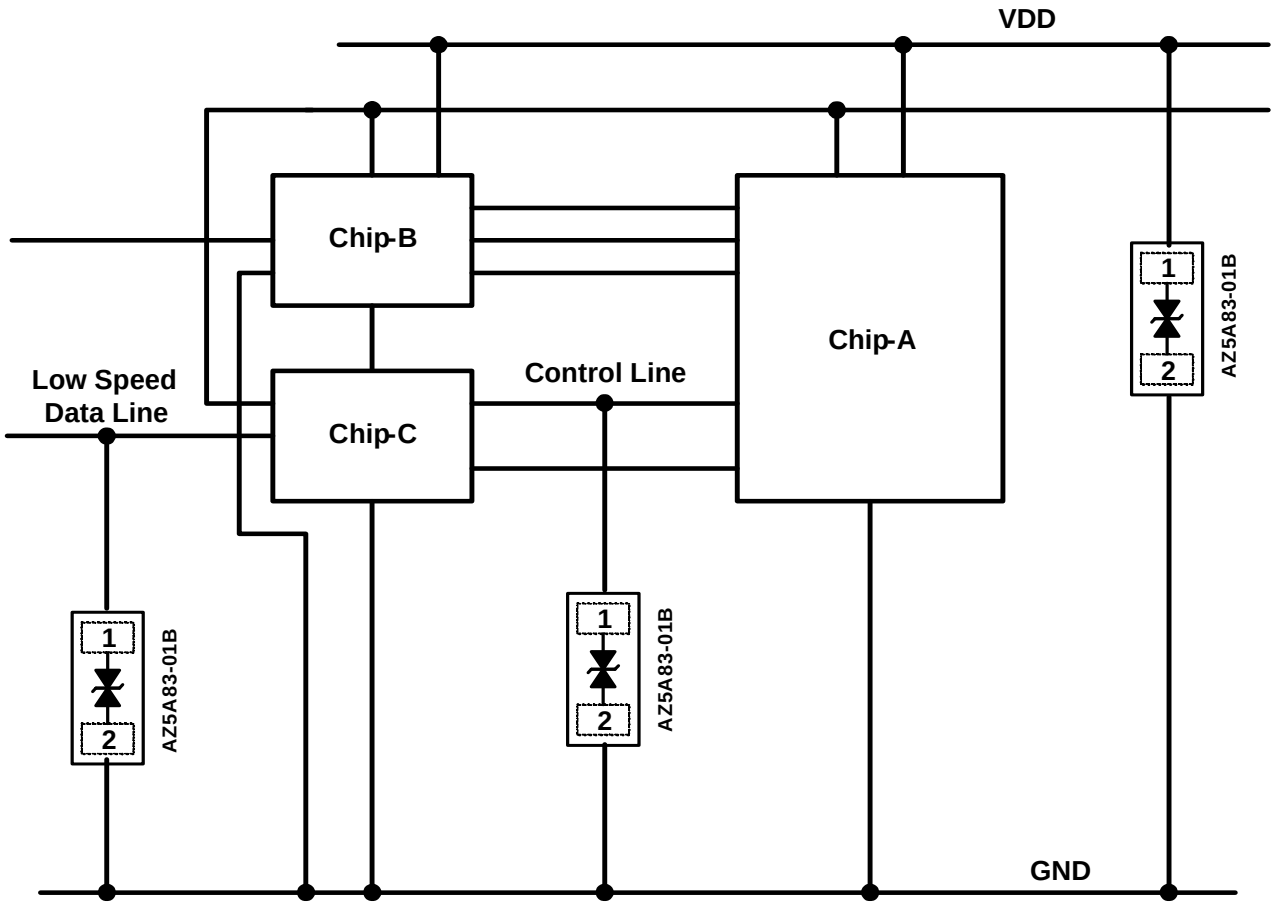


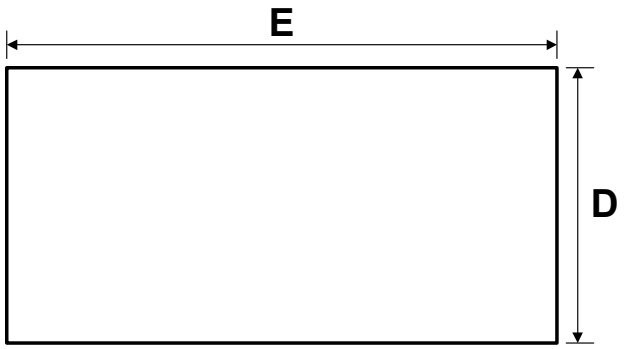
Fig. 2

Mechanical Details

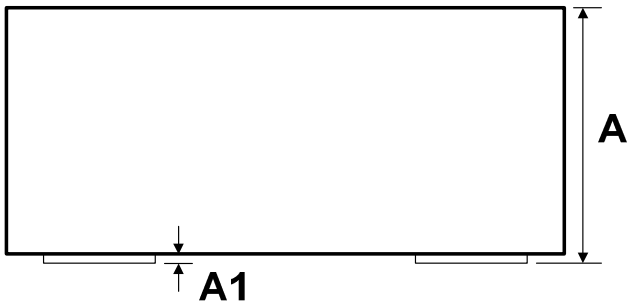
CSP0603P2Y

PACKAGE DIAGRAMS

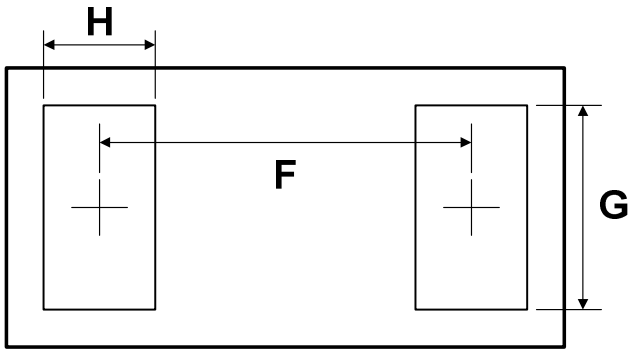
TOP VIEW



SIDE VIEW



BOTTOM VIEW

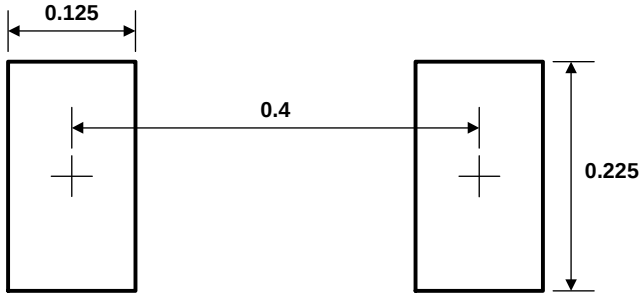


PACKAGE DIMENSIONS

Symbol	Millimeters		
	MIN.	TYP.	MAX.
D	0.275	0.300	0.325
E	0.575	0.600	0.625
A	0.256	0.276	0.296
A1		0.011	
F		0.400	
G	0.210	0.220	0.230
H	0.110	0.120	0.130

LAND LAYOUT

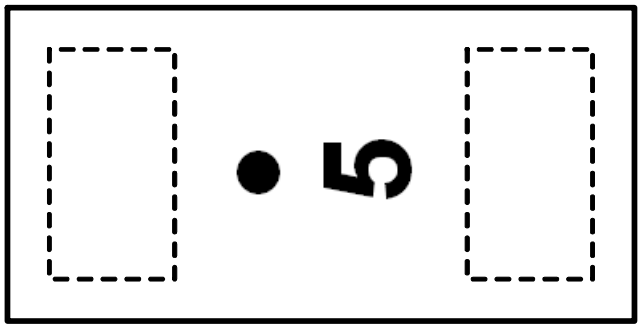
Unit: mm



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Part Number	Marking Code
AZ5A83-01B.R7G (Green Part)	5

Note : Green means Pb-free, RoHS, and Halogen free compliant.

5 = Device Code

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5A83-01B.R7G	Green	T/R	7 inch	15,000/reel	4 reels = 60,000/box	6 boxes = 360,000/carton

Revision History

Revision	Modification Description
Revision 2015/07/07	Preliminary Release.
Revision 2016/07/15	Revised Description.
Revision 2017/04/25	Formal Release.