# ESP32-WROVER-E & ESP32-WROVER-IE

## Datasheet

Version 1.8

Espressif Systems

# About This Document

This document provides the specifications for the ESP32-WROVER-E and ESP32-WROVER-IE modules.

## Document Updates

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## Revision History

For revision history of this document, please refer to the last page.

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# 1 Overview

ESP32-WROVER-E and ESP32-WROVER-IE are two powerful, generic Wi-Fi + Bluetooth + Bluetooth LE MCU modules that target a wide variety of applications, ranging from low-power sensor networks to the most demanding tasks, such as voice encoding, music streaming and MP3 decoding.

ESP32-WROVER-E comes with a PCB antenna, and ESP32-WROVER-IE with a connector for an external antenna. **The information in this datasheet is applicable to both modules.**

The Series Comparison for the two modules is as follows:

**Table 1: ESP32-WROVER-E Series Comparison[1]**

| Ordering Code | Flash | PSRAM | Ambient Temp.[2] (°C) | Size[3] (mm) |
|---|---|---|---|---|
| ESP32-WROVER-E-N4R8 | 4 MB (Quad SPI) | 8 MB (Quad SPI) | –40 ~ 85 | 18.0 x 31.4 x 3.3 |
| ESP32-WROVER-E-N8R8 | 8 MB (Quad SPI) | 8 MB (Quad SPI) | –40 ~ 85 | |
| ESP32-WROVER-E-N16R8 | 16 MB (Quad SPI) | 8 MB (Quad SPI) | –40 ~ 85 | |
| ESP32-WROVER-E-N4R2 | 4 MB (Quad SPI) | 2 MB (Quad SPI)[4] | –40 ~ 85 | |
| ESP32-WROVER-E-N8R2 | 8 MB (Quad SPI) | 2 MB (Quad SPI)[4] | –40 ~ 85 | |
| ESP32-WROVER-E-N16R2 | 16 MB (Quad SPI) | 2 MB (Quad SPI)[4] | –40 ~ 85 | |

[1] This table shares the same notes presented in the table 2 below.

**Table 2: ESP32-WROVER-IE Series Comparison**

| Ordering Code | Flash | PSRAM | Ambient Temp.[2] (°C) | Size[3] (mm) |
|---|---|---|---|---|
| ESP32-WROVER-IE-N4R8 | 4 MB (Quad SPI) | 8 MB (Quad SPI) | –40 ~ 85 | 18.0 x 31.4 x 3.3 |
| ESP32-WROVER-IE-N8R8 | 8 MB (Quad SPI) | 8 MB (Quad SPI) | –40 ~ 85 | |
| ESP32-WROVER-IE-N16R8 | 16 MB (Quad SPI) | 8 MB (Quad SPI) | –40 ~ 85 | |
| ESP32-WROVER-IE-N4R2 | 4 MB (Quad SPI) | 2 MB (Quad SPI)[4] | –40 ~ 85 | |
| ESP32-WROVER-IE-N8R2 | 8 MB (Quad SPI) | 2 MB (Quad SPI)[4] | –40 ~ 85 | |
| ESP32-WROVER-IE-N16R2 | 16 MB (Quad SPI) | 2 MB (Quad SPI)[4] | –40 ~ 85 | |

[2] Ambient temperature specifies the recommended temperature range of the environment immediately outside the Espressif module.

[3] For details, refer to Section 9 *Physical Dimensions*.

[4] This module uses PSRAM integrated in the chip's package.

At the core of the module is the ESP32-D0WD-V3 chip or ESP32-D0WDR2-V3 chip*. The chip embedded is designed to be scalable and adaptive. There are two CPU cores that can be individually controlled, and the CPU clock frequency is adjustable from 80 MHz to 240 MHz. The chip also has a low-power coprocessor that can be used instead of the CPU to save power while performing tasks that do not require much computing power, such as monitoring of peripherals. ESP32 integrates a rich set of peripherals, ranging from capacitive touch sensors, SD card interface, Ethernet, high-speed SPI, UART, I2S and I2C.

**Note:**

* For details on the part numbers of the ESP32 family of chips, please refer to the document *ESP32 Datasheet*.

The integration of Bluetooth®, Bluetooth LE and Wi-Fi ensures that a wide range of applications can be targeted, and that the module is all-around: using Wi-Fi allows a large physical range and direct connection to the Internet through a Wi-Fi router, while using Bluetooth allows the user to conveniently connect to the phone or broadcast low energy beacons for its detection. The sleep current of the ESP32 chip is less than 5 $\mu$A, making it suitable for battery powered and wearable electronics applications. The module supports a data rate of up to 150 Mbps, and 20 dBm output power at the antenna to ensure the widest physical range. As such the module does offer industry-leading specifications and the best performance for electronic integration, range, power consumption, and connectivity.

The operating system chosen for ESP32 is freeRTOS with LwIP; TLS 1.2 with hardware acceleration is built in as well. Secure (encrypted) over the air (OTA) upgrade is also supported, so that users can upgrade their products even after their release, at minimum cost and effort.

Table 3 provides the specifications of the two modules.

**Table 3: ESP32-WROVER-E & ESP32-WROVER-IE Specifications**

| Categories | Items | Specifications |
|---|---|---|
| Certification | RF certification | See certificates for ESP32-WROVER-E and ESP32-WROVER-IE |
| Test | Reliablity | HTOL/HTSL/uHAST/TCT/ESD |
| Wi-Fi | Protocols | 802.11 b/g/n (802.11n up to 150 Mbps) |
| | | A-MPDU and A-MSDU aggregation and 0.4 $\mu$s guard interval support |
| | Center frequency range of operating channel | 2412 ~ 2484 MHz |
| Bluetooth | Protocols | Bluetooth v4.2 BR/EDR and Bluetooth LE specification |
| | Radio | NZIF receiver with –97 dBm sensitivity |
| | | Class-1, class-2 and class-3 transmitter |
| | | AFH |
| | Audio | CVSD and SBC |
| Hardware | Module interfaces | SD card, UART, SPI, SDIO, I2C, LED PWM, Motor PWM, I2S, IR, pulse counter, GPIO, capacitive touch sensor, ADC, DAC, Two-Wire Automotive Interface (TWAI®), compatible with ISO11898-1 (CAN Specification 2.0) |
| | Integrated crystal | 40 MHz crystal |
| | Integrated SPI flash | See Table 1 and Table 2 |
| | Integrated PSRAM | See Table 1 and Table 2 |
| | Operating voltage/Power supply | 3.0 V ~ 3.6 V |
| | Minimum current delivered by power supply | 500 mA |
| | Package size | (18.00±0.15) mm × (31.40±0.15) mm × (3.30±0.15) mm |
| | Moisture sensitivity level (MSL) | Level 3 |

# 2 Block Diagram

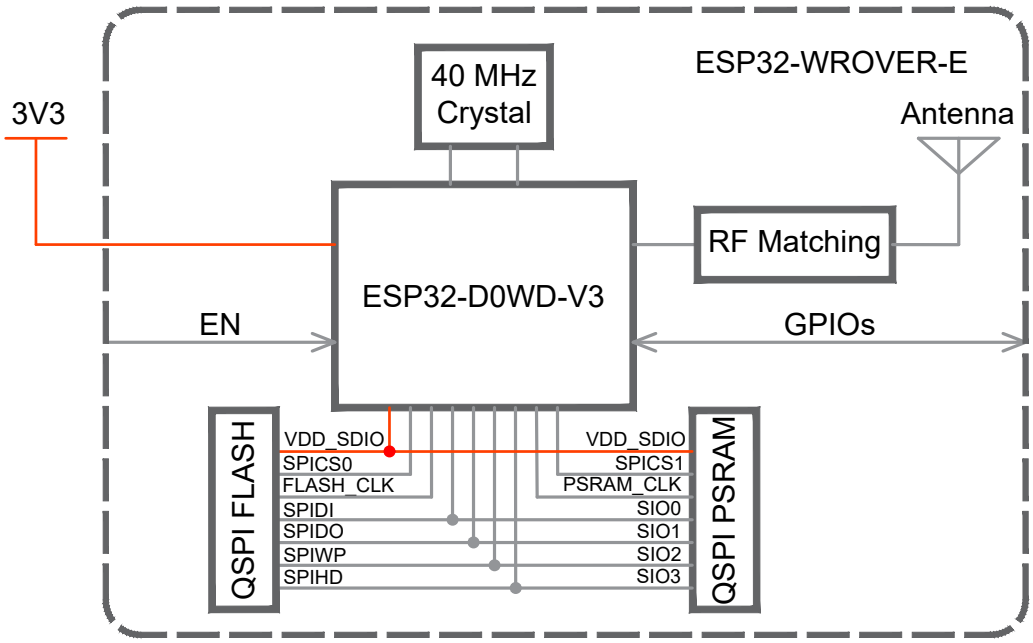



**Figure 1: ESP32-WROVER-E Block Diagram (with ESP32-D0WD-V3 embedded)**

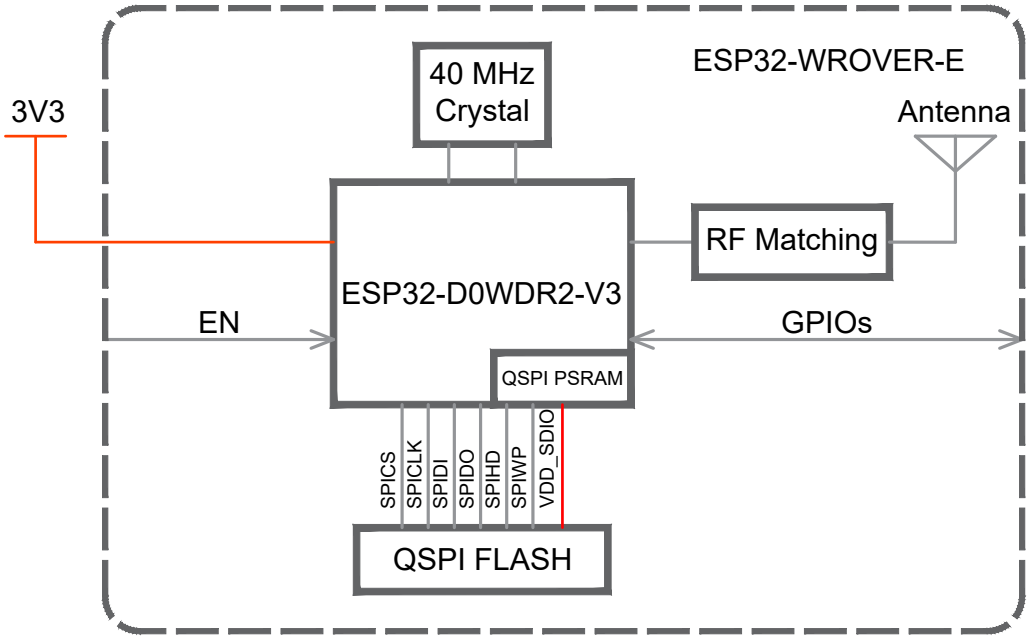



**Figure 2: ESP32-WROVER-E Block Diagram (with ESP32-D0WDR2-V3 embedded)**

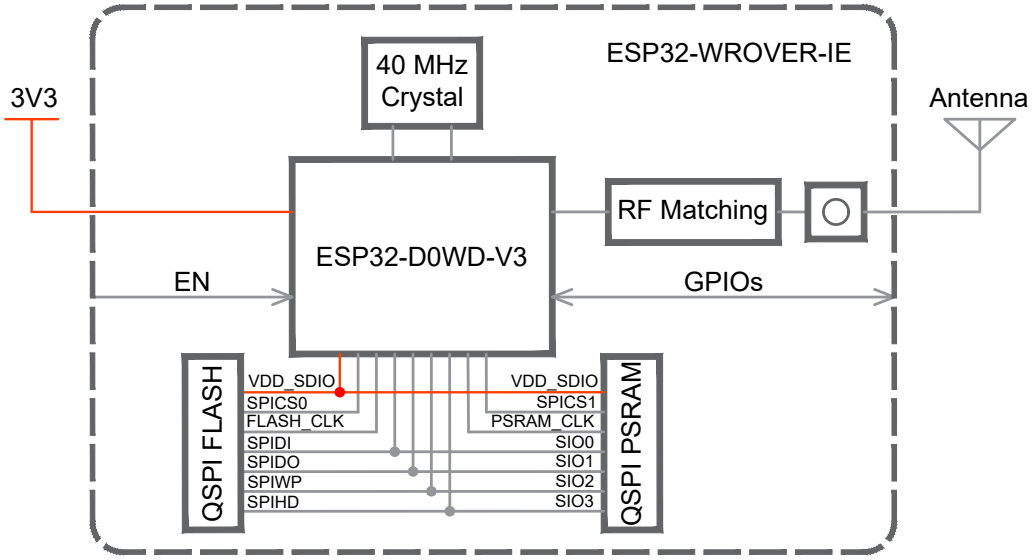



**Figure 3: ESP32-WROVER-IE Block Diagram (with ESP32-D0WD-V3 embedded)**

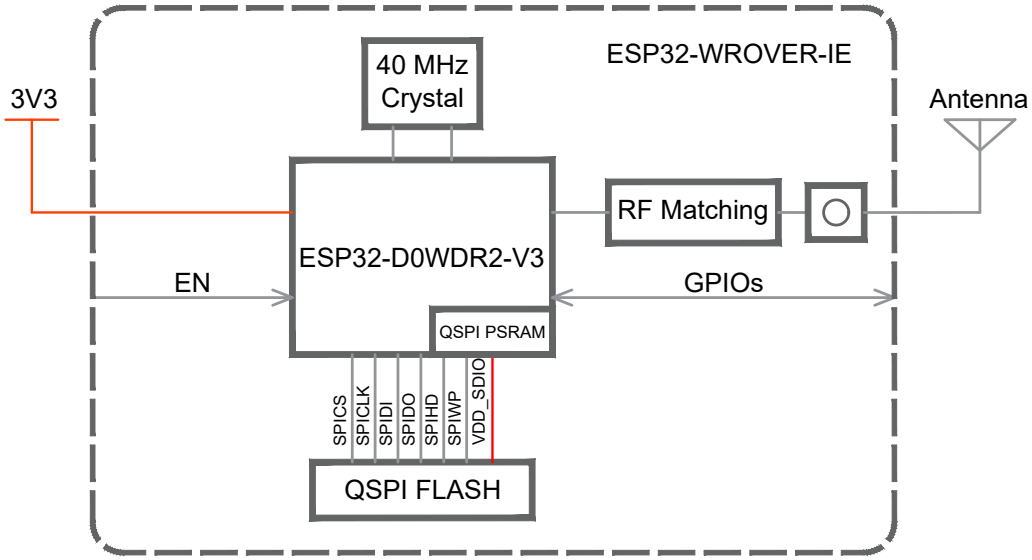



**Figure 4: ESP32-WROVER-IE Block Diagram (with ESP32-D0WDR2-V3 embedded)**

# 3 Pin Definitions

## 3.1 Pin Layout

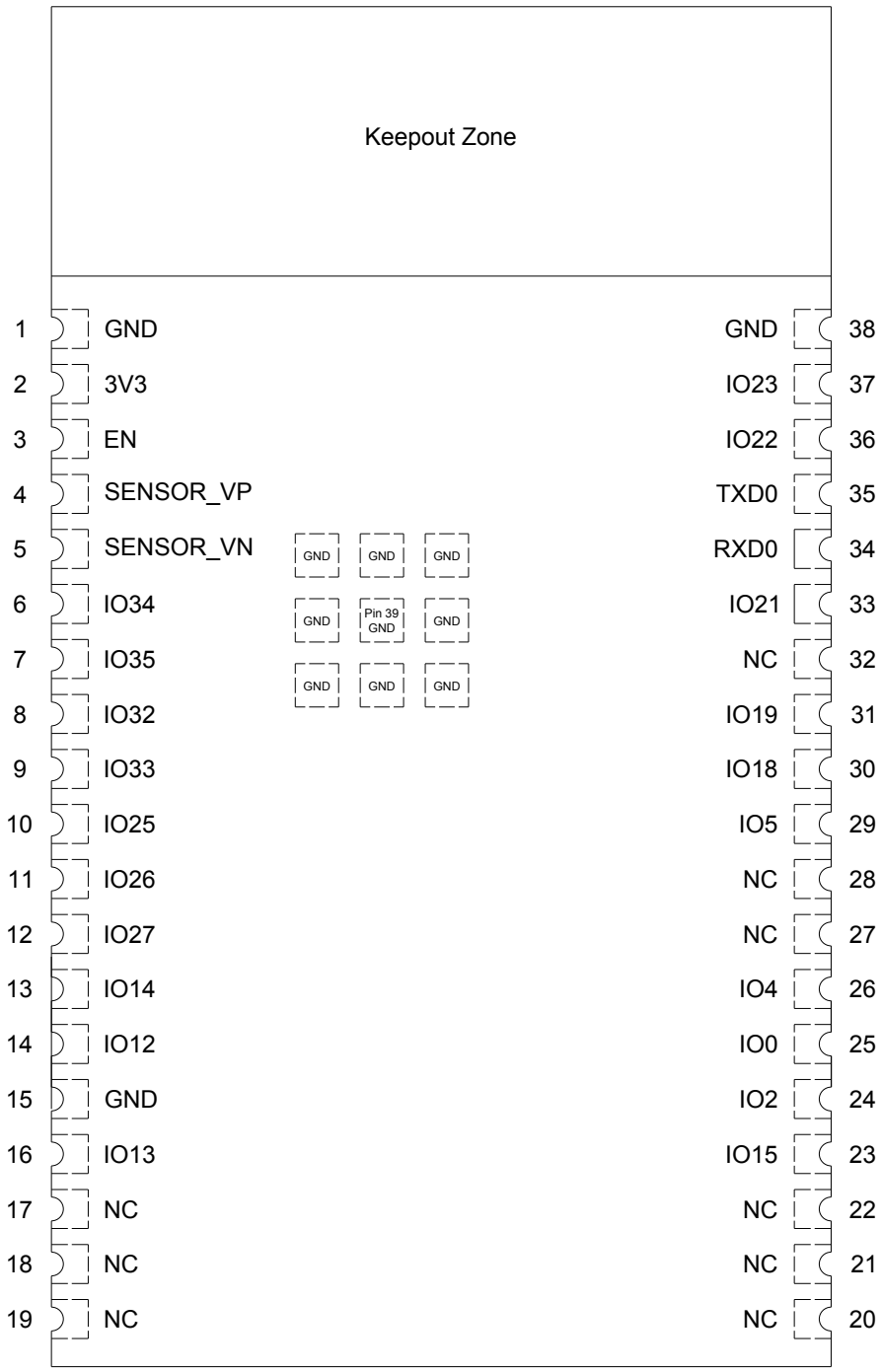



**Figure 5: Pin Layout (Top View)**

## 3.2 Pin Description

The module has 38 pins. See pin definitions in Table 4.

**Table 4: Pin Definitions**

| Name | No. | Type | Function |
|---|---|---|---|
| GND | 1 | P | Ground |
| 3V3 | 2 | P | Power supply |
| EN | 3 | I | Module-enable signal. Active high. |
| SENSOR_VP | 4 | I | GPIO36, ADC1_CH0, RTC_GPIO0 |
| SENSOR_VN | 5 | I | GPIO39, ADC1_CH3, RTC_GPIO3 |
| IO34 | 6 | I | GPIO34, ADC1_CH6, RTC_GPIO4 |
| IO35 | 7 | I | GPIO35, ADC1_CH7, RTC_GPIO5 |
| IO32 | 8 | I/O | GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9 |
| IO33 | 9 | I/O | GPIO33, XTAL_32K_N (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8 |
| IO25 | 10 | I/O | GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0 |
| IO26 | 11 | I/O | GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1 |
| IO27 | 12 | I/O | GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV |
| IO14 | 13 | I/O | GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2 |
| IO12 | 14 | I/O | GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3 |
| GND | 15 | P | Ground |
| IO13 | 16 | I/O | GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER |
| NC * | 17 | - | - |
| NC * | 18 | - | - |
| NC * | 19 | - | - |
| NC * | 20 | - | - |
| NC * | 21 | - | - |
| NC * | 22 | - | - |
| IO15 | 23 | - | GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3 |
| IO2 | 24 | I/O | GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0 |
| IO0 | 25 | I/O | GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK |
| IO4 | 26 | I/O | GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER |
| NC | 27 | - | - |
| NC | 28 | - | - |
| IO5 | 29 | I/O | GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK |
| IO18 | 30 | I/O | GPIO18, VSPICLK, HS1_DATA7 |
| IO19 | 31 | I/O | GPIO19, VSPIQ, U0CTS, EMAC_TXD0 |
| NC | 32 | - | - |
| IO21 | 33 | I/O | GPIO21, VSPIHD, EMAC_TX_EN |

| Name | No. | Type | Function |
|---|---|---|---|
| RXD0 | 34 | I/O | GPIO3, U0RXD, CLK_OUT2 |
| TXD0 | 35 | I/O | GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2 |
| IO22 | 36 | I/O | GPIO22, VSPIWP, U0RTS, EMAC_TXD1 |
| IO23 | 37 | I/O | GPIO23, VSPID, HS1_STROBE |
| GND | 38 | P | Ground |

**Notice:**

* Pins GPIO6 to GPIO11 on the ESP32-D0WD-V3/ESP32-D0WDR2-V3 chip are connected to the SPI flash integrated on the module and are not led out.

## 3.3 Strapping Pins

ESP32 has five strapping pins, which can be seen in Chapter 7 Schematics:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

Software can read the values of these five bits from register "GPIO_STRAPPING".

During the chip's system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device's boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32.

After reset release, the strapping pins work as normal-function pins.

Refer to Table 5 for a detailed boot-mode configuration by strapping pins.

**Table 5: Strapping Pins**

| Voltage of Internal LDO (VDD_SDIO) | | | |
|---|---|---|---|
| Pin | Default | 3.3 V | 1.8 V |
| MTDI | Pull-down | 0 | 1 |
| Booting Mode | | | |
| Pin | Default | SPI Boot | Download Boot |
| GPIO0 | Pull-up | 1 | 0 |
| GPIO2 | Pull-down | Don't-care | 0 |

| Enabling/Disabling Debugging Log Print over U0TXD During Booting | | | |
|---|---|---|---|
| Pin | Default | U0TXD Active | U0TXD Silent |
| MTDO | Pull-up | 1 | 0 |

| Timing of SDIO Slave | | | | | |
|---|---|---|---|---|---|
| Pin | Default | FE Sampling FE Output | FE Sampling RE Output | RE Sampling FE Output | RE Sampling RE Output |
| MTDO | Pull-up | 0 | 0 | 1 | 1 |
| GPIO5 | Pull-up | 0 | 1 | 0 | 1 |

**Note:**

- FE: falling-edge, RE: rising-edge.
- Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave" after booting.
- Internal pull-up resistor (R9) for MTDI is not populated in the module, as the flash and SRAM in the module only support a power voltage of 3.3 V (output by VDD_SDIO).

The illustration below shows the setup and hold times for the strapping pins before and after the CHIP_PU signal goes high. Details about the parameters are listed in Table 6.

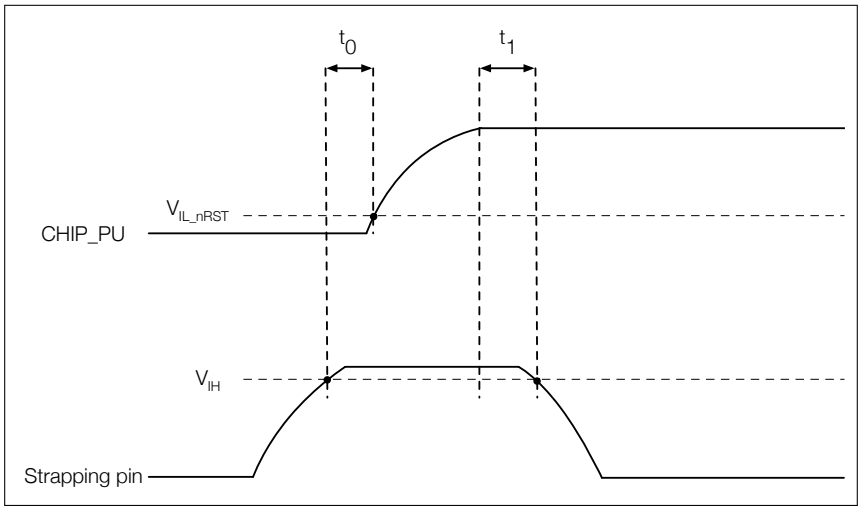



**Figure 6: Setup and Hold Times for the Strapping Pins**

**Table 6: Parameter Descriptions of Setup and Hold Times for the Strapping Pins**

| Parameters | Description | Min. | Unit |
|---|---|---|---|
| $t_0$ | Setup time before CHIP_PU goes from low to high | 0 | ms |
| $t_1$ | Hold time after CHIP_PU goes high | 1 | ms |

# 4 Functional Description

This chapter describes the modules and functions integrated in ESP32-WROVER-E and ESP32-WROVER-IE.

## 4.1 CPU and Internal Memory

ESP32-D0WD-V3 (or ESP32-D0WDR2-V3) contains two low-power Xtensa® 32-bit LX6 microprocessors. The internal memory includes:

- 448 KB of ROM for booting and core functions.
- 520 KB of on-chip SRAM for data and instructions.
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep-sleep mode.
- 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co-processor during the Deep-sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including flash-encryption and chip-ID.

## 4.2 External Flash and SRAM

ESP32 supports multiple external QSPI flash and SRAM chips. More details can be found in Chapter SPI in the *ESP32 Technical Reference Manual*. ESP32 also supports hardware encryption/decryption based on AES to protect developers' programs and data in flash.

ESP32 can access the external QSPI flash and SRAM through high-speed caches.

- The external flash can be mapped into CPU instruction memory space and read-only memory space simultaneously.
  - When external flash is mapped into CPU instruction memory space, up to 11 MB + 248 KB can be mapped at a time. Note that if more than 3 MB + 248 KB are mapped, cache performance will be reduced due to speculative reads by the CPU.
  - When external flash is mapped into read-only data memory space, up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads are supported.
- External SRAM can be mapped into CPU data memory space. Up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads and writes are supported.

## 4.3 Crystal Oscillators

The module uses a 40-MHz crystal oscillator.

## 4.4 RTC and Low-Power Management

With the use of advanced power-management technologies, ESP32 can switch between different power modes.

For details on ESP32's power consumption in different power modes, please refer to section "RTC and Low-Power Management" in *ESP32 Datasheet*.

# 5 Peripherals and Sensors

Please refer to Section *Peripherals and Sensors* in *ESP32 Datasheet*.

**Note:**

External connections can be made to any GPIO except for GPIOs in the range 6-11, 16, or 17. GPIOs 6-11 are connected to the module's integrated SPI flash. GPIOs 16 and 17 are connected to the module's integrated PSRAM. For details, please see Section 7 *Schematics*.

# 6 Electrical Characteristics

## 6.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the recommended operating conditions.

**Table 7: Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| VDD33 | Power supply voltage | –0.3 | 3.6 | V |
| $I_{output}$[1] | Cumulative IO output current | - | 1,100 | mA |
| $T_{store}$ | Storage temperature | –40 | 105 | °C |

1. The module worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO) output high logic level to ground. Please note that pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.
2. Please see Appendix *IO_MUX* in *ESP32 Datasheet* for IO's power domain.

## 6.2 Recommended Operating Conditions

**Table 8: Recommended Operating Conditions**

| Symbol | Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| VDD33 | Power supply voltage | 3.0 | 3.3 | 3.6 | V |
| $I_{VDD}$ | Current delivered by external power supply | 0.5 | - | - | A |
| T | Operating temperature | –40 | - | 85 | °C |

## 6.3 DC Characteristics (3.3 V, 25 °C)

**Table 9: DC Characteristics (3.3 V, 25 °C)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Pin capacitance | - | 2 | - | pF |
| $V_{IH}$ | High-level input voltage | 0.75×VDD[1] | - | VDD[1]+0.3 | V |
| $V_{IL}$ | Low-level input voltage | –0.3 | - | 0.25×VDD[1] | V |
| $I_{IH}$ | High-level input current | - | - | 50 | nA |
| $I_{IL}$ | Low-level input current | - | - | 50 | nA |
| $V_{OH}$ | High-level output voltage | 0.8×VDD[1] | - | - | V |
| $V_{OL}$ | Low-level output voltage | - | - | 0.1×VDD[1] | V |

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OH}$ | High-level source current (VDD[1] = 3.3 V, $V_{OH}$ >= 2.64 V, output drive strength set to the maximum) | VDD3P3_CPU power domain [1, 2] | - | 40 | - | mA |
| | | VDD3P3_RTC power domain [1, 2] | - | 40 | - | mA |
| | | VDD_SDIO power domain [1, 3] | - | 20 | - | mA |
| $I_{OL}$ | Low-level sink current (VDD[1] = 3.3 V, $V_{OL}$ = 0.495 V, output drive strength set to the maximum) | | - | 28 | - | mA |
| $R_{PU}$ | Resistance of internal pull-up resistor | | - | 45 | - | kΩ |
| $R_{PD}$ | Resistance of internal pull-down resistor | | - | 45 | - | kΩ |
| $V_{IL\_nRST}$ | Low-level input voltage of CHIP_PU to shut down the chip | | - | - | 0.6 | V |

**Notes:**

1. Please see Appendix *IO_MUX* in *ESP32 Datasheet* for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, $V_{OH}$>=2.64 V, as the number of current-source pins increases.
3. Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

## 6.4 Wi-Fi Radio

**Table 10: Wi-Fi Radio Characteristics**

| Parameter | Condition | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Center frequency range of operating channel [note1] | - | 2412 | - | 2484 | MHz |
| Output impedance [note2] | - | - | * | - | Ω |
| TX power [note3] | 11n, MCS7 | 12 | 13 | 14 | dBm |
| | 11b mode | 18.5 | 19.5 | 20.5 | dBm |
| Sensitivity | 11b, 1 Mbps | - | –97 | - | dBm |
| | 11b, 11 Mbps | - | –88 | - | dBm |
| | 11g, 6 Mbps | - | –92 | - | dBm |
| | 11g, 54 Mbps | - | –75 | - | dBm |
| | 11n, HT20, MCS0 | - | –92 | - | dBm |
| | 11n, HT20, MCS7 | - | –72 | - | dBm |
| | 11n, HT40, MCS0 | - | –89 | - | dBm |
| | 11n, HT40, MCS7 | - | –69 | - | dBm |
| Adjacent channel rejection | 11g, 6 Mbps | - | 27 | - | dB |
| | 11g, 54 Mbps | - | 13 | - | dB |
| | 11n, HT20, MCS0 | - | 27 | - | dB |
| | 11n, HT20, MCS7 | - | 12 | - | dB |

**Notes:**

1. Device should operate in the frequency range allocated by regional regulatory authorities. Target center operating frequency range is configurable by software.
2. For the modules that use external antennas, the output impedance is 50 Ω. For other modules without external antennas, users do not need to concern about the output impedance.
3. Target TX power is configurable based on device or certification requirements.

## 6.5 Bluetooth LE Radio

### 6.5.1 Receiver

**Table 11: Receiver Characteristics – Bluetooth LE**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Sensitivity @30.8% PER | - | –94 | –93 | –92 | dBm |
| Maximum received signal @30.8% PER | - | 0 | - | - | dBm |
| Co-channel C/I | - | - | +10 | - | dB |
| Adjacent channel selectivity C/I | F = F0 + 1 MHz | - | –5 | - | dB |
| | F = F0 – 1 MHz | - | –5 | - | dB |
| | F = F0 + 2 MHz | - | –25 | - | dB |
| | F = F0 – 2 MHz | - | –35 | - | dB |
| | F = F0 + 3 MHz | - | –25 | - | dB |
| | F = F0 – 3 MHz | - | –45 | - | dB |
| Out-of-band blocking performance | 30 MHz ~ 2000 MHz | –10 | - | - | dBm |
| | 2000 MHz ~ 2400 MHz | –27 | - | - | dBm |
| | 2500 MHz ~ 3000 MHz | –27 | - | - | dBm |
| | 3000 MHz ~ 12.5 GHz | –10 | - | - | dBm |
| Intermodulation | - | –36 | - | - | dBm |

### 6.5.2 Transmitter

**Table 12: Transmitter Characteristics – Bluetooth LE**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RF transmit power | - | - | 0 | - | dBm |
| Gain control step | - | - | 3 | - | dBm |
| RF power control range | - | –12 | - | +9 | dBm |
| Adjacent channel transmit power | F = F0 ± 2 MHz | - | –52 | - | dBm |
| | F = F0 ± 3 MHz | - | –58 | - | dBm |
| | F = F0 ± > 3 MHz | - | –60 | - | dBm |
| $\Delta f1_{avg}$ | - | - | - | 265 | kHz |
| $\Delta f2_{max}$ | - | 247 | - | - | kHz |
| $\Delta f2_{avg}/\Delta f1_{avg}$ | - | - | +0.92 | - | - |
| ICFT | - | - | –10 | - | kHz |
| Drift rate | - | - | 0.7 | - | kHz/50 $\mu$s |
| Drift | - | - | 2 | - | kHz |

# 7 Schematics

This is the reference design of the module.

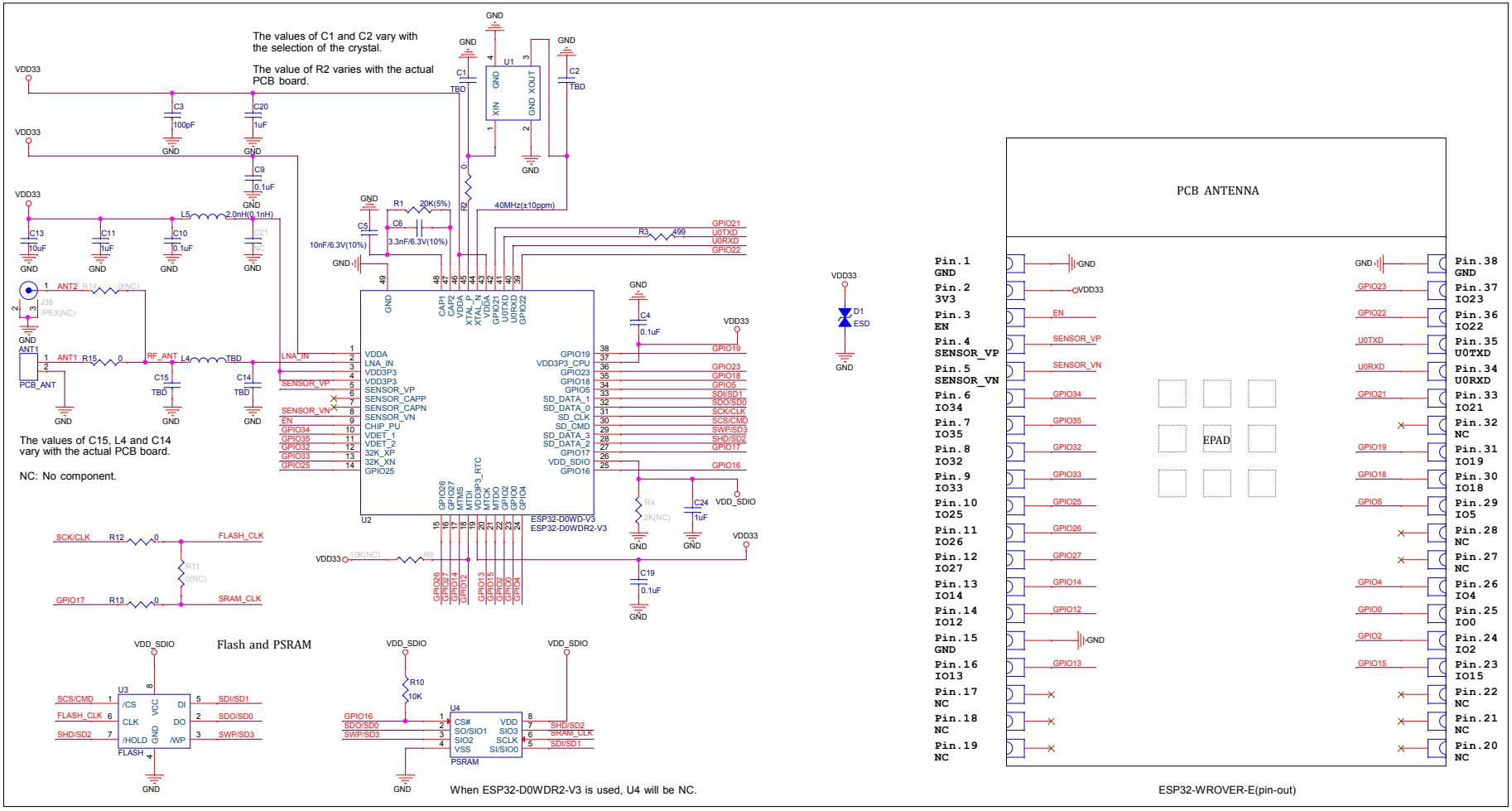



Figure 7: Schematics of ESP32-WROVER-E

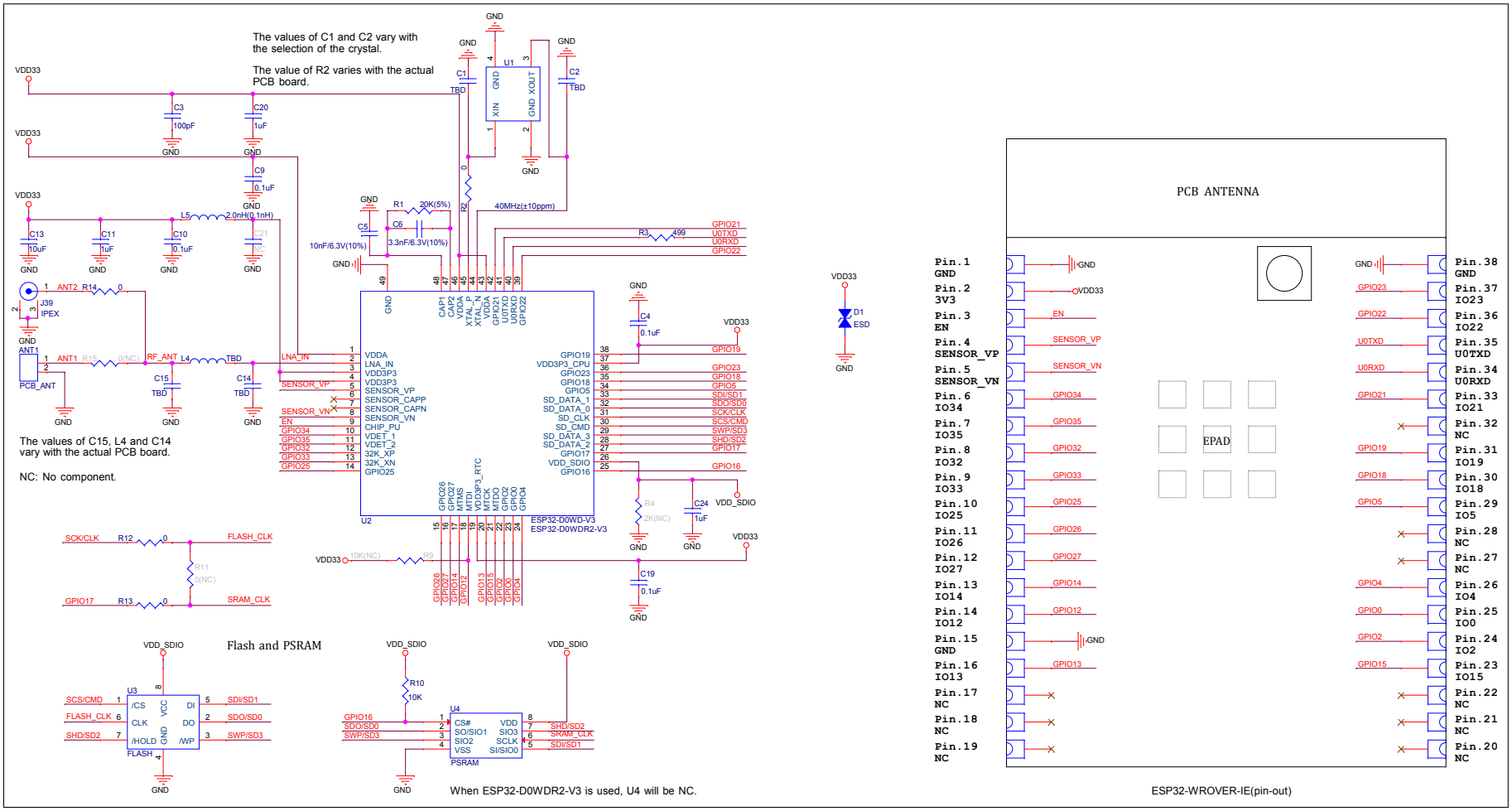



Figure 8: Schematics of ESP32-WROVER-IE

# 8 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

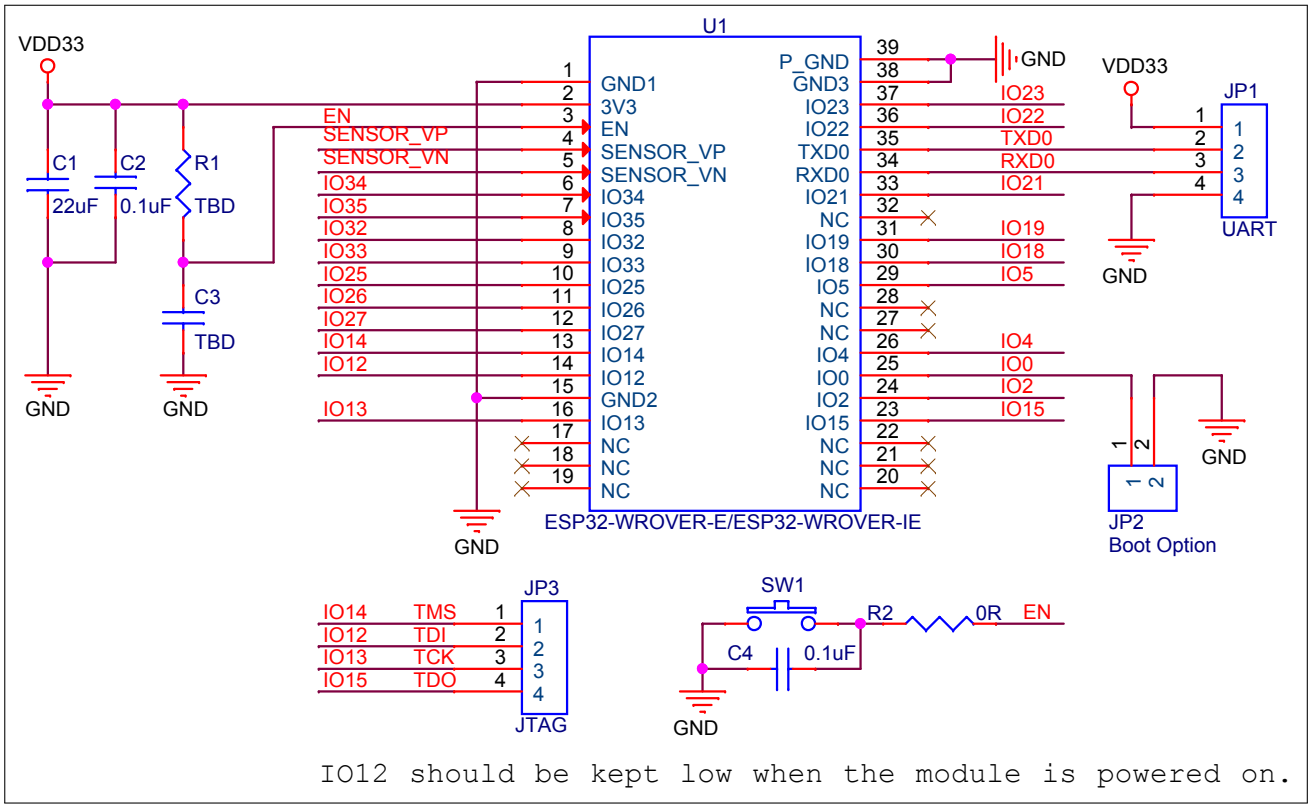



**Figure 9: Peripheral Schematics**

**Note:**

- Soldering Pad 39 to the Ground of the base board is not necessary for a satisfactory thermal performance. If users do want to solder it, they need to ensure that the correct quantity of soldering paste is applied.
- To ensure the power supply to the ESP32 chip during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 $\mu$F. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in *ESP32 Datasheet*.

# 9 Physical Dimensions

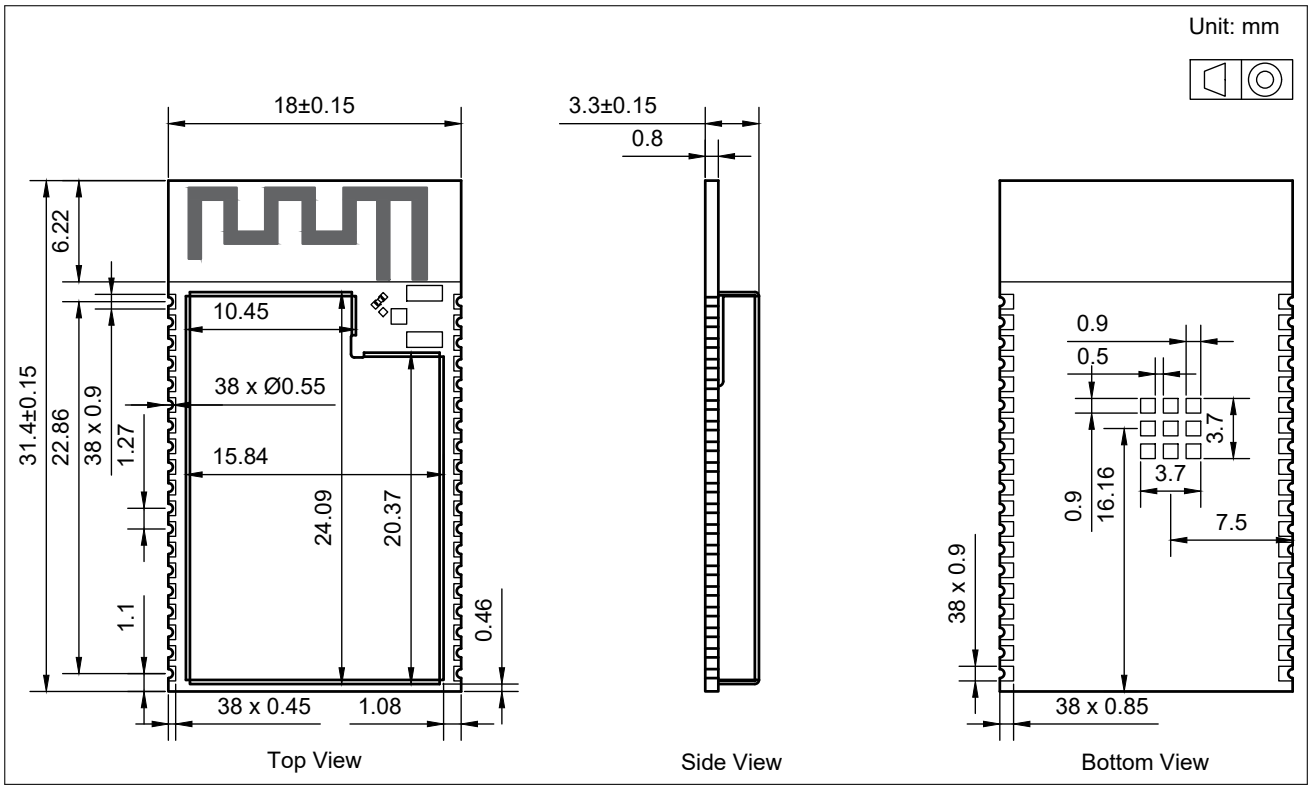



**Figure 10: ESP32-WROVER-E Dimensions**

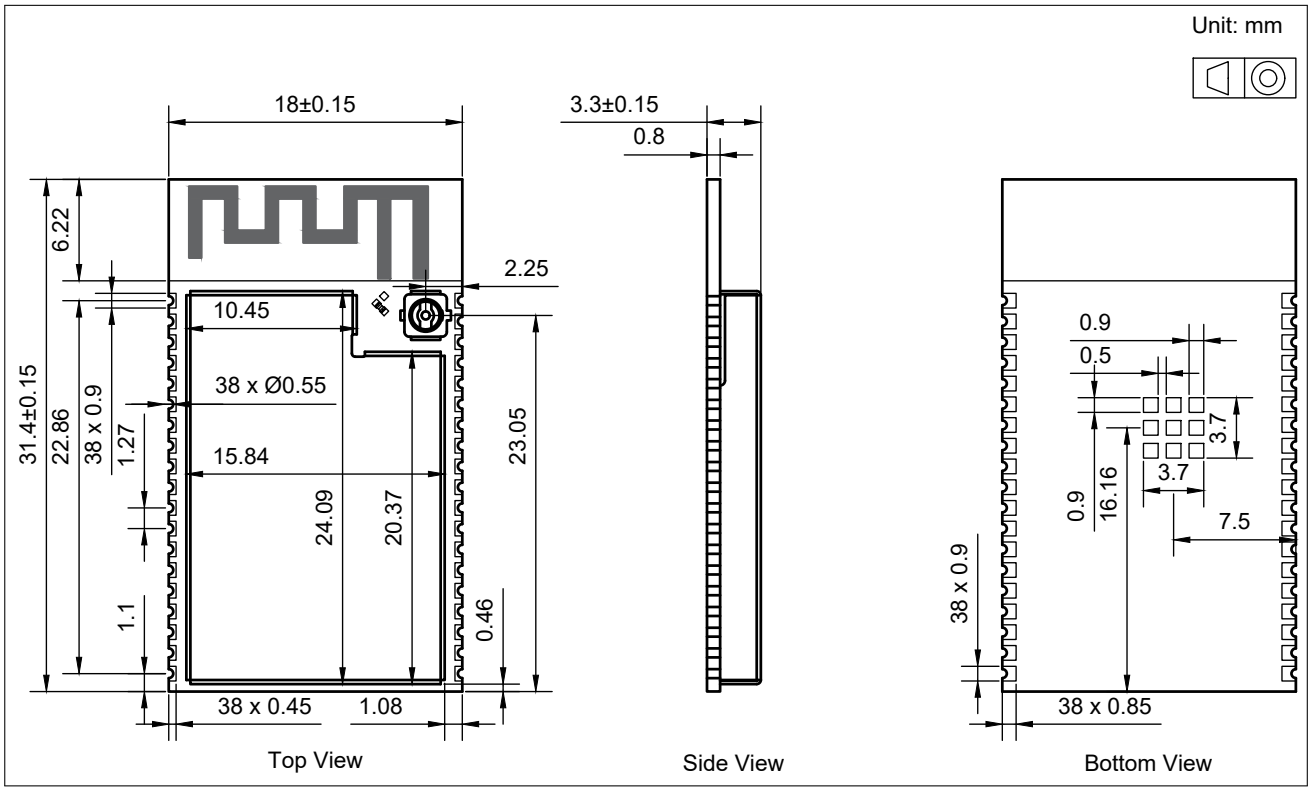



**Figure 11: ESP32-WROVER-IE Dimensions**

# 10 Recommended PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 12 *Recommended PCB Land Pattern*.
- Source files of recommended PCB land patterns to measure dimensions not covered in Figure 12. You can view the source files for ESP32-WROVER-E and ESP32-WROVER-IE with Autodesk Viewer.
- 3D models of ESP32-WROVER-E and ESP32-WROVER-IE. Please make sure that you download the 3D model file in .STEP format (beware that some browsers might add .txt).

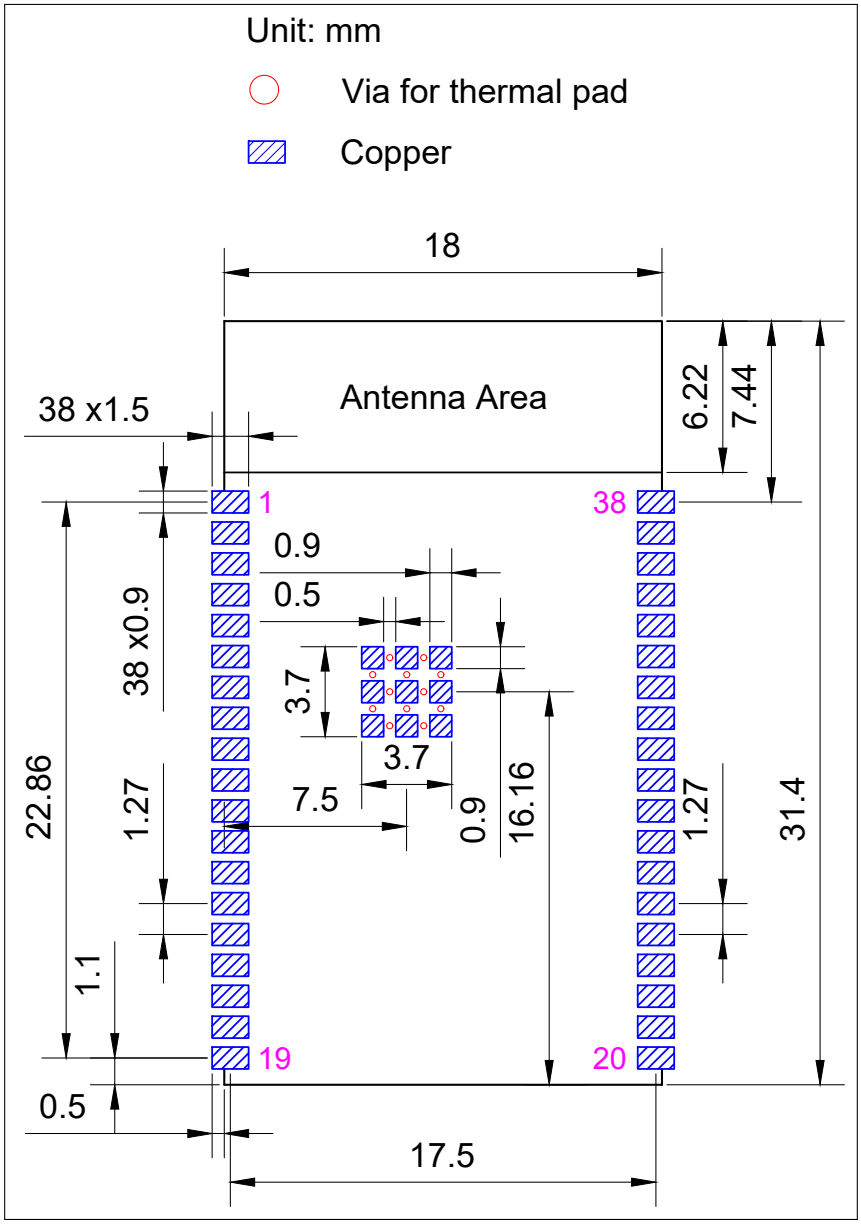



**Figure 12: Recommended PCB Land Pattern**

# 11 Dimensions of External Antenna Connector

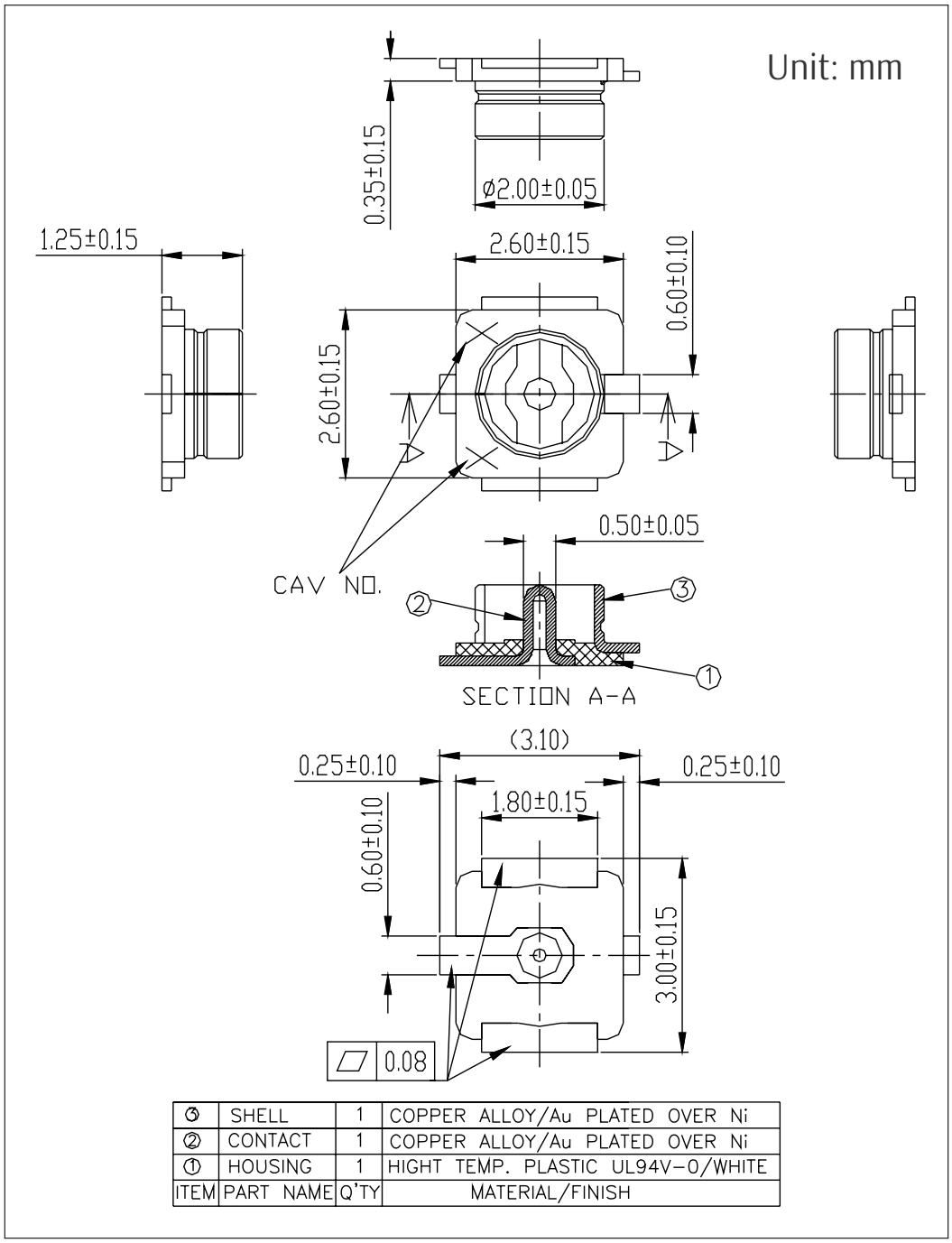



**Figure 13: Dimensions of External Antenna Connector**

# 12 Product Handling

## 12.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

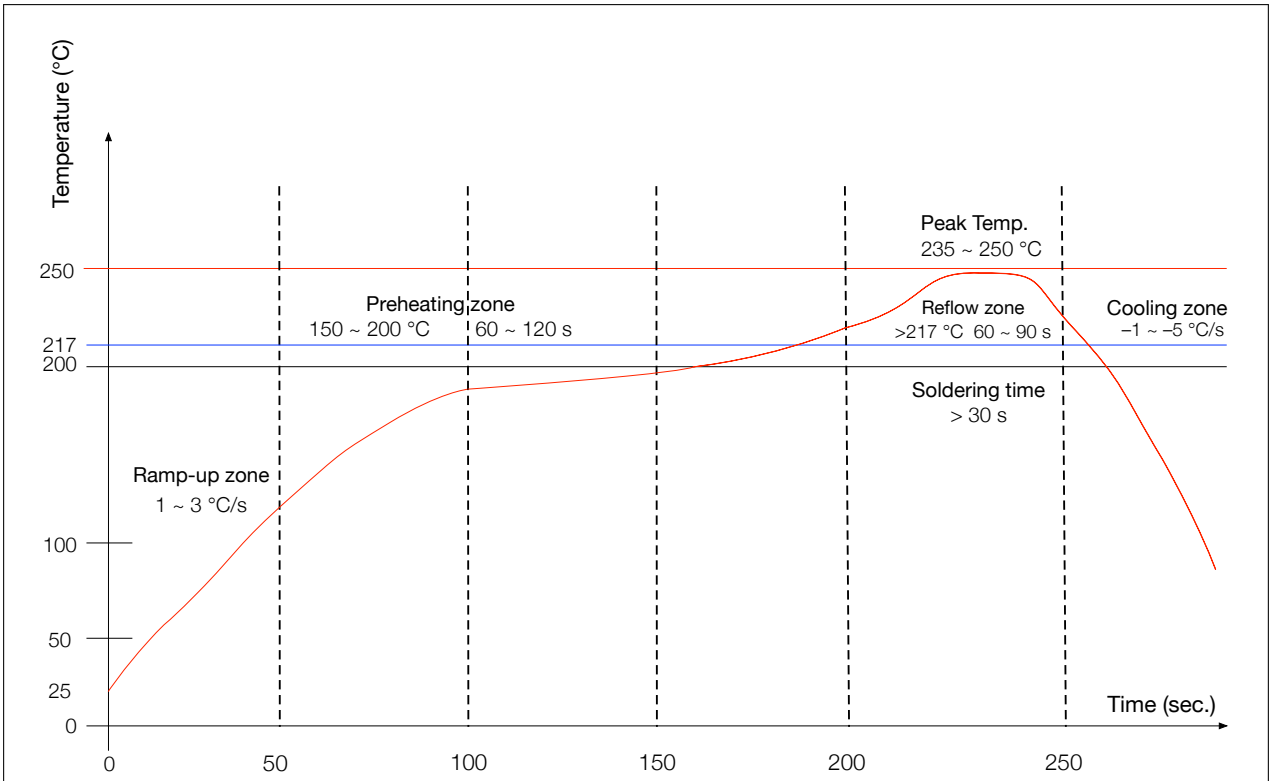
After unpacking, the module must be soldered within 168 hours with the factory conditions 25 ± 5 °C and 60 %RH. If the above conditions are not met, the module needs to be baked.

## 12.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

## 12.3 Reflow Profile

Solder the module in a single reflow.




**Ramp-up zone** — Temp.: 25 ~ 150 °C Time: 60 ~ 90 s Ramp-up rate: 1 ~ 3 °C/s
**Preheating zone** — Temp.: 150 ~ 200 °C Time: 60 ~ 120 s
**Reflow zone** — Temp.: >217 °C Time: 60 ~ 90 s; Peak Temp.: 235 ~ 250 °C Time: 30 ~ 70 s
**Cooling zone** — Peak Temp. ~ 180 °C Ramp-down rate: –1 ~ –5 °C/s
**Solder** — Sn-Ag-Cu (SAC305) lead-free solder alloy

**Figure 14: Reflow Profile**

## 12.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

# 13 Related Documentation and Resources

## Related Documentation

- ESP32 Series Datasheet – Specifications of the ESP32 hardware.
- ESP32 Technical Reference Manual – Detailed information on how to use the ESP32 memory and peripherals.
- ESP32 Hardware Design Guidelines – Guidelines on how to integrate the ESP32 into your hardware product.
- ESP32 ECO and Workarounds for Bugs – Correction of ESP32 design errors.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns
- *ESP32 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

## Developer Zone

- ESP-IDF Programming Guide for ESP32 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

## Products

- *ESP32 Series SoCs* – Browse through all ESP32 SoCs.
  https://espressif.com/en/products/socs?id=ESP32
- *ESP32 Series Modules* – Browse through all ESP32-based modules.
  https://espressif.com/en/products/modules?id=ESP32
- *ESP32 Series DevKits* – Browse through all ESP32-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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  https://espressif.com/en/contact-us/sales-questions

# Revision History

| Date | Version | Release notes |
|---|---|---|
| 2023-02-09 | v1.8 | Major updates:<br>• Removed contents about hall sensor according to PCN20221202<br>Other updates:<br>• Added source files of PCB land patterns and 3D models of the modules (if available) in Section 10: *Recommended PCB Land Pattern* |
| 2022-12-02 | v1.7 | Updated Figure *Physical Dimensions* and *Recommended PCB Land Pattern* |
| 2022-07-20 | v1.6 | Added module variants embedded with ESP32-D0WDR2-V3 chip<br>Added Table 1: *ESP32-WROVER-E Series Comparison* and Table 2: *ESP32-WROVER-IE Series Comparison*<br>Added Figure 6 and Table 6 in Section 3.3: *Strapping Pins*<br>Updated Section 13: *Related Documentation and Resources* |
| 2022-02-22 | v1.5 | Replaced Espressif Product Ordering Information with ESP Product Selector<br>Updated the description of TWAI in Table 3<br>Added a link to RF certificates in Table 3<br>Updated Ordering Information Table<br>Updated Table 7<br>Fixed typos |
| 2021-02-09 | V1.4 | Updated Figure 9: *Physical Dimensions*<br>Updated Figure 12: *Recommended PCB Land Pattern* |
| 2021-02-02 | V1.3 | Updated the trade mark from TWAI™ to TWAI®<br>Modified the note below Figure 14: *Reflow Profile*<br>Deleted Reset Circuit and Discharge Circuit for VDD33 Rail in Section 8: *Peripheral Schematics* |
| 2020-11-02 | V1.2 | Updated Figure 3.1: *Pin Layout*<br>Added a note to EPAD in Section 10: *Recommended PCB Land Pattern*<br>Updated the note to RC delay circuit in Section 8: *Peripheral Schematics* |
| 2020-06-11 | V1.1 | Updated the following figures:<br>• Figure 1: *ESP32-WROVER-E Block Diagram (with ESP32-D0WD-V3 embedded)*<br>• Figure 2: *ESP32-WROVER-E Block Diagram (with ESP32-D0WDR2-V3 embedded)* |
| 2020-05-22 | V1.0 | Official release |

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