Si5347-46
Data Sheet Errata for Product Revision B

This document contains information on the errata of product revision B of Si5347/46.

The device data sheet explains how to identify chip revision, either from package marking or electronically.

Errata effective date: 15 June 2015. Applies to the Si5347/46 Data Sheet revision 0.95.

Note: This document applies to Ordering Part Numbers (OPNs) which refer to product revision **B** (silicon revision A2). For example: Si5347A-**B**-GM or Si5346A-**B**xxxxx-GM, where xxxxx is the custom OPN ID, and B refers to the product revision.

ERRATA DEFINITIONS

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround(s) exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet and/or ClockBuilder Pro may be changed to match or address the device behavior.

Table .1. Errata Status Summary

Erratum	Title/Problem	Impact	Workarounds	Resolution
1	Impedance in LVCMOS high-Z mode is too low	Information	Yes	Si5347/46 Data Sheet and CBPro have been updated. Will also be fixed in the next silicon revision.
2	When entering holdover mode without valid holdover history data, holdover frequency may not be accurate	Information	Yes	Si5347/46 Data Sheet and CBPro have been updated.
3	VCO drifts to unknown frequency when holdover is disabled and there are no valid input clocks	Information	Yes	Si5347/46 Data Sheet and CBPro have been updated.
4	Inadvertent assertion of LOL during clock switching	Information	Yes	Si5347/46 Data Sheet and CBPro have been updated.
5	Possible output frequency transients when switching between clocks of the same nominal frequency	Information	Yes	A ramp switching feature will be available in the next silicon revision.
6	Exit from holdover ramp feature is not functional	Minor	Yes	Will be fixed in the next silicon revision.
8	No individual LOS or OOF sticky status bit may be cleared when any other LOS or OOF alarm is asserted	Minor	Yes	Will be fixed in the next silicon revision.
8	Possible part-per-trillion (ppt) frequency error	Minor	Yes	Will be fixed in the next silicon revision. CBPro v2.0 now addresses this issue.
9	SMBus timeout	Major	No	Will be fixed in the next silicon revision.

1. LVCMOS High-Impedance Mode is Too Low

Description

LVCMOS high-impedance is too low.

Impact without Workarounds

In earlier versions of ClockBuilder Pro (e.g., prior to v1.0), LVCMOS and differential output formats could be user-configured to disable in a low logic state, a high logic state, or in a stop mid (high-impedance or Hi-Z) state. The LVCMOS high-impedance mode should not be used.

Woraround

Select the disable state as stop-high or stop-low.

Resolution

This erratum will be fixed in the next silicon revision. ClockBuilder Pro (prior to v1.0) no longer allowed users to select the Hi-Z disable state. The Si5347/46 Data Sheet, beginning with v0.95, also removes support for Hi-Z mode.

2. Holdover Frequency May Not Be Accurate in Holdover Mode

Description

When entering holdover mode without valid holdover history data, holdover frequency may not be accurate. After exiting holdover, the device will operate normally.

Impact

When the holdover history is not valid (i.e., incomplete due to the holdover history window not completely occupied), the output frequency while in holdover may not be frozen at the last output frequency value before entry into holdover.

Workaround

Avoid entry into holdover until the holdover history window is valid.

Resolution

This erratum will be fixed in the next silicon revision (the device will enter holdover at the last output frequency value, even if there is not valid holdover history data).

3. VCO Drifts to Unknown Frequency

Description

VCO drifts to unknown frequency when holdover is disabled and there are no valid input clocks.

Impacts

VCO drifts to unknown frequency causing output clocks to operate at indeterminate frequencies.

Workaround

Ensure the HOLD_EN_PLLA, HOLD_EN_PLLB, HOLD_EN_PLLC and HOLD_EN_PLLD bits are always set. Holdover has been enabled automatically since CBPro v1.0.

Resolution

This erratum has been addressed with ClockBuilder Pro, beginning with v1.0.

4. Inadvertent Assertion of LOL During Clock Switching

Description

Inadvertent assertion of LOL during clock switching between two clocks that are the same exact frequency.

Impacts

If LOL is asserted, the device may enter fastlock LBW mode, causing undesirable frequency transients.

Workaround

Relaxing the LOL set and clear thresholds will eliminate this issue. ClockBuilder Pro, beginning with version v1.1, implements these settings as the defaults.

Resolution

This erratum was addressed, beginning with ClockBuilder Pro v1.1. Users are strongly encouraged to always use the latest ClockBuilder Pro revision.

5. Possible Output Frequency Transients

Description

Possible output frequency transients when switching between clocks that are not the same exact frequency.

Impact

The device's output clocks may overshoot (frequency) temporarily.

Workaround

In general, hitless switching can be used to minimize the frequency overshoot. Since this behavior is highly frequency plan dependent, contact Silicon Labs if you need additional support.

Resolution

This behavior will be addressed in the next silicon revision. The future silicon revision includes an option to enable ramp switching, if the application can accommodate the additional time required to measure the target frequency.

6. Exit From Holdover Ramp Feature Not Functional

Description

The exit from holdover ramp feature is not functional.

Impact

Using the ramp feature to lock to a new input frequency while exiting from holdover does not function. The user cannot select holdover modes that exit using a frequency ramp. Instead, the exit from holdover frequency rate of change needs to be governed by the loop bandwidth.

Workaround

When exiting from holdover, use a loop bandwidth-determined exit from holdover. For example, loop bandwidth-controlled exit from holdover can be configured to meet the requirements of Stratum 3 and many other standards. To do this, ensure HOLD_RAMP_BYP_PLLA, HOLD_RAMP_BYP_PLLB, HOLD_RAMP_BYP_PLLC, and HOLD_RAMP_BYP_PLLD are set high at locations 0x042C[3], 0x052C[3], and 0x062D[3). These registers have been set correctly since CBPro v1.0 was released.

Resolution

This erratum will be fixed in the next silicon revision.

7. LOS or OOF Sticky Status Bits May Not Be Cleared

Description

No individual LOS or OOF sticky status bit may be cleared when any other LOS or OOF alarm is asserted.

Impact

When two or more LOS or OOF sticky status bits are asserted, clearing either one or both requires disabling all the LOS or OOF fault monitors. LOS and OOF sticky (flag) bits will always remain set whenever asserted. Clearing the sticky bit(s) will have no effect.

Workaround

It is possible to clear a sticky bit by temporarily disabling all LOS and OOF fault monitors. Once disabled, the bit can be cleared and the fault monitor re-enabled.

Resolution

This erratum will be fixed in the next silicon revision.

8. Possible Part-per-Trillion Frequency Offset

Description

Based on a device's specific frequency plan and configuration, a minor frequency error may be generated in some output clock frequency configurations. Refer to **Si534x Applications Notification: Parts-per-Trillion Frequency Error** for detailed information.

Impact

Affected frequency plans can result in output clocks' frequency offsets between 1 and 10,000 part-per-trillion (ppt).

If the FINC/FDEC feature of the device is used to adjust the output frequency, the M divider is likely to use a value that triggers this frequency offset issue. Since using FINC/FDEC causes the M values to change, there is no single frequency plan that will prevent this from happening. Generally, applications that use FINC/FDEC are adjusting the frequency to match an external clock and the offset caused by this error will be unnoticeable since the FINC/FDEC adjustments are orders of magnitude greater than the offset caused by the error.

Workaround

ClockBuilder Pro configuration software enhancements address this issue. Download version v2.0 or later. After opening an existing project file, ClockBuilder Pro will analyze the frequency plan for the frequency offset and re-calculate the entire frequency plan to use the latest ClockBuilder Pro algorithms, while minimizing or eliminating the residual frequency offset issue.

Resolution

This erratum will be fixed in the next silicon revision; in the meantime, ClockBuilder Pro or later can be used to address this issue.

9. SMBUS Timeout Register Setting (SMBUS_TIMEOUT) Does Not Assert

Description

The SMBus timeout register setting (SMBUS_TIMEOUT) does not assert when the device exceeds the 35 ms maximum value prescribed by the standard.

Impact

If SMBUS_TIMEOUT is mapped to affect the hardware interrupt pin (INTR#), the SDA bus will not be released as expected and required by the SMBus standard.

Workaround

None. Avoid reliance on the SMBus timeout feature.

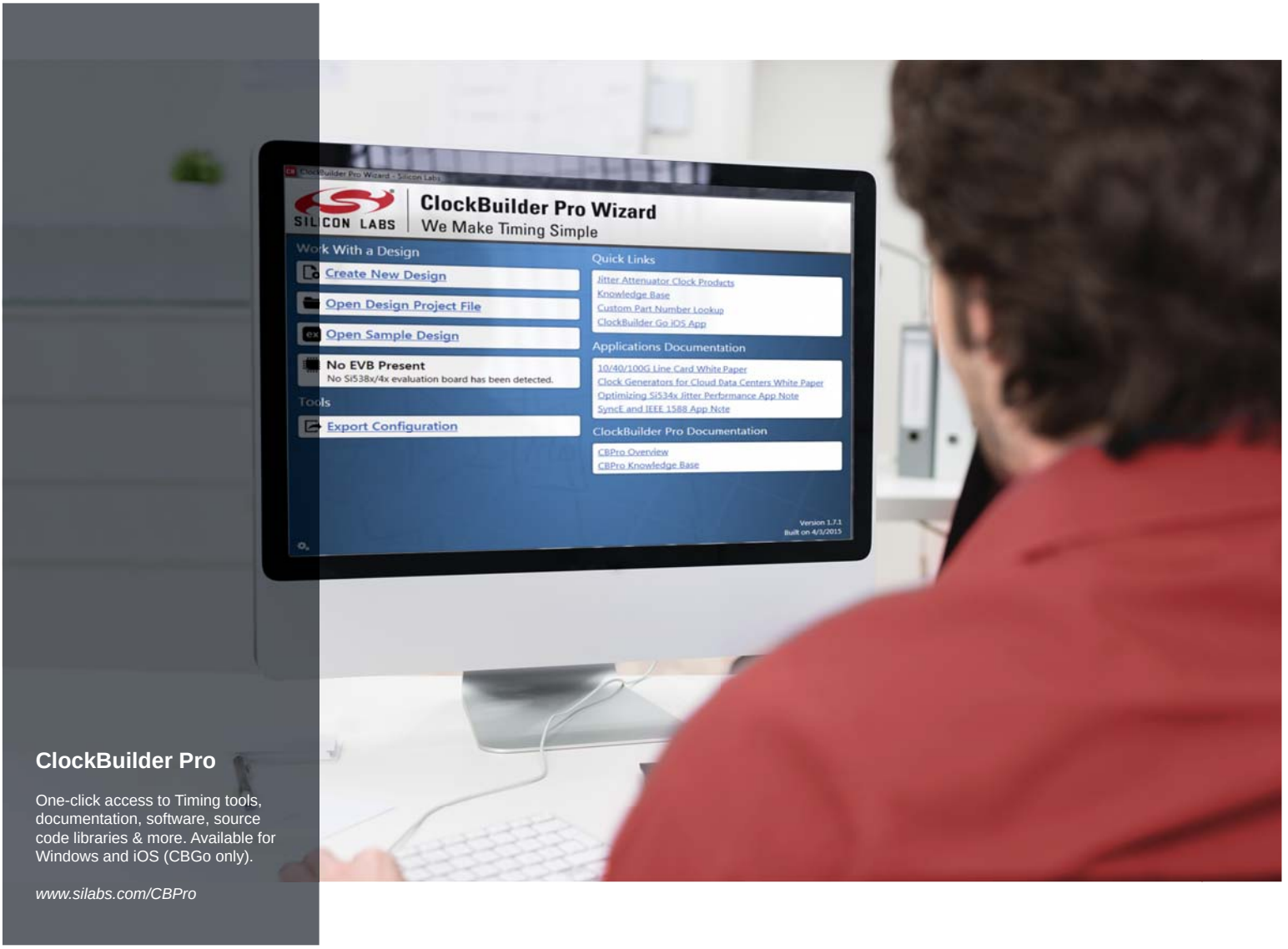
Resolution

This erratum will be fixed in the next silicon revision.

10. Document History

v2.0: June 2015

- Initial revision of this document for Si534/46 errata, documented separately from other Si534x family members.
- Derived from original Si534x Family Errata, v1.0 (12-August-2014).



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com