

N- and P-Channel 20V (D-S) Power MOSFET

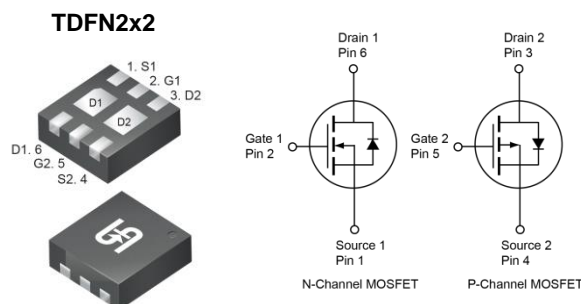
FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Low gate charge for fast power switching
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

APPLICATIONS

- Load Switch
- Power Management
- Portable Devices

KEY PERFORMANCE PARAMETERS			
PARAMETER	TYPE	VALUE	UNIT
V_{DS}	N-ch	20	V
	P-ch	-20	
$R_{DS(on)}$ (max)	N-ch	$V_{GS} = 4.5V$	30
		$V_{GS} = 2.5V$	36
		$V_{GS} = 1.8V$	42
	P-ch	$V_{GS} = -4.5V$	55
		$V_{GS} = -2.5V$	78
		$V_{GS} = -1.8V$	90
Q_g	N-ch	7.3	nC
	P-ch	9.3	



Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)				
PARAMETER	SYMBOL	N-ch	P-ch	UNIT
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 10	± 10	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ C$	13	-9.5
		$T_A = 25^\circ C$	6.4	-5
Pulsed Drain Current	I_{DM}	52	-38	A
Total Power Dissipation	P_D	$T_C = 25^\circ C$	5	5
		$T_C = 125^\circ C$	1	1
Total Power Dissipation	P_D	$T_A = 25^\circ C$	1.89	1.89
		$T_A = 125^\circ C$	0.38	0.38
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150		$^\circ C$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	25	$^\circ C/W$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	66	

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)							
PARAMETER	CONDITIONS	SYMBOL	TYPE	MIN	TYP	MAX	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu\text{A}$	BV_{DSS}	N-ch	20	--	--	V
	$V_{GS} = 0V, I_D = -250\mu\text{A}$		P-ch	-20	--	--	
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	N-ch	0.4	0.6	0.8	V
	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$		P-ch	-0.4	-0.6	-0.8	
Gate-Source Leakage Current	$V_{GS} = \pm 10V, V_{DS} = 0V$	I_{GSS}	N-ch	--	--	± 100	nA
	$V_{GS} = \pm 10V, V_{DS} = 0V$		P-ch	--	--	± 100	
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$	I_{DSS}	N-ch	--	--	1	μA
	$V_{GS} = 0V, V_{DS} = 20V$ $T_J = 125^\circ\text{C}$			--	--	100	
	$V_{GS} = 0V, V_{DS} = -20V$		P-ch	--	--	-1	
	$V_{GS} = 0V, V_{DS} = -20V$ $T_J = 125^\circ\text{C}$			--	--	-100	
Drain-Source On-State Resistance ^(Note 2)	$V_{GS} = 4.5V, I_D = 6.4A$	$R_{DS(on)}$	N-ch	--	17	30	m Ω
	$V_{GS} = 2.5V, I_D = 5.8A$			--	22	36	
	$V_{GS} = 1.8V, I_D = 3.9A$			--	32	42	
	$V_{GS} = -4.5V, I_D = -5A$		P-ch	--	48	55	
	$V_{GS} = -2.5V, I_D = -4.2A$			--	60	78	
	$V_{GS} = -1.8V, I_D = -3.9A$			--	78	90	
Forward Transconductance ^(Note 2)	$V_{DS} = 5V, I_D = 6.4A$	g_{fs}	N-ch	--	28	--	S
	$V_{DS} = -5V, I_D = -5A$		P-ch	--	15	--	
Dynamic ^(Note 3)							
Total Gate Charge	N-ch $V_{GS} = 4.5V,$ $V_{DS} = 10V, I_D = 6.4A$	Q_g	N-ch	--	7.3	--	nC
			P-ch	--	9.3	--	
Gate-Source Charge	P-ch	Q_{gs}	N-ch	--	0.9	--	
			P-ch	--	1.7	--	
Gate-Drain Charge	$V_{GS} = -4.5V,$ $V_{DS} = -10V, I_D = -5A$	Q_{gd}	N-ch	--	2	--	
			P-ch	--	1.9	--	
Input Capacitance	N-ch $V_{GS} = 0V, V_{DS} = 10V$	C_{iss}	N-ch	--	536	--	pF
			P-ch	--	903	--	
Output Capacitance	f = 1.0MHz P-ch	C_{oss}	N-ch	--	82	--	
			P-ch	--	104	--	
Reverse Transfer Capacitance	$V_{GS} = 0V, V_{DS} = -10V$ f = 1.0MHz	C_{rss}	N-ch	--	54	--	
			P-ch	--	64	--	
Gate Resistance	f = 1.0MHz	R_g	N-ch	--	0.6	--	Ω
			P-ch	--	14.8	--	

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)							
PARAMETER	CONDITIONS	SYMBOL	TYPE	MIN	TYP	MAX	UNIT
Switching ^(Note 3)							
Turn-On Delay Time	N-ch	$t_{d(on)}$	N-ch	--	8.9	--	ns
			P-ch	--	11.4	--	
Turn-On Rise Time	$V_{GS} = 4.5\text{V}, R_G = 2\Omega$ $V_{DS} = 10\text{V}, I_D = 6.4\text{A}$	t_r	N-ch	--	75.6	--	
			P-ch	--	73.1	--	
Turn-Off Delay Time	P-ch	$t_{d(off)}$	N-ch	--	24.5	--	
			P-ch	--	39.5	--	
Turn-Off Fall Time	$V_{DS} = -10\text{V}, I_D = -5\text{A}$	t_f	N-ch	--	98.1	--	
			P-ch	--	91	--	
Source-Drain Diode							
Forward Voltage ^(Note 2)	$V_{GS} = 0\text{V}, I_S = 6.4\text{A}$	V_{SD}	N-ch	--	--	1	V
	$V_{GS} = 0\text{V}, I_S = -5\text{A}$		P-ch	--	--	-1	
Reverse recovery Time	N-ch $I_S = 6.4\text{A},$ $dI/dt = 100\text{A}/\mu\text{s}$	t_{rr}	N-ch	--	11.4	--	nc
			P-ch	--	12.3	--	
Reverse Recovery Charge	P-ch $I_S = -5\text{A},$ $dI/dt = 100\text{A}/\mu\text{s}$	Q_{rr}	N-ch	--	4.3	--	nc
			P-ch	--	4.5	--	

Notes:

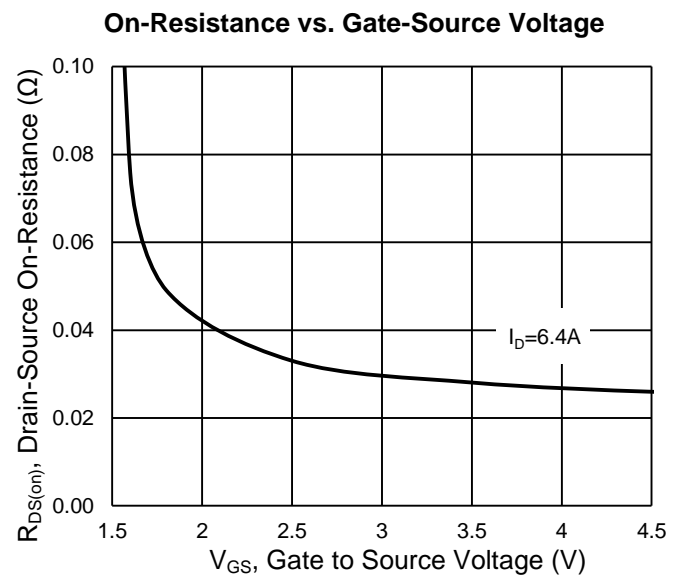
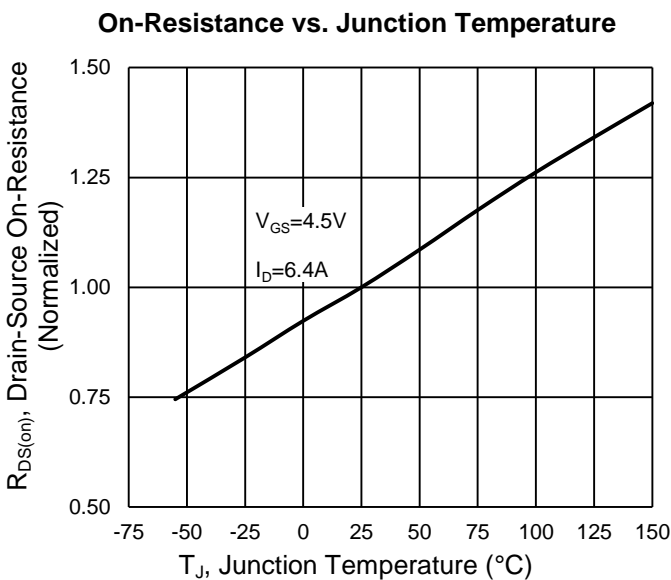
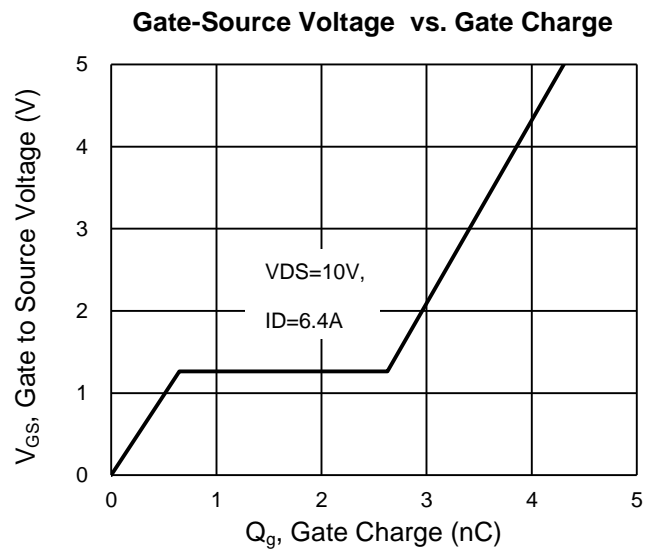
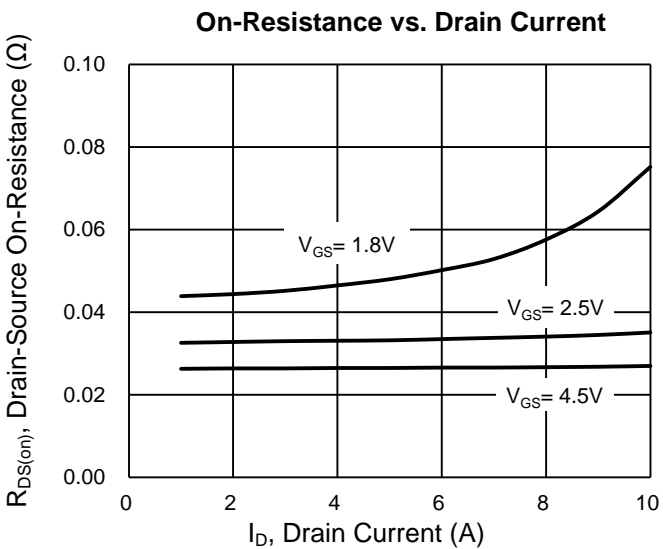
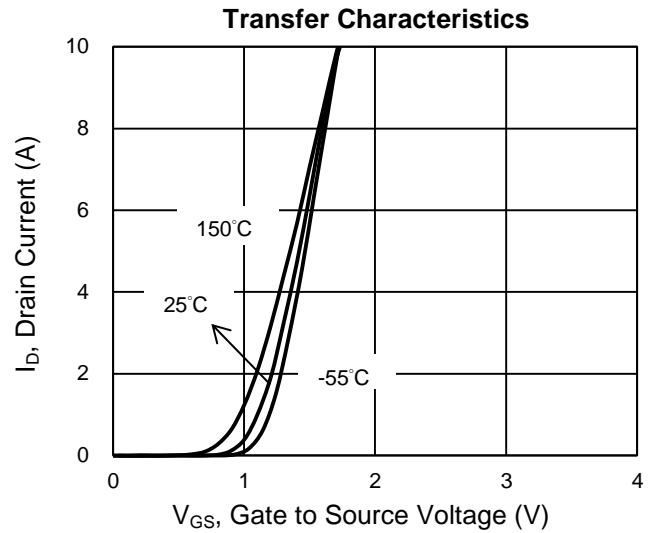
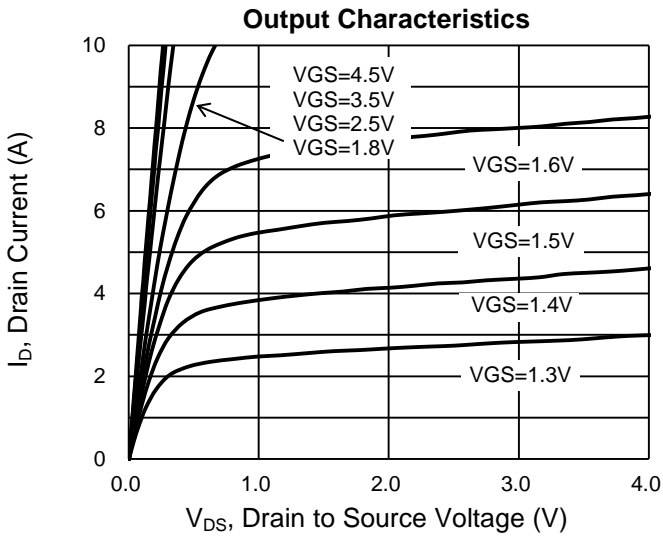
1. Silicon limited current only.
2. Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM2537CQ RFG	TDFN2x2	3,000pcs / 7" Reel

CHARACTERISTICS CURVES (N-Channel)

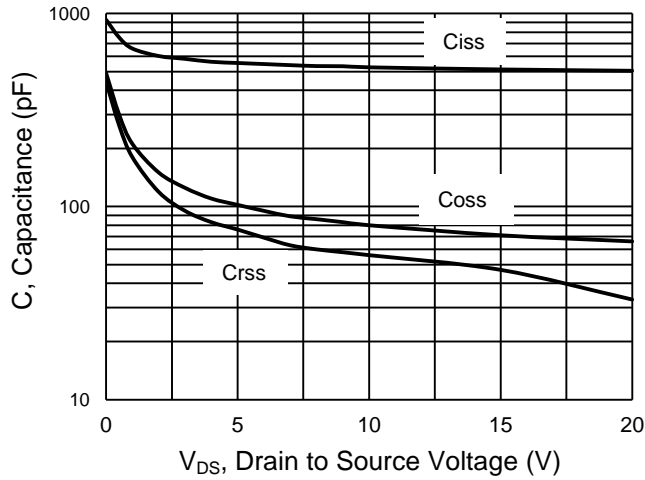
($T_A = 25^\circ\text{C}$ unless otherwise noted)



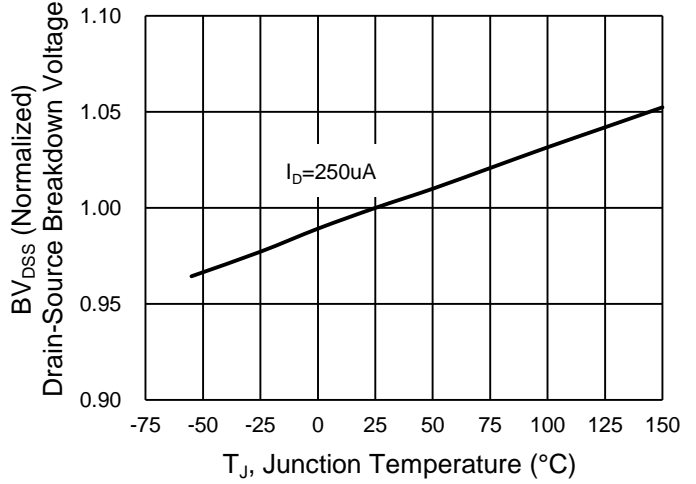
CHARACTERISTICS CURVES (N-Channel)

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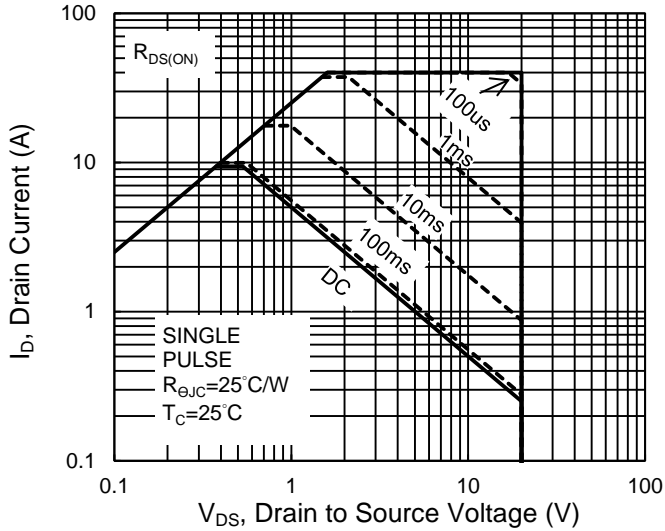
Capacitance vs. Drain-Source Voltage



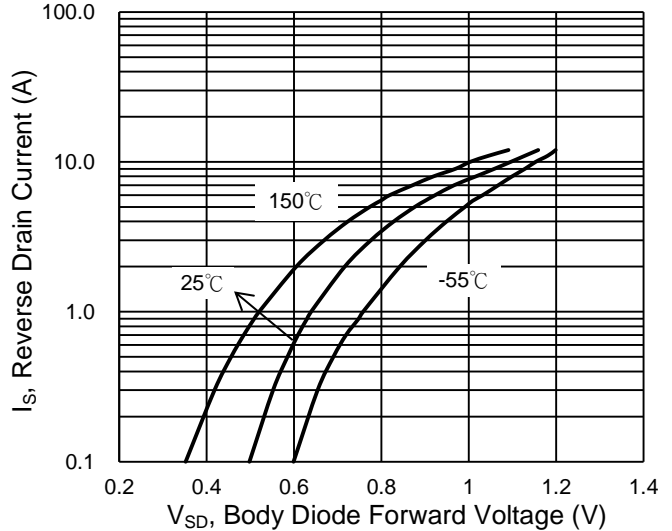
BV_{DSS} vs. Junction Temperature



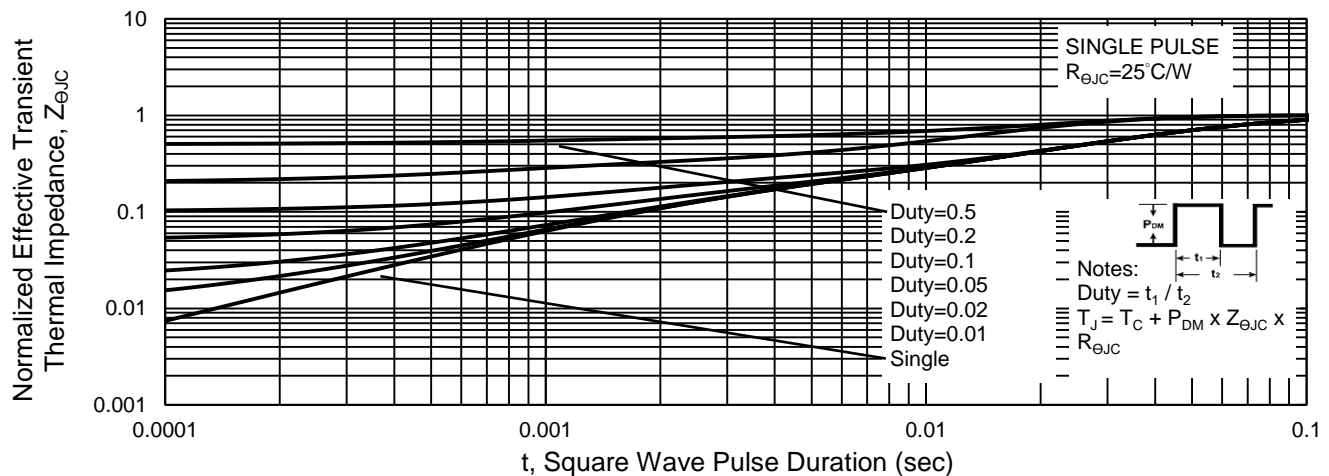
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

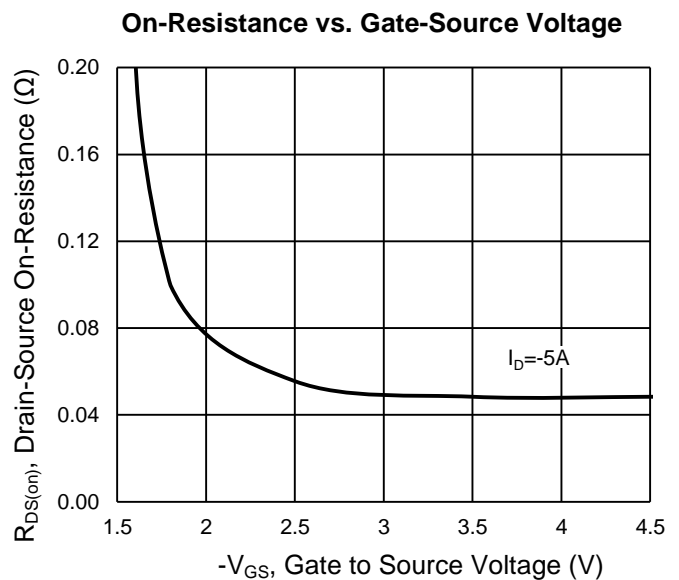
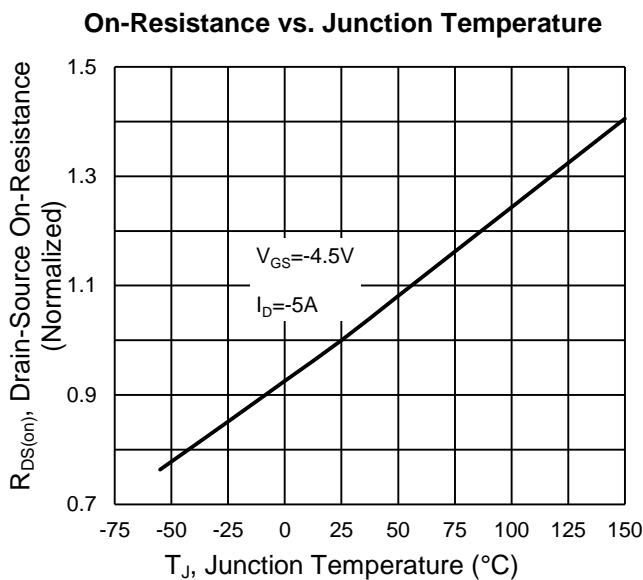
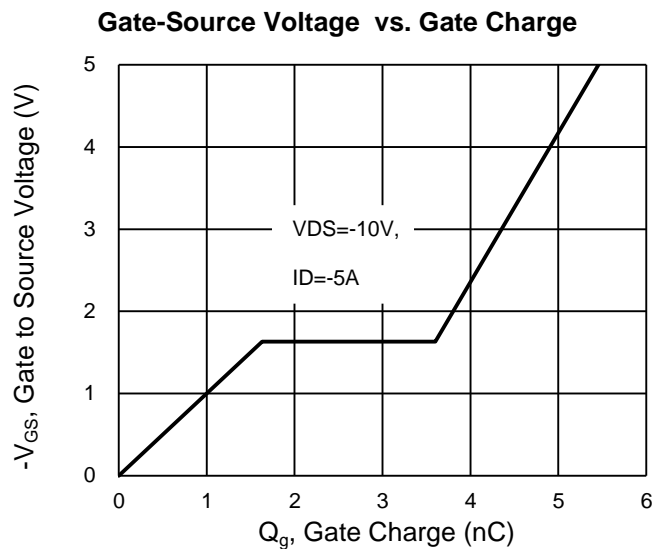
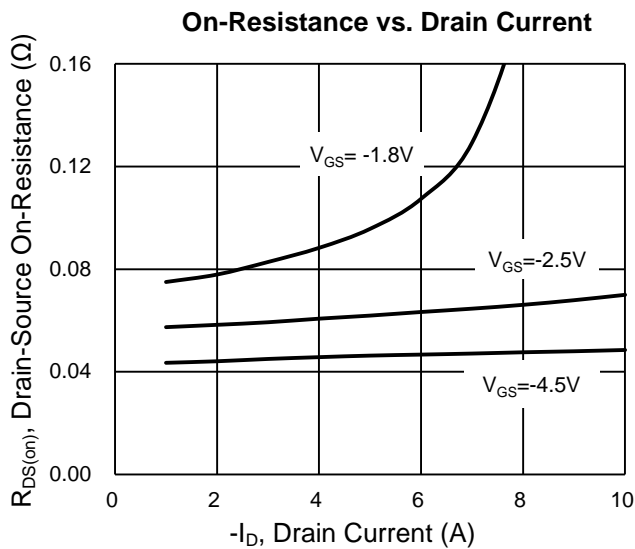
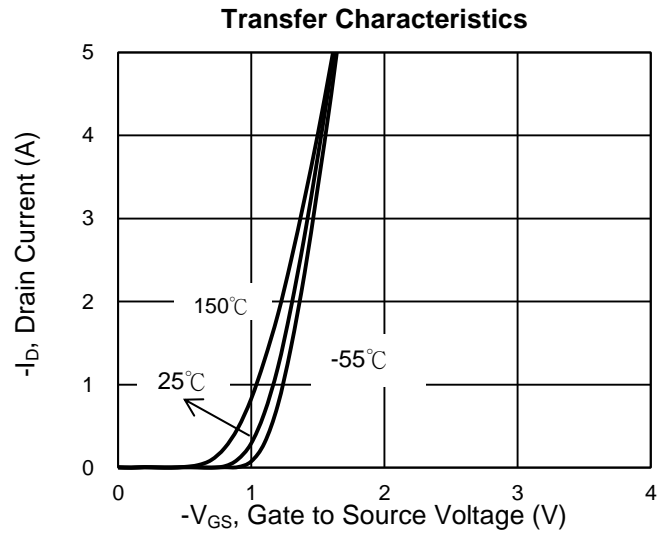
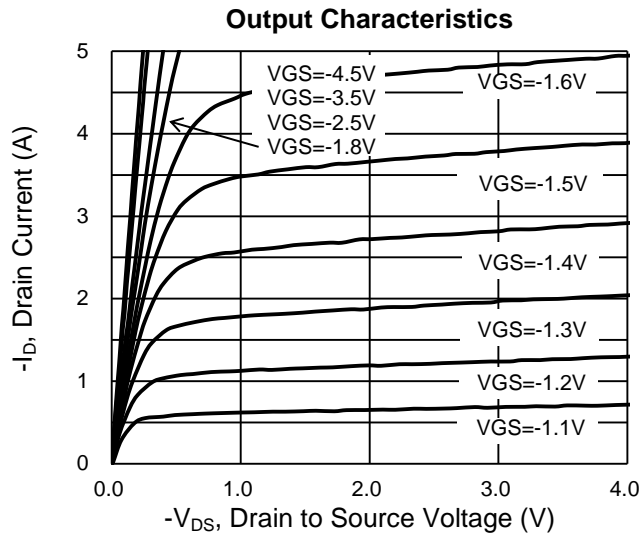


Normalized Thermal Transient Impedance, Junction-to-Case



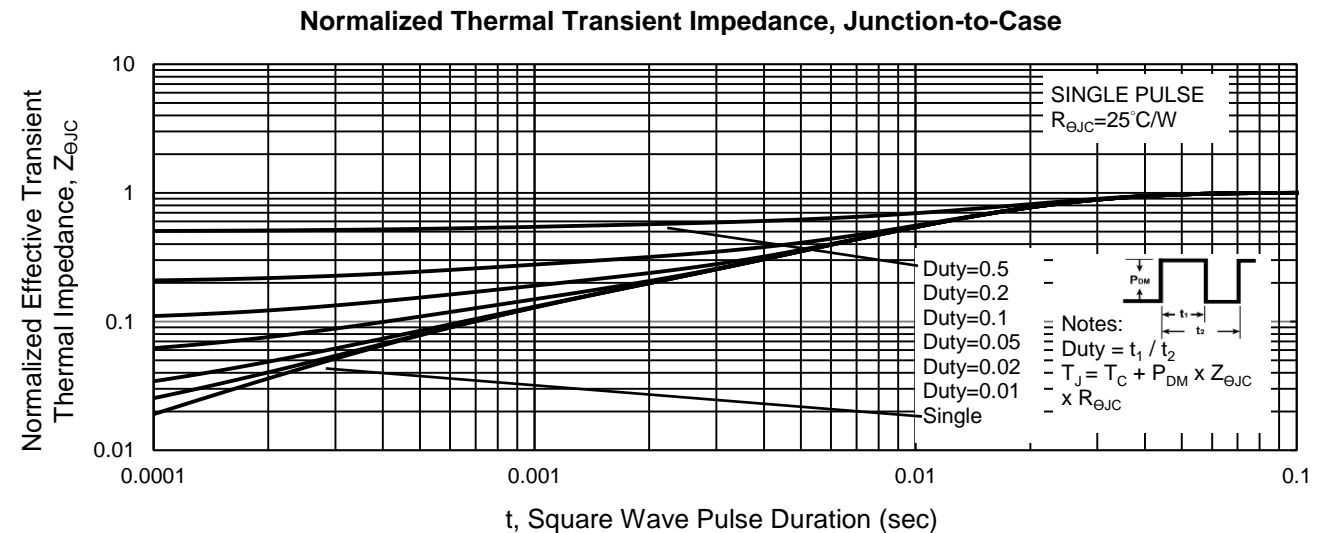
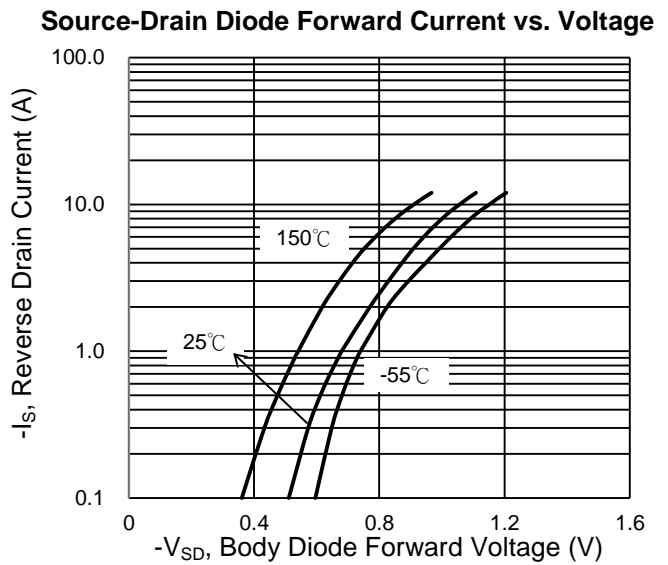
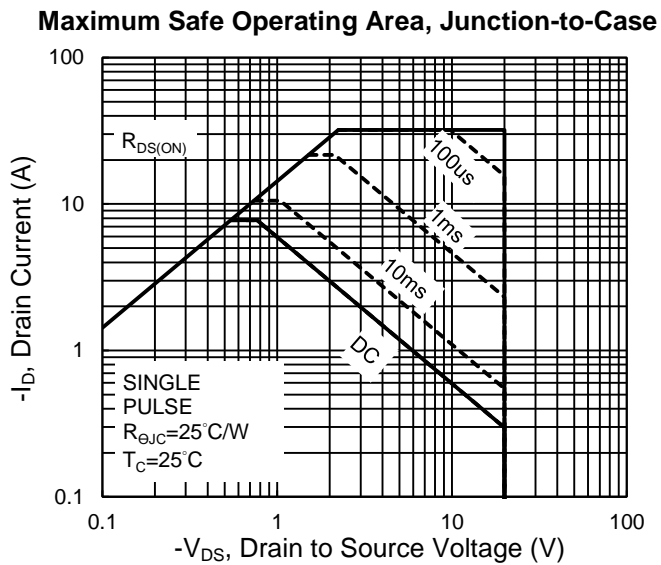
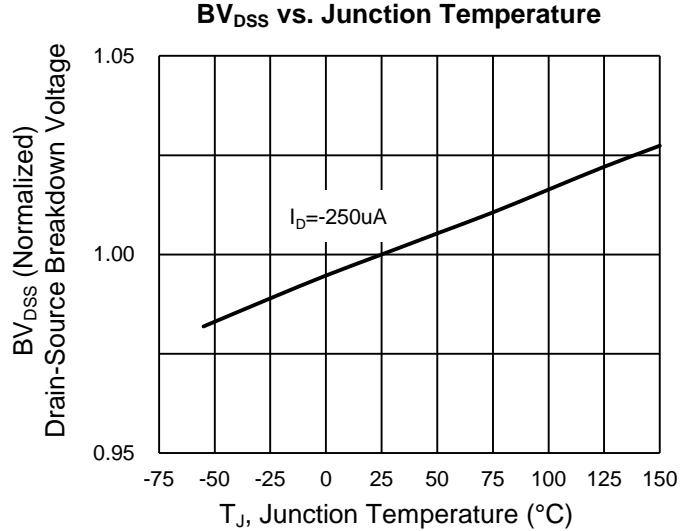
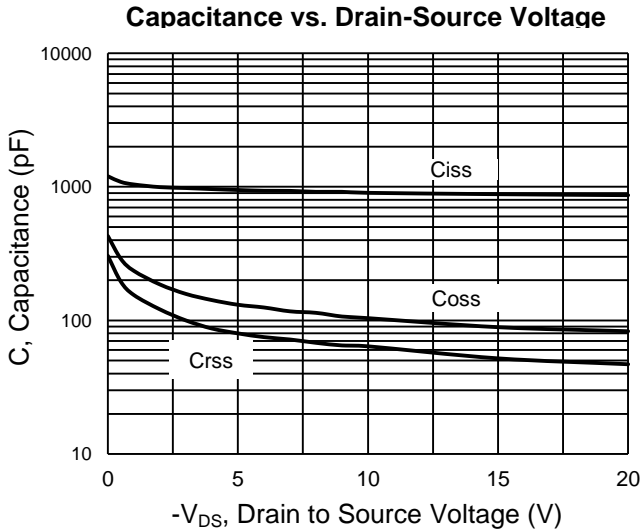
CHARACTERISTICS CURVES (P-Channel)

($T_A = 25^\circ\text{C}$ unless otherwise noted)



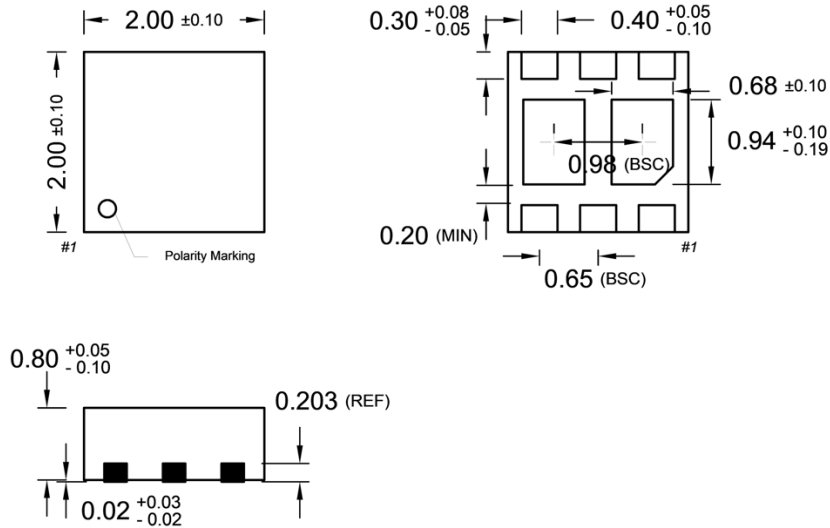
CHARACTERISTICS CURVES (P-Channel)

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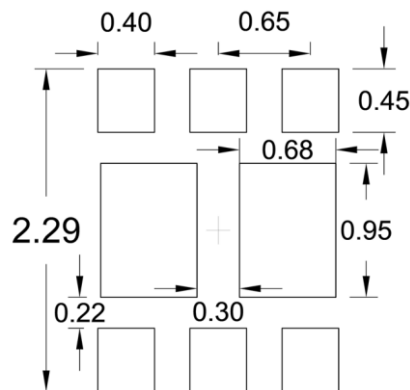


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

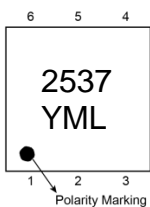
TDFN2x2



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- M** = Month Code for Halogen Free
 - O** =Jan **P** =Feb **Q** =Mar **R** =Apr
 - S** =May **T** =Jun **U** =Jul **V** =Aug
 - W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

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