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TFT | OLED | GRAPHIC | CHARACTER | UWVD | SEGMENT | CUSTOM

Character OLED Module

Part Number

O164A-CW-SS3

Overview:

- 16x4 Character OLED
- White Pixel Color
- Overall Size: 87mm x 60mm
- Parallel Interface
- -40C to 70C Operating Temperature
- 3.3V
- Controller: KS0066 or Equivalent
- RoHS Compliant

Character OLED Features:

Character Format: 5x7 Dots with Cursor

Display Format: 16 Characters x 4 Lines

Interface: Parallel

Controller: KS0066 or Equivalent

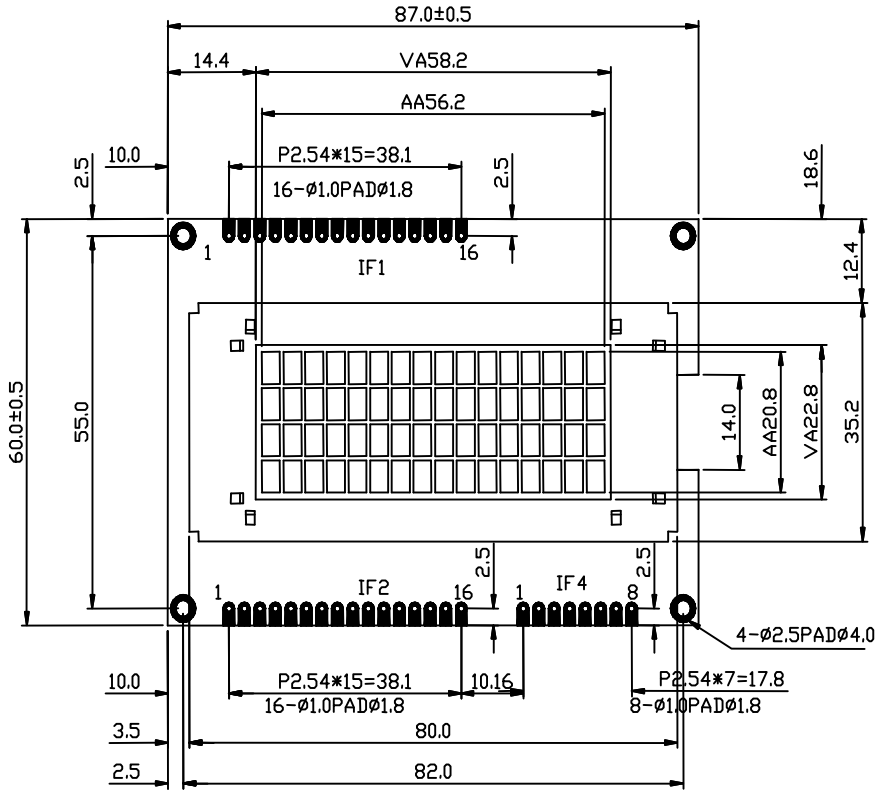
RoHS Compliant

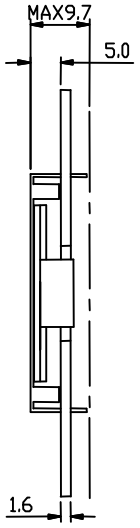
General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area	58.2x22.8	mm	-
Pixel Color	White	-	-
Viewing Direction	Free	-	-
Voltage	3.3	V	-
Number of Characters	16x4	-	-
Controller IC	KS0066 or Equivalent	-	-
Interface	Parallel	-	-
DC to DC Circuit	Built In	-	-
Operating temperature	-40～+70	℃	-
Storage temperature	-40～+85	℃	-

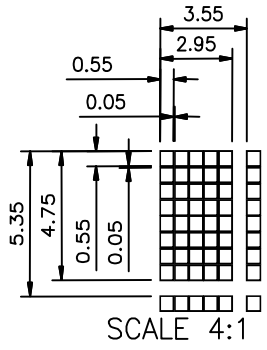
Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module size	X (Width)		87		mm	-
	Y (Height)		60		mm	-
	Z (Depth)			9.7	mm	-

1. Outline Dimensions







SCALE 4:1

PIN NO	SIGNAL
1	VSS
2	VDD
3	VR
4	RS
5	WR#
6	RD#
7	D0
8	D1
9	D2
10	D3
11	D4
12	D5
13	D6
14	D7
15	NC
16	NC

Notes:
1.) Display: OLED White
2.) OLED Type: Character
3.) OLED Color: White
4.) Temperature Range: Wide
5.) Display Format: 16 characters x 4 lines
6.) Interface: 8-bit parallel
7.) IC Controller: KS0066

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		PARTS NO.	O164A-CW-SS3
TOLERANCE UNLESS OTHERWISE SPECIFIED	X.X±0.3 X.XX±0.2	Drawn	Unit
		Checked	mm
Scale 1:1		Approve	Page 1 1

2. Input Terminal Pin Assignment

NO.	Symbol	Description
1	VSS	Power Supply Ground
2	VDD	Power Supply Voltage
3	NC	No Connector
4	RS	Register Select
5	R/W	Read/Write
6	E	Enable Signal
7	DB0	Data Bit 0
8	DB1	Data Bit 1
9	DB2	Data Bit 2
10	DB3	Data Bit 3
11	DB4	Data Bit 4
12	DB5	Data Bit 5
13	DB6	Data Bit 6
14	DB7	Data Bit 7

3. Optical Characteristics

Item		Symbol	Condition	Min	Typ.	Max	Unit
Viewing Angle		Φ1	Cr≥ 10000:1	--	75	--	deg
		Φ2		--	75	--	
		Φl		--	65	--	
		Φr		--	65	--	
Response Time	Rise	t_r		--	40	--	ms
	Fall	t_f		--	40	--	
Contrast Ratio		Cr		--	10000:1	--	--
Brightness		L		30	40	--	cd/m^2
Peak Emission Wavelength		CIE (White)		X=0.25 Y=0.27	X=0.29 Y=0.31	X=0.33 Y=0.35	nm

4. Electrical Characteristics

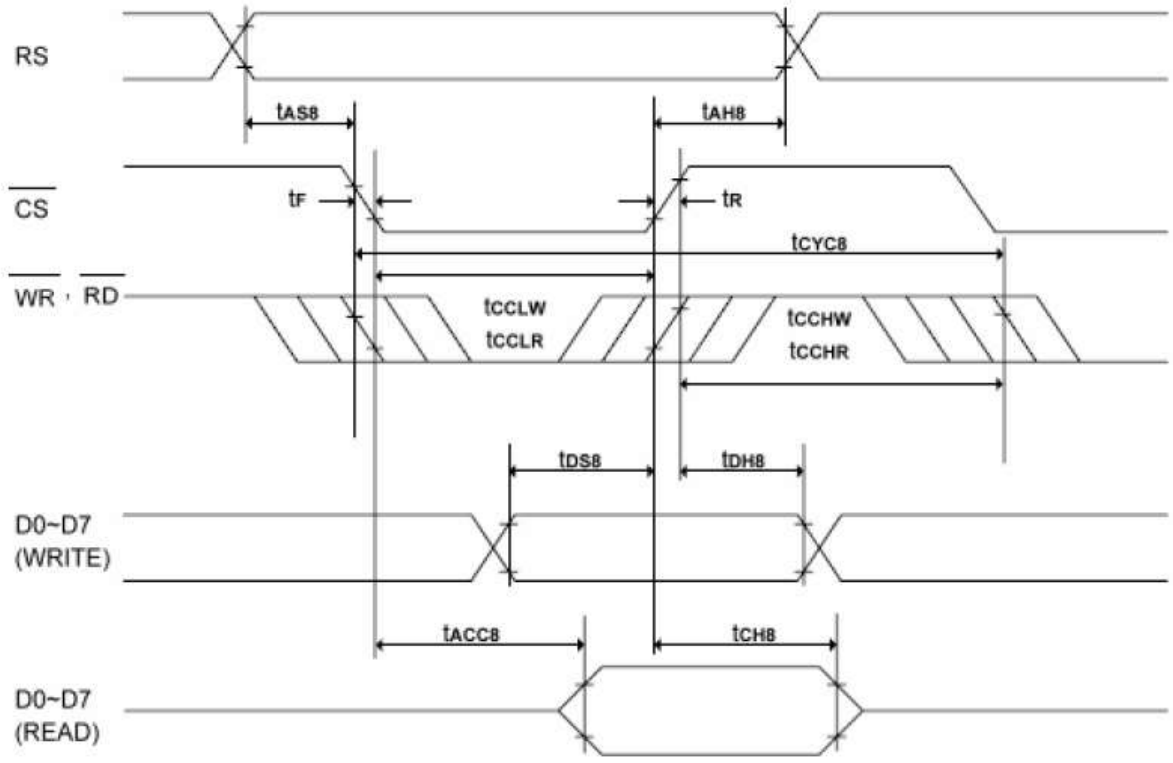
4.1 DC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Condition
Supply Voltage for Logic	V_{DD}-V_{SS}	2.7	3.3	3.5	V	
Power Supply for OLED	V_{cc}-V_{ss}	8.5	9.0	9.5	V	
Input Voltage	V_{IL}	0	--	$0.3V_{DD}$	V	L level
	V_{IH}	$0.7V_{DD}$	--	V_{DD}	V	H level
Output Voltage	V_{OL}	0	--	$0.3V_{DD}$	V	L level
	V_{OH}	$0.7V_{DD}$	--	V_{DD}	V	H level
Operating Current for V_{pp}	I_{pp}	--	39.2	54.5	mA	
Power Supply Current for OLED	I_{DD}	--	39.7	54.8	mA	V_{DD} = 3.3V V_{pp} = 9.0V

NOTE: If the maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the specified parameters.

5. Timing Characteristics

Parameter	Symbol	Min	Max	Unit
System cycle time	t_{CYC8}	500	--	ns
Address setup time	t_{AS8}	0	--	ns
Address hold time	t_{AH8}	0	--	ns
Data setup time	t_{DS8}	66	--	ns
Data hold time	t_{DH8}	25	--	ns
Output disable time (C_L = 100pF)	t_{CH8}	16	110	ns
$\overline{RD}$ access time (C_L = 100pF)	t_{ACC8}	--	230	ns
Control L pulse width (WR)	t_{CCLW}	166	--	ns
Control L pulse width (RD)	t_{CCLR}	200	--	ns
Control H pulse width (WR)	t_{CCHW}	166	--	ns
Control H pulse width (RD)	t_{CCHR}	166	--	ns
Rise time	t_R	--	25	ns
Fall time	t_F	--	25	ns



6. Instructions

To overcome the speed difference between the internal clock of ST7066 (or equivalent) and the MPU clock, ST7066 performs internal operations by storing control in formations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. Instructions can be divided largely into four groups:

1) ST7066 function set instructions (set display methods, set data length, etc.)
2)Address set instructions to internal RAM
3)Data transfer instructions with internal RAM
4)Others

The address of the internal RAM is automatically increased or decreased by 1.
Note: during internal operation, busy flag (DB7) is read "High". Busy flag check must be preceded by the next instruction.

6.1 Instruction Table

Instruction	Instruction Code										Description	Exc. Time (fosc = 270kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to original position if shifted. Contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and blinking of display	39us
Display On/Off	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit	-
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving, shift control bit and direction. Does not change DDRAM data	39us
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8/4-bit), Numbers of display Line (N: 2/1 line) and font type (F:5x11/5x8)	39us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	39us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	39us
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag and address. Can be done during internal operation by reading BF	0us
Write Data to Address	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	43us
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	43us

NOTE: When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2fosc is necessary for executing the next instruction by the falling edge of the "E" signal after the busy flag (DB7) goes to "Low".

6.2 Contents

6.2.1 Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display. Make the entry mode increment (I/D="High").

6.2.2 Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change

6.2.3 Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	I/D	SH

Set the moving direction of cursor and display.
I/D: increment / decrement of DDRAM address (cursor or blink)
When I/D="high", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D="Low", cursor/blink moves to left and DDRAM address is increased by 1.
CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.
SH: shift of entire display
When DDRAM read (CGRAM read/write) operation or SH="Low", shifting of entire display is not performed. If SH ="High" and DDRAM write operation, shift of entire display is performed according to I/D value. (I/D="high". shift left, I/D="Low". Shift right)

6.2.4 Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1-bit register.
D: Display ON/OFF control bit
When D="High", entire display is turned on.
When D="Low", display is turned off, but display data remains in DDRAM.
C: cursor ON/OFF control bit
When D="High", cursor is turned on.
When D="Low", cursor is disappeared in current display, but I/D register preserves its data.
B: Cursor blink ON/OFF control bit
When B="High", cursor blink is on, which performs alternately between all the "High" data and display characters at the cursor position.
When B="Low", blink is off.

6.2.5 Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line. Note that display shift is performed simultaneously in all the lines. When display data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not change

Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left. AC is decreased by 1
0	1	Shift cursor to the right. AC is increased by 1
1	0	Shift all the display to the left. Cursor moves according to the display
1	1	Shift all the display to the right. Cursor moves according to the display

6.2.6 Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit
When DL="High", it means 8-bit bus mode with MPU.
When DL="Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-but bus mode, it needs to transfer 4-bit data twice.
N: Display line number control bit
When N="Low", 1-line display mode is set.
When N="High", 2-line display mode is set.
F: Display line number control bit
When F="Low", 5x8 dots format display mode is set.
When F="High", 5x11 dots format display mode.

6.2.7 Set CGRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
The instruction makes CGRAM data available from MPU.

6.2.8 Set DDRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N=LOW), DDRAM address is form “00H” to “4FH”.In 2-line display mode (N=High), DDRAM address in the 1st line form “00H” to “27H”, and DDRAM address in the 2nd line is from “40H” to “67H”.

6.2.9 Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether ST7066 is in internal operation or not. If the resultant BF is “High”, internal operation is in progress and should wait BF is to be LOW, which by then the nest instruction can be performed. In this instruction you can also read the value of the address counter.

6.2.10 Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set). RAM set instruction can also determine the AC direction to RAM. After write operation. The address is automatically increased/decreased by 1, according to the entry mode.

6.2.11 Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before, read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register. After read operation, address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation. At this time, AC indicates next address position, but only the previous data can be read by the read instruction.

7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static, it may cause damage to the CMOS ICs.
9. Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

7.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the OLED module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.