PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG/14/8369
Dated 05 Mar 2014

Assembly and Testing capacity expansion, for the product housed in TO-220FP package at the Nantong Fujitsu Microelectronics (NFME) Subcontractor

Table 1. Change Implementation Schedule

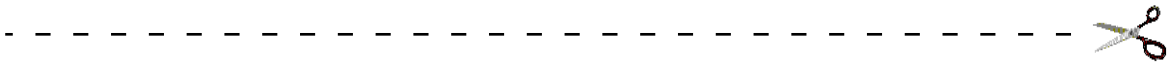
Forecasted implementation date for change	21-May-2014
Forecasted availability date of samples for customer	26-Feb-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	26-Feb-2014
Estimated date of changed product first shipment	04-Jun-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Assembly additional location
Reason for change	To improve service to ST Customers
Description of the change	To respond the ever increasing demand for the products housed in TO-220FP package, ST is glad to announce the expansion of capacity at NFME Subcontractor factory located in China. For the complete list of the part numbers affected by this change, please refer to the attached Products List.
Change Product Identification	"GF" marked on the package
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG/14/8369**
Please sign and return to STMicroelectronics Sales Office	**Dated 05 Mar 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Giuffrida, Antonino	Marketing Manager
Martelli, Nunzio	Product Manager
Vitali, Gian Luigi	Q.A. Manager

PRODUCT/PROCESS
CHANGE NOTIFICATION

IPG Group

Assembly and Testing capacity expansion, for the product housed in TO-220FP package,
at the Nantong Fujitsu Microelectronics (NFME) Subcontractor plant.

Packages typology

TO-220FP

WHAT:

To respond the ever increasing demand for the products housed in TO-220FP package, ST is glad to announce the expansion of capacity at NFME Subcontractor factory located in China. For the complete list of the part numbers affected by this change, please refer to the attached Products List.

Samples of the test vehicle devices are available right now. Any other sample request will be granted upon request.

WHY:

To improve service to ST Customers

HOW:

By expanding capacity according the ST quality and reliability standard.

The changed here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant product's datasheets.
There are as well neither modifications in the packing modes nor in the standard delivery quantities.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests.
Please refer to Appendix 1 for all the details.

WHEN:

Production start and first shipments will occur as indicated in the table below.

Affected Product Types	Samples	1st Shipment
Power MOSFET	**Now**	**Wk 20-14**
Rectifier	**Now**	**Wk 20-14**

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts produced in NFME will be ensured by the Q.A. number and plant code identification “GF” marked on the package, as illustrated in the below picture.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change.
After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer’s written agreement.

Reliability Report
TO-220FP assembly and testing subcontractor qualification for STPSxxxFP and STTHxxxFP products (capacity extension)

General Information	
Product Line	*BU78*
Product Description	*Rectifier*
Part numbers	*STPSxxxFP* *STTHxxxFP*
Product Group	*IPG*
Product division	*ASD&IPAD*
Package	*TO-220FP*
Maturity level step	*Qualified*

Locations	
Wafer fab	*ST Ang Mo Kio (Singapore)* *ST Tours (France)*
Assembly plant	*Subcontractor (China)*
Reliability Lab	*ST Tours*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	10/02/2014	8	Aude DROMEL	Jean-Paul REBRASSE	

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

SS	Sample Size
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB	Temperature Humidity Bias
IOLT	Intermittent Operating Life Test
AC	Autoclave (Pressure Cooker Test)
RSH	Resistance to Solder Heat

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify the expansion of capacity for products housed in TO-220FP packages in a new subcontractor factory in China.

The reliability test methodology used follows the JESD47-H: « Stress Test Driven Qualification Methodology ». Rectifier diodes perimeter is covered through 5 different test vehicles including turbo/bipolar diodes and Schottky barrier diodes. These test vehicles have been chosen to include the most critical parameters for reliability (die size, highest voltage, etc.)
The following reliability tests are:

- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- TC and IOLT to ensure the mechanical robustness of the products.
- THB/AC to check the robustness to corrosion and the good package hermeticity.
- RSH

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

All bipolar rectifers and power schottky in TO-220 Full Pack package.

4.2 Construction Note

	STTHxxxFP
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours (France)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours (France)
Assembly information	
Assembly site	Subcontractor (China)
Package description	TO-220FP
Molding compound	ECOPACK®2 ("Halogen-free")
Lead finishing material	Tin (Sn 100%)
Final testing information	
Testing location	Subcontractor (China)

	STPSxxxFP
Wafer/Die fab. information	
Wafer fab manufacturing location	*ST Ang Mo Kio (Singapore)*
Wafer Testing (EWS) information	
Electrical testing manufacturing location	*ST Ang Mo Kio (Singapore)*
Assembly information	
Assembly site	Subcontractor (China)
Package description	TO-220FP
Molding compound	ECOPACK®2 ("Halogen-free")
Lead finishing material	Tin (Sn 100%)
Final testing information	
Testing location	Subcontractor (China)

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Package	Part Number	Comments for STPSxxxFP	Comments for STTHxxxFP
1	TO-220FP	STTH512FP		Die highest voltage (1200V)
2		STPS30H60CFP	60V Schottky barrier diode Big die	
3		STPS30M100SFP	100V Schottky barrier diode Big die	
4		STTH16L06CFP		600V diode, Big die
5		STTH2002CFP	200V diode	

Detailed results in below chapter will refer to these references.

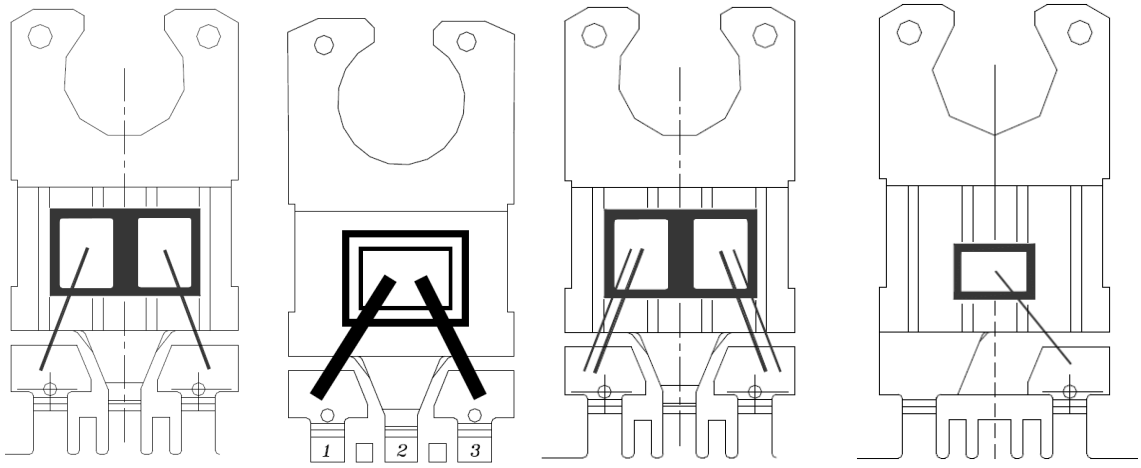
5.2 Test plan and results summary

Test	Std ref.	Conditions	SS	Steps / duration	Failure/SS					Note
					Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	
HTRB	JESD22 A-108	Tj = Tjmax* Ta= 150°C lot 1 Ta = 100°C lot 3 VR = 0.8xVRRM	153	168h	0/77		0/76			
				504h	0/77		0/76			
				1000h	0/77		0/76			
THB	JESD22 A-101	85% RH, 85°C VR=24V	75	168h	0/25		0/25		0/25	
				500h	0/25		0/25		0/25	
				1000h	0/25		0/25		0/25	
TC	JESD22 A-104	-40 +125°C 1 cycle/hour	75	500cy		0/25	0/25	0/25		
PCT	JESD22 A-102	121°C 2bar 100% RH	75	96h		0/25		0/25	0/25	
IOLT	Mil Std 750 method 1037	ΔTc = 85°C t_{on} = t_{off} = 210s	75	8572cy	0/25	0/25		0/25		
RSH	JESD22 A-106	260°C, 10sec.	10	N/A		0/10				

* Tjmax=maximal available temperature preventing from thermal runaway.

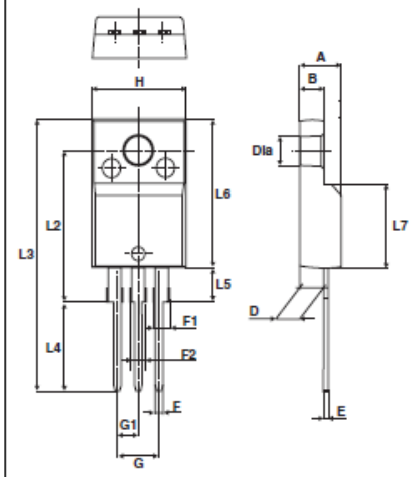
6 ANNEXES : DEVICE DETAILS

6.1 Pin connection



6.2 Package outline / mechanical data

Table 6. TO-220FPAB dimensions



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.4	4.6	0.173	0.181
B	2.5	2.7	0.098	0.106
D	2.5	2.75	0.098	0.108
E	0.45	0.70	0.018	0.027
F	0.75	1	0.030	0.039
F1	1.15	1.70	0.045	0.067
F2	1.15	1.70	0.045	0.067
G	4.95	5.20	0.195	0.205
G1	2.4	2.7	0.094	0.106
H	10	10.4	0.393	0.409
L2	16 Typ.		0.63 Typ.	
L3	28.6	30.6	1.126	1.205
L4	9.8	10.6	0.386	0.417
L5	2.9	3.6	0.114	0.142
L6	15.9	16.4	0.626	0.646
L7	9.00	9.30	0.354	0.366
Dia.	3.00	3.20	0.118	0.126

6.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
PCT Pressure Cooker Test (Autoclave)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
IOLT Intermittent Operating Life Test	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly, not gradually, to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only. Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO39).	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
RSH Resistance to Solder Heat	Device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.

Reliability Report

Assembly and Testing capacity expansion, for the product housed in TO-220FP package, at the Nantong Fujitsu Microelectronics (NFME) Subcontractor plant (China).

General Information	
Product Lines:	ED6E – TZ63 – QD0J – M266 – EZ9K
Product Families:	Power MOSFET
P/Ns:	STP55NF06FP (ED6E) STF6N62K3 (TZ63) STP80NF10FP (QD0J) STF26NM60N (M266) STF9NK90Z (EZ9K)
Product Group:	IPG
Product division:	Power Transistor Division
Package:	TO-220FP
Silicon Process techn.:	STripFET™ II Power MOSFET Supermesh™ PowerMOSFET MDmesh™ II Power MOSFET

Locations	
Wafer Diffusion Plants:	*Ang Mo Kio (Singapore)* *Catania CT8 (Italy)*
EWS Plants:	*Ang Mo Kio (Singapore)* *Catania CT8 (Italy)*
Assembly plant:	*Nantong Fujitsu Microelectronics (China)*
Reliability Lab:	*IPG-PTD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	February 2014	14	A. Settinieri	C. Cappello	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Capacity expansion activities of the TO-220FP package graded Molding Compound manufactured in NFME Subcontractor factory located in China.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET

4.2 Construction note

D.U.T.: STP55NF06FP LINE: ED6E PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	STripFET™ II Enhancement N-channel Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	2510 x 3560 μm^2
Metal	Al/Si/Cu
Passivation type	NONE

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – 15 mils Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	TESEC

D.U.T.: STF6N62K3 LINE: TZ63 PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	SuperMESH III High Voltage Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	3990 x 2890 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – 7 mils Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	TESEC

D.U.T.: STP80NF10FP LINE: QD0J PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	STripFET™ II Enhancement N-channel Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	4620 x 5670 μm^2
Metal	Al/Si
Passivation type	NONE

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – 15 mils Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	TESEC

D.U.T.: STF26NM60N LINE: M266 PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania CT8 (Italy)
Technology	MDmesh™ II Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	4980 x 4600 µm^2
Metal	AlCu/Ti/TiN
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania CT8 (Italy)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – 10 mils Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	TESEC

D.U.T.: STF9NK90Z LINE: EZ9K PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	SuperMESH High Voltage Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	6330 x 4630 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – 10 mils Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	TESEC

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STP55NF06FP	ED6E	Power MOSFET
2	STF6N62K3	TZ63	
3	STP80NF10FP	QD0J	
4	STF26NM60N	M266	
5	STF9NK90Z	EZ9K	

5.2 Reliability test plan summary

Lot. 1 - D.U.T.: STP55NF06FP LINE: ED6E PACKAGE: TO-220FP

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 1
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=175°C Vdss=48V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 20V	77	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 175°C	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=50V	25	168 H 500 H 1000 H	0/25
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	25	100 cy 200 cy 500 cy	0/25
TF/IOL	N	Mil-STD 750D Method 1037	ΔTc=+105°C	25	5K cy 10K cy	0/25
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	25	96 H	0/25

Lot. 2 - D.U.T.: STF6N62K3 LINE: TZ63 PACKAGE: TO-220FP

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 2
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=500V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 30V	77	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 150°C	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	25	168 H 500 H 1000 H	0/25
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	25	100 cy 200 cy 500 cy	0/25
TF/IOL	N	Mil-STD 750D Method 1037	ΔTc=+105°C	25	5K cy 10K cy	0/25
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	25	96 H	0/25

Lot. 3 - D.U.T.: STP80NF10FP LINE: QD0J PACKAGE: TO-220FP

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 3
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=175°C Vdss=80V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 20V	77	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 150°C	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=80V	25	168 H 500 H 1000 H	0/25
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	25	100 cy 200 cy 500 cy	0/25
TF/IOL	N	Mil-STD 750D Method 1037	ΔTc=+105°C	25	5K cy 10K cy	0/25
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	25	96 H	0/25

Lot. 4 - D.U.T.: STF26NM60N LINE: M266 PACKAGE: TO-220FP

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 4
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=480V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 30V	77	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 150°C	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	25	168 H 500 H 1000 H	0/25
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	25	100 cy 200 cy 500 cy	0/25
TF/IOL	N	Mil-STD 750D Method 1037	ΔTc=+105°C	25	5K cy 10K cy	0/25
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	25	96 H	0/25

Lot. 5 - D.U.T.: STF9NK90Z LINE: EZ9K PACKAGE: TO-220FP

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 5
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=720V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 30V	77	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 150°C	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	25	168 H 500 H 1000 H	0/25
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	25	100 cy 200 cy 500 cy	0/25
TF/IOL	N	Mil-STD 750D Method 1037	ΔTc=+105°C	25	5K cy 10K cy	0/25
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	25	96 H	0/25

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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