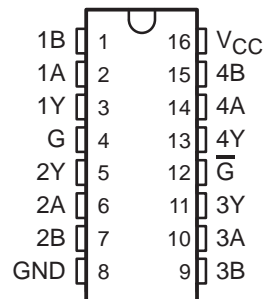


# SN75LVDS32, SN75LVDS9637 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

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- Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard
- Operates With a Single 3.3-V Supply
- Designed for Signaling Rate of up to 155 Mbps
- Differential Input Thresholds  $\pm 100$  mV Max
- Low-Voltage TTL (LVTTTL) Logic Output Levels
- Open-Circuit Fail Safe
- Characterized For Operation From 0°C to 70°C

SN75LVDS32D (Marked as 75LVDS32)  
SN75LVDS32PW (Marked as DS32)  
(TOP VIEW)



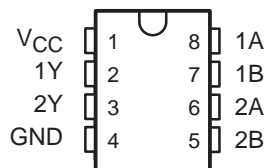
## description

The SN75LVDS32 and SN75LVDS9637 are differential line receivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four differential receivers provides a valid logical output state with a  $\pm 100$  mV allow operation with a differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100  $\Omega$ . The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN75LVDS32 and SN75LVDS9637 are characterized for operation from 0°C to 70°C.

SN75LVDS9637D (Marked as DF637 or 7L9637)  
SN75LVDS9637DGK (Marked as AXI)  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

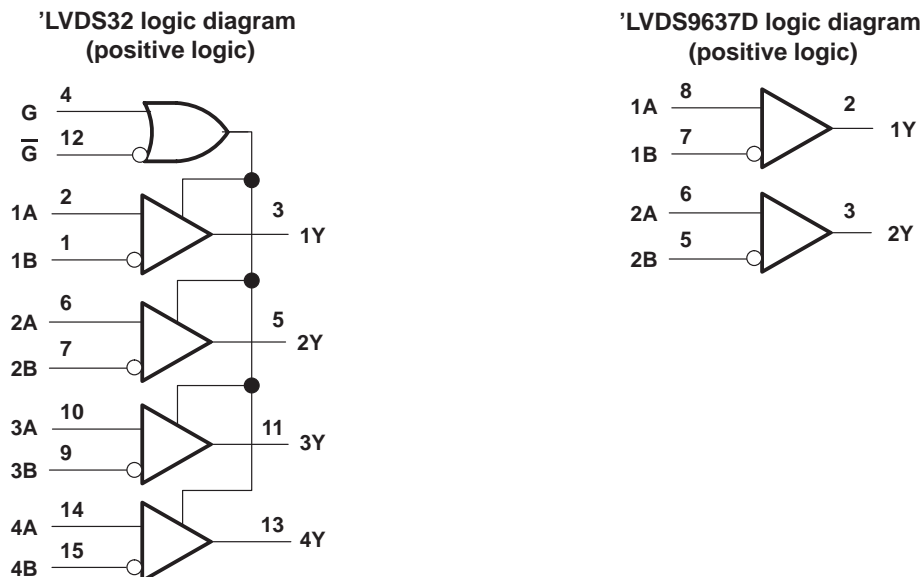
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# SN75LVDS32, SN75LVDS9637 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

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## logic diagram

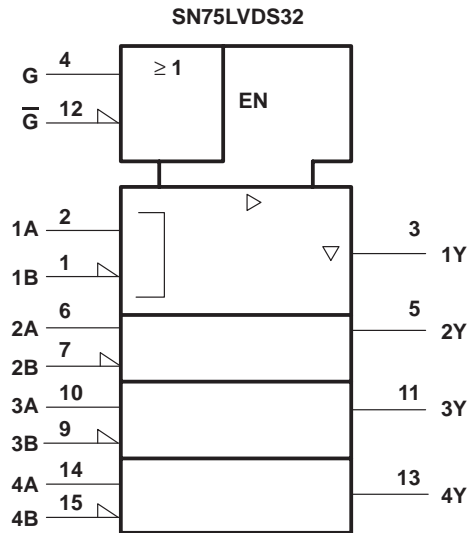


### Function Tables

SN75LVDS32			
DIFFERENTIAL INPUT	ENABLES		OUTPUT
A, B	G	$\bar{G}$	Y
$V_{ID} \geq 100 \text{ mV}$	H	X	H
	X	L	H
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	H	X	?
	X	L	?
$V_{ID} \leq -100 \text{ mV}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off), ? = indeterminate

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

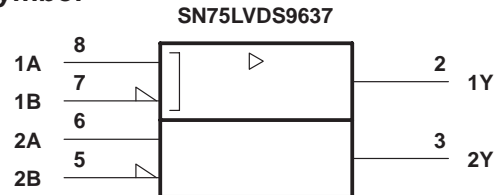
## Function Table

SN75LVDS9637

DIFFERENTIAL INPUT	OUTPUT
A, B	Y
$V_{ID} \geq 100 \text{ mV}$	H
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	?
$V_{ID} \leq -100 \text{ mV}$	L
Open	H

H = high level, L = low level, ? = indeterminate

## logic symbol†

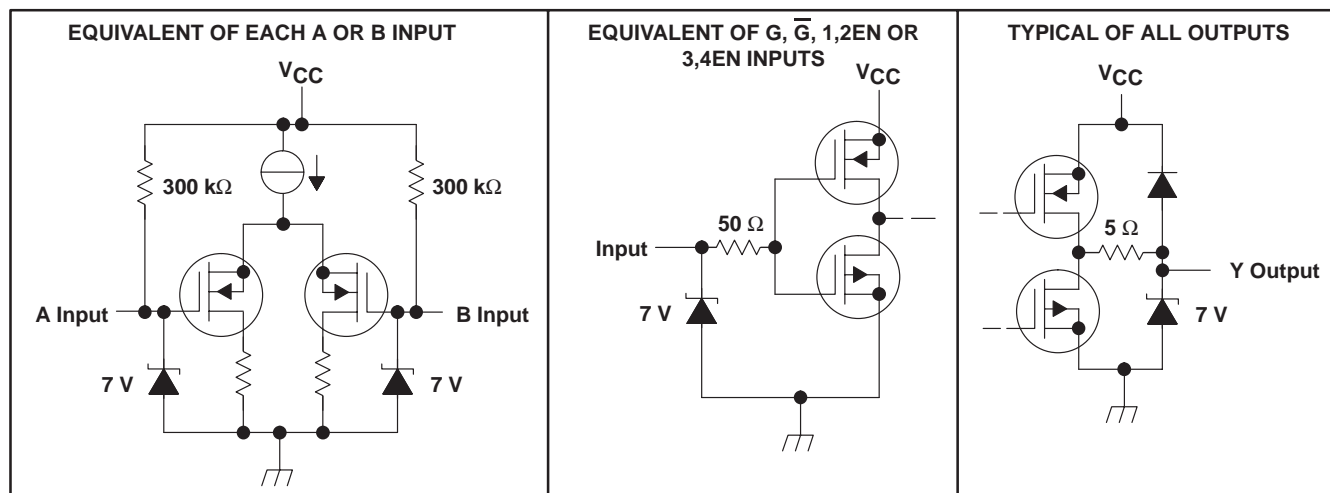


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN75LVDS32, SN75LVDS9637 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

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## equivalent input and output schematic diagrams



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1)	–0.5 V to 4 V
Input voltage range, $V_I$	–0.5 V to $V_{CC} + 0.5$ V
Input voltage range, $V_I$ (A or B)	–0.5 V to 4 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW
D (16)	950 mW	7.6 mW/°C	608 mW
PW	774 mW	6.2 mW/°C	496 mW
DGK	425 mW	3.4 mW/°C	272 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		3	3.3	3.6	V
High-level input voltage, $V_{IH}$	$G, \bar{G}$	2			V
Low-level input voltage, $V_{IL}$	$G, \bar{G}$			0.8	V
Magnitude of differential input voltage, $ V_{ID} $		0.1		0.6	V
Common-mode input voltage, $V_{IC}$ (see Figure 1)		$\frac{ V_{ID} }{2}$	$2.4 - \frac{ V_{ID} }{2}$		V
			$V_{CC} - 0.8$		V
Operating free-air temperature, $T_A$		0		70	°C

**COMMON-MODE INPUT VOLTAGE RANGE  
vs  
DIFFERENTIAL INPUT VOLTAGE**

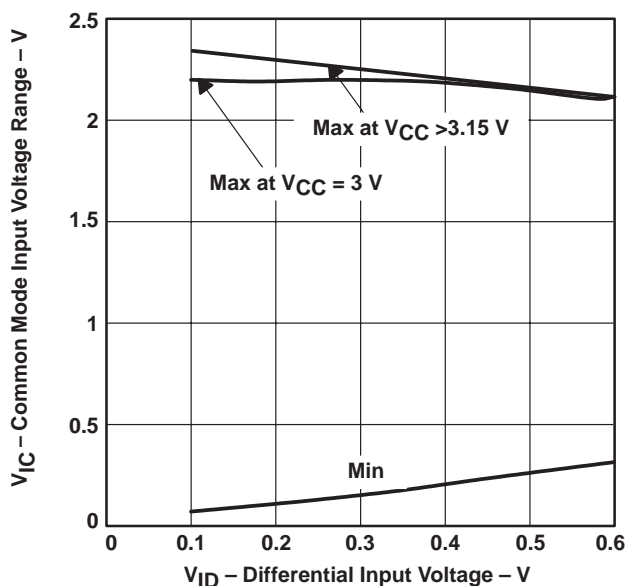


Figure 1.  $V_{IC}$  Versus  $V_{ID}$  and  $V_{CC}$

# SN75LVDS32, SN75LVDS9637 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

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## SN75LVDSxxxx electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN75LVDS32, SN75LVDS9637			UNIT	
			MIN	TYP†	MAX		
V <sub>I</sub> TH+	Positive-going differential input voltage threshold	See Figure 2 and Table 1	100			mV	
V <sub>I</sub> TH-	Negative-going differential input voltage threshold‡		-100			mV	
V <sub>O</sub> H	High-level output voltage	I <sub>OH</sub> = -8 mA	2.4			V	
V <sub>O</sub> L	Low-level output voltage	I <sub>OL</sub> = 8 mA	0.4			V	
I <sub>CC</sub>	Supply current	SN75LVDS32	Enabled, No load		10	18	mA
			Disabled		0.25	0.5	
		SN75LVDS9637	No load		5.5	10	
I <sub>I</sub>	Input current (A or B inputs)	V <sub>I</sub> = 0		-2	-10	-20	µA
		V <sub>I</sub> = 2.4 V		-1.2	-3		
I <sub>I</sub> (OFF)	Power-off input current (A or B inputs)	V <sub>CC</sub> = 0, V <sub>I</sub> = 3.6 V		6	20	µA	
I <sub>I</sub> H	High-level input current (G, or $\overline{G}$ inputs)	V <sub>I</sub> H = 2 V		10		µA	
I <sub>I</sub> L	Low-level input current (G, or $\overline{G}$ inputs)	V <sub>I</sub> L = 0.8 V		10		µA	
I <sub>OZ</sub>	High-impedance output current	V <sub>O</sub> = 0 or V <sub>CC</sub>		±10		µA	

† All typical values are at T<sub>A</sub> = 25°C and with V<sub>CC</sub> = 3.3 V.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for the negative-going differential input voltage threshold only.

## SN75LVDSxxxx switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN75LVDS32, SN75LVDS9637			UNIT
			MIN	TYP†	MAX	
t <sub>p</sub> LH	Propagation delay time, low-to-high-level output	C <sub>L</sub> = 100 pF, See Figure 3	2.1		6	ns
t <sub>p</sub> HL	Propagation delay time, high-to-low-level output		2.1		6	ns
t <sub>sk</sub> (p)	Pulse skew ( t <sub>p</sub> HL - t <sub>p</sub> LH )		0.6		1.5	ns
t <sub>sk</sub> (o)	Channel-to-channel output skew†		0.7		1.5	ns
t <sub>sk</sub> (pp)	Part-to-part skew‡				0.6	ns
t <sub>r</sub>	Output signal rise time, 20% to 80%				0.6	ns
t <sub>f</sub>	Output signal fall time, 80% to 20%				1	ns
t <sub>p</sub> HZ	Propagation delay time, high-level-to-high-impedance output	See Figure 4			25	ns
t <sub>p</sub> LZ	Propagation delay time, low-level-to-high-impedance output				25	ns
t <sub>p</sub> ZH	Propagation delay time, high-impedance-to-high-level output				25	ns
t <sub>p</sub> ZL	Propagation delay time, high-impedance-to-low-level output				25	ns

† All typical values are at 25°C and with a 3.3-V supply.

‡ t<sub>sk</sub>(p) is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output

§ t<sub>sk</sub>(o) is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.

¶ t<sub>sk</sub>(pp) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.



PARAMETER MEASUREMENT INFORMATION

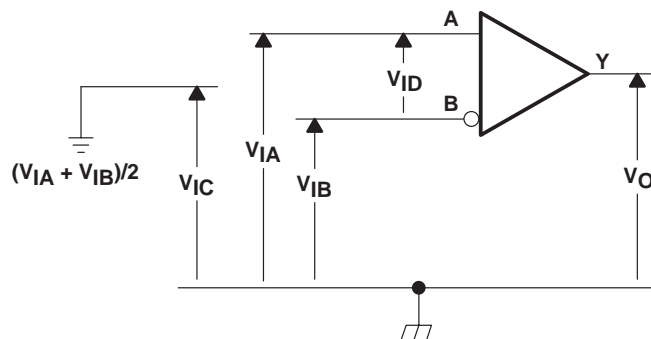


Figure 2. Voltage Definitions

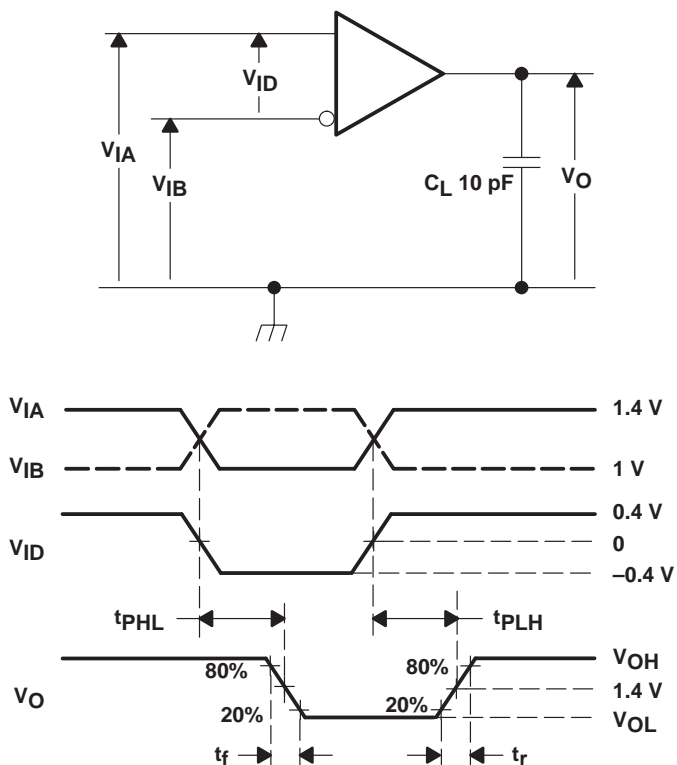
Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
$V_{IA}$	$V_{IB}$	$V_{ID}$	$V_{IC}$
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	-600 mV	0.3 V

# SN75LVDS32, SN75LVDS9637 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

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## PARAMETER MEASUREMENT INFORMATION

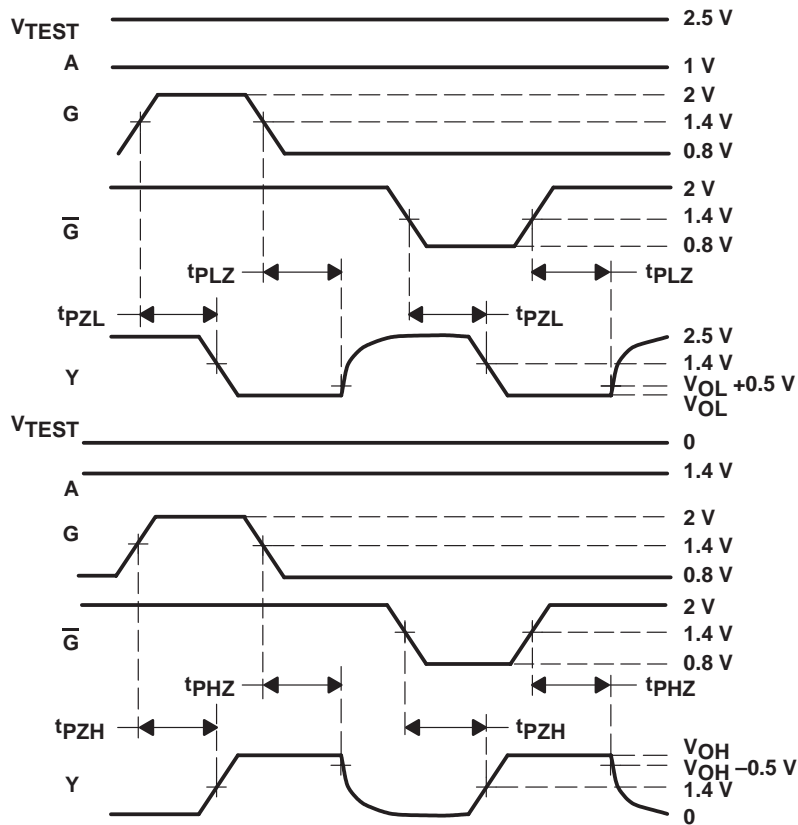
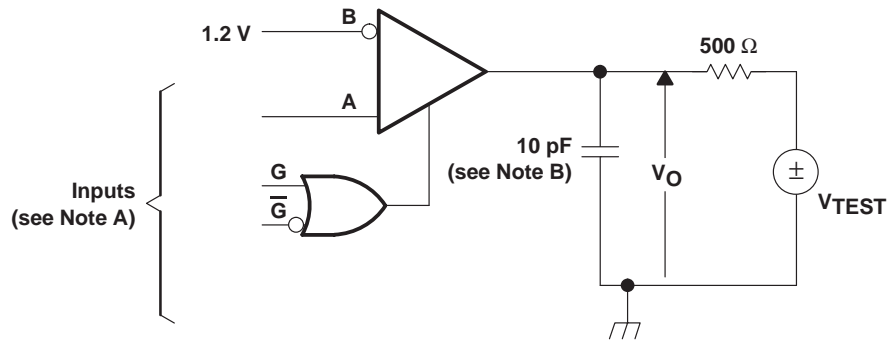


- NOTES: A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1 \text{ ns}$ , pulse repetition rate (PRR) = 50 Mpps, pulse width =  $10 \pm 0.2 \text{ ns}$ .  
B.  $C_L$  includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

**Figure 3. Timing Test Circuit and Wave Forms**



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width =  $500 \pm 10$  ns.  
B.  $C_L$  includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable/Disable Time Test Circuit and Wave Forms

# SN75LVDS32, SN75LVDS9637 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

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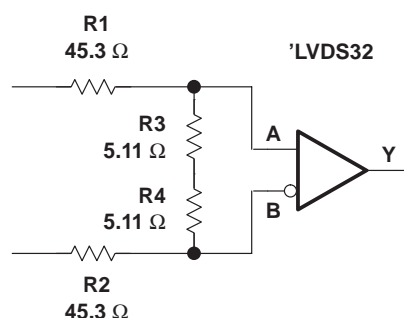
## APPLICATION INFORMATION

### using an LVDS receiver with RS-422 data

Receipt of data from a TIA/EIA-422 line driver may be accomplished using a TIA/EIA-644 line receiver with the addition of an attenuator circuit. This technique gives the user a very high-speed and low-power 422 receiver.

If the ground noise between the transmitter and receiver is not a concern (less than  $\pm 1$  V), the answer can be as simple as shown below in Figure 5. The use of a resistor divider circuit in front of the LVDS receiver attenuates the 422 differential signal to LVDS levels.

The resistors present a total differential load of  $100\ \Omega$  to match the characteristic impedance of the transmission line and to reduce the signal 10:1. The maximum 422 differential output signal or 6 V is reduced to 600 mV. The high input impedance of the LVDS receiver prevents input bias offsets and maintains a better than 200-mV differential input voltage threshold at the inputs to the divider. This circuit is used in front of each LVDS channel that also receives 422 signals.



NOTE A: The components used were standard values.

R1, R2 = NRC12F45R3TR, NIC Components, 45.3 Ohm, 1/8W, 1%, 1206 Package

R3, R4 = NRC12F5R11TR, NIC Components, 5.11 Ohm, 1/8W, 1%, 1206 Package

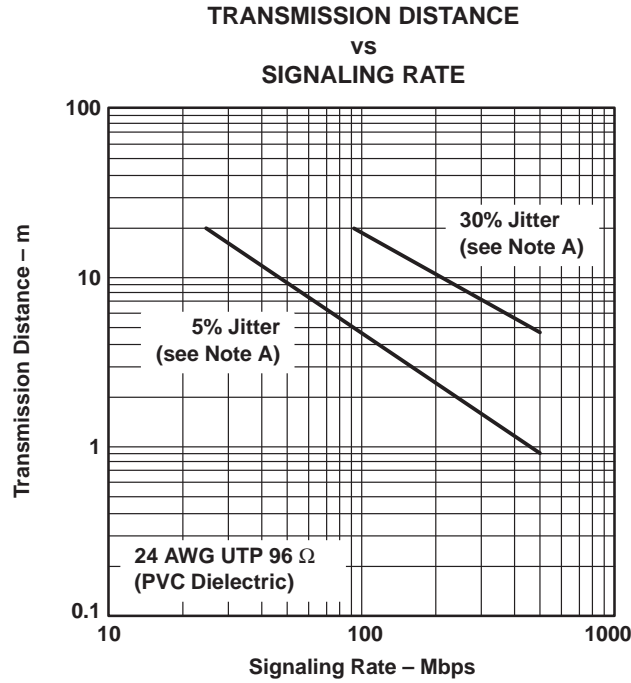
The resistor values do not need to be 1% tolerance. However, it can be difficult locating a supplier of resistors having values less than  $100\ \Omega$  in stock and readily available. The user may find other suppliers with comparable parts having tolerances of 5% or even 10%. These parts are adequate for use in this circuit.

### Figure 5. RS-422 Data Input to an LVDS Receiver Under Low Ground Noise Conditions

If ground noise between the RS-422 driver and LVDS receiver is a concern, then the common-mode voltage must be attenuated. The circuit must then be modified to connect the node between R3 and R4 to the LVDS receiver ground. This modification to the circuit increases the common-mode voltage from  $\pm 1$  V to greater than  $\pm 4.5$  V.

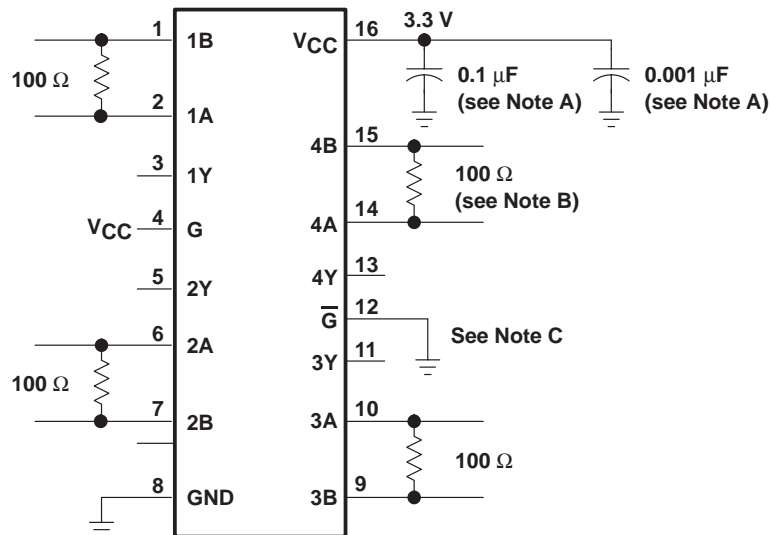
APPLICATIONS INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission where ground differences are less than 1 V. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.



NOTE A: This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

Figure 6. Typical Transmission Distance vs Signaling Rate



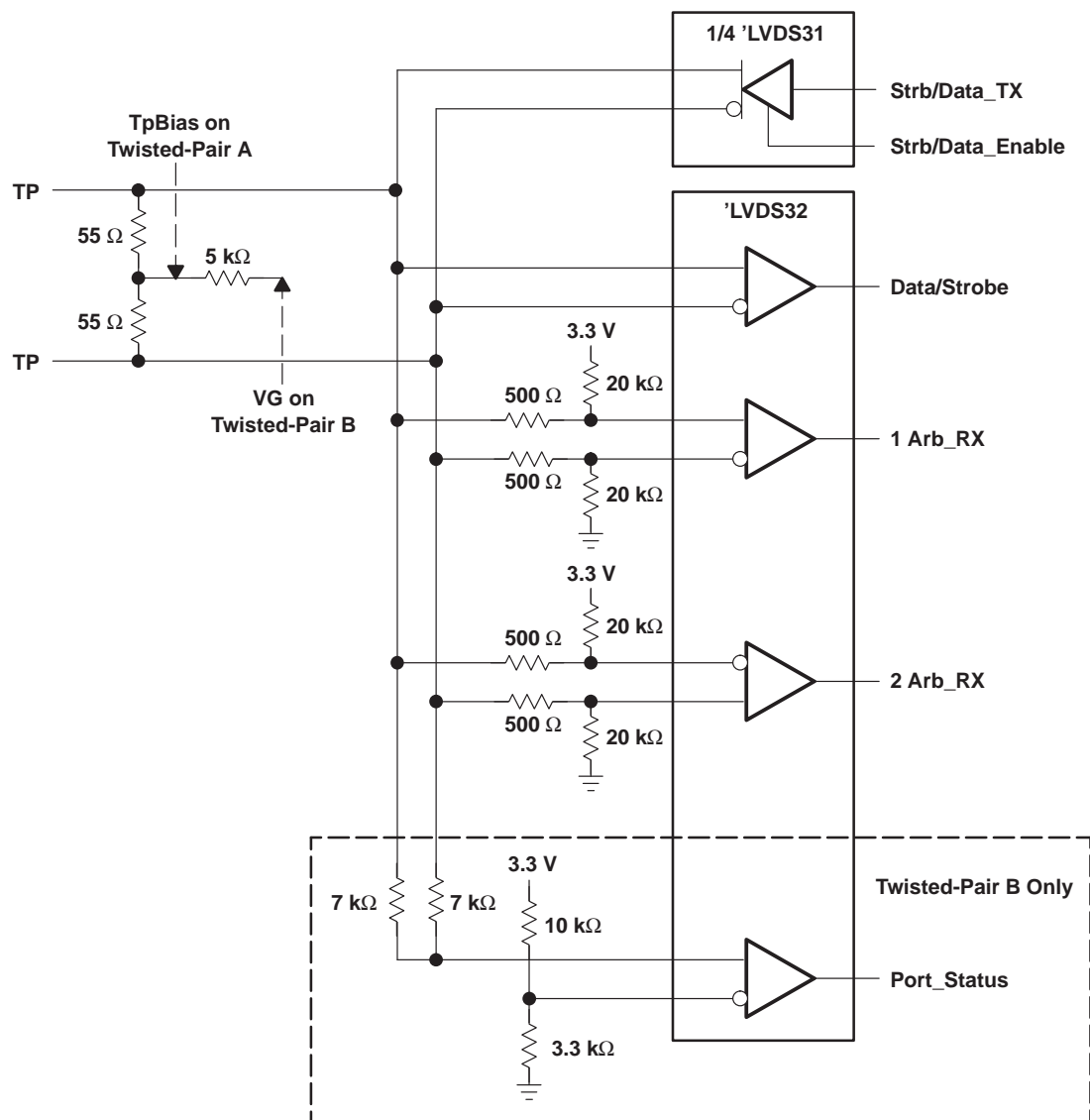
- NOTES: A. Place a 0.1  $\mu\text{F}$  and a 0.001  $\mu\text{F}$  Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between  $V_{CC}$  and the ground plane. The capacitors should be located as close as possible to the device terminals.  
 B. The termination resistance value should match the nominal characteristic impedance of the transmission media with  $\pm 10\%$ .  
 C. Unused enable inputs should be tied to  $V_{CC}$  or GND as appropriate.

Figure 7. Typical Application Circuit Schematic

# SN75LVDS32, SN75LVDS9637 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

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## APPLICATION INFORMATION



- NOTES: A. Resistors are leadless thick-film (0603) 5% tolerance.  
 B. Decoupling capacitance is not shown but recommended.  
 C.  $V_{CC}$  is 3 V to 3.6 V.  
 D. The differential output voltage of the 'LVDS31 can exceed that allowed by IEEE1394.

Figure 8. 100-Mbps IEEE 1394 Transceiver

APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between  $-100$  mV and  $100$  mV if it is within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near  $V_{CC}$  through  $300\text{-k}\Omega$  resistors as shown in Figure 9. The fail-safe feature uses an AND gate with input voltage thresholds at about  $2.3$  V to detect this condition and force the output to a high level, regardless of the differential input voltage.

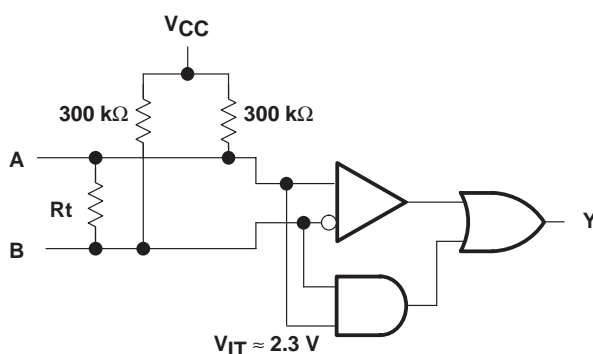


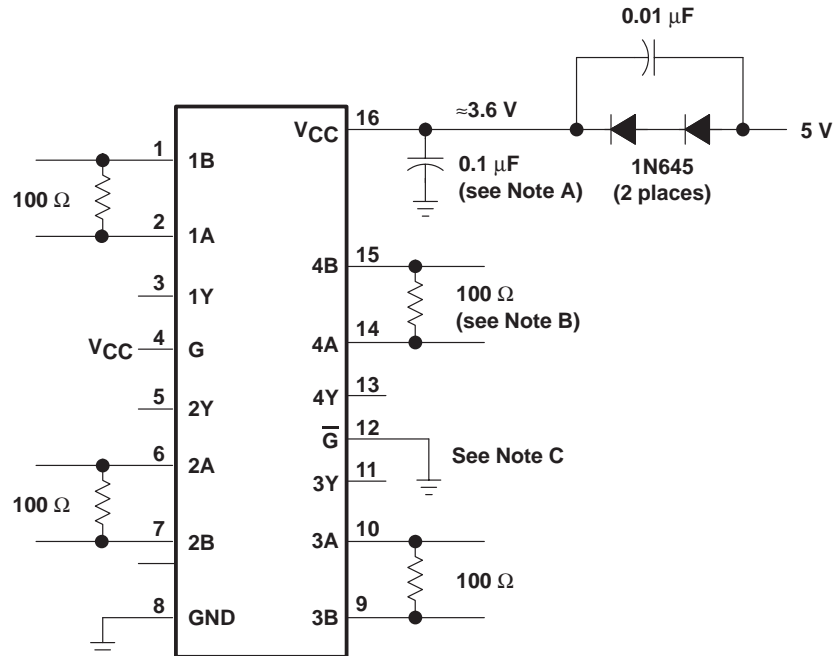
Figure 9. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a  $100\text{-mV}$  differential input voltage magnitude. The presence of the termination resistor,  $R_t$ , does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

# SN75LVDS32, SN75LVDS9637 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

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## APPLICATION INFORMATION



- NOTES: A. Place a 0.1 μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V<sub>CC</sub> and the ground plane. The capacitor should be located as close as possible to the device terminals.
- B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.
- C. Unused enable inputs should be tied to V<sub>CC</sub> or GND as appropriate.

Figure 10. Operation With 5-V Supply

### related information

IBIS modeling is available for this device. Please contact the local TI sales office or the TI Web site at [www.ti.com](http://www.ti.com) for more information.

For more application guidelines, please see the following documents:

- *Low-Voltage Differential Signalling Design Notes* (TI literature SLLA014)
- *Interface Circuits for TIA/EIA-644 (LVDS)* (TI literature SLLA038)
- *Reducing EMI with LVDS* (TI literature SLLA030)
- *Slew Rate Control of LVDS Circuits* (TI literature SLLA034)
- *Using an LVDS Receiver with RS-422 Data* (TI literature SLLA031)
- *Evaluating the LVDS EVM* (TI literature SLLA033)

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVDS32D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS32	<a href="#">Samples</a>
SN75LVDS32DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS32	<a href="#">Samples</a>
SN75LVDS9637D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	DF637	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN75LVDS32 :**

- Military: [SN55LVDS32](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS32DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS32DR	SOIC	D	16	2500	333.2	345.9	28.6

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