

Power management (dual transistors)

UMF6N

2SA2018 and 2SK3019 are housed independently in a UMT package.

●Application

Power management circuit

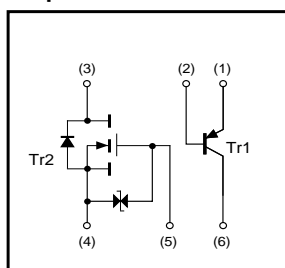
●Features

- 1) Power switching circuit in a single package.
- 2) Mounting cost and area can be cut in half.

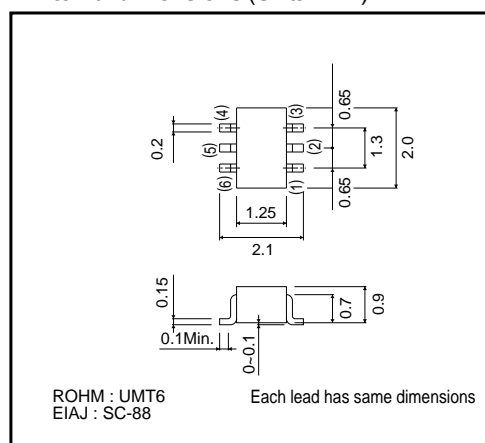
●Structure

Silicon epitaxial planar transistor

●Equivalent circuits



●External dimensions (Units : mm)



●Packaging specifications

Type	UMF6N
Package	UMT6
Marking	F6
Code	TR
Basic ordering unit (pieces)	3000

Transistors

●Absolute maximum ratings (Ta=25°C)

Tr1

Parameter	Symbol	Limits	Unit
Collector-base voltage	V _{CB0}	-15	V
Collector-emitter voltage	V _{CEO}	-12	V
Emitter-base voltage	V _{EBO}	-6	V
Collector current	I _C	-500	mA
	I _{CP}	-1.0	A *1
Power dissipation	P _C	150(TOTAL)	mW *2
Junction temperature	T _j	150	°C
Range of storage temperature	T _{stg}	-55~+150	°C

*1 Single pulse P_W=1ms

*2 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

Tr2

Parameter	Symbol	Limits	Unit
Drain-source voltage	V _{DSS}	30	V
Gate-source voltage	V _{GSS}	±20	V
Drain current	Continuous	I _D	100 mA
	Pulsed	I _{DP}	200 mA *1
Reverse drain current	Continuous	I _{DR}	100 mA
	Pulsed	I _{DRP}	200 mA *1
Total power dissipation	P _D	150(TOTAL)	mW *2
Channel temperature	T _{ch}	150	°C
Range of storage temperature	T _{stg}	-55~+150	°C

*1 P_W≤10ms Duty cycles≤50%

*2 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

●Electrical characteristics (Ta=25°C)

Tr1

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-emitter breakdown voltage	BV _{CEO}	-12	-	-	V	I _C =-1mA
Collector-base breakdown voltage	BV _{CB0}	-15	-	-	V	I _C =-10μA
Emitter-base breakdown voltage	BV _{EBO}	-6	-	-	V	I _E =-10μA
Collector cut-off current	I _{CB0}	-	-	-100	nA	V _{CB} =-15V
Emitter cut-off current	I _{EBO}	-	-	-100	nA	V _{EB} =-6V
Collector-emitter saturation voltage	V _{CE(sat)}	-	-100	-250	mV	I _C =-200mA, I _B =-10mA
DC current gain	h _{FE}	270	-	680	-	V _{CE} =-2V, I _C =-10mA
Transition frequency	f _T	-	260	-	MHz	V _{CE} =-2V, I _E =10mA, f=100MHz
Collector output capacitance	C _{ob}	-	6.5	-	pF	V _{CB} =-10V, I _E =0mA, f=1MHz

Tr2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	-	-	±1	μA	V _{GS} =±20V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	30	-	-	V	I _D =10μA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	-	-	1.0	μA	V _{DS} =30V, V _{GS} =0V
Gate-threshold voltage	V _{GS(th)}	0.8	-	1.5	V	V _{DS} =3V, I _D =100μA
Static drain-source on-state resistance	R _{DS(on)}	-	5	8	Ω	I _D =10mA, V _{GS} =4V
		-	7	13	Ω	I _D =1mA, V _{GS} =2.5V
Forward transfer admittance	Y _{fs}	20	-	-	ms	V _{DS} =3V, I _D =10mA
Input capacitance	C _{iss}	-	13	-	pF	V _{DS} =5V, V _{GS} =0V, f=1MHz
Output capacitance	C _{oss}	-	9	-	pF	
Reverse transfer capacitance	C _{rss}	-	4	-	pF	
Turn-on delay time	t _{d(on)}	-	15	-	ns	
Rise time	t _r	-	35	-	ns	I _D =10mA, V _{DD} =5V, V _{GS} =5V, R _L =500Ω, R _{GS} =10Ω
Turn-off delay time	t _{d(off)}	-	80	-	ns	
Fall time	t _f	-	80	-	ns	

Transistors

●Electrical characteristic curves

Tr1

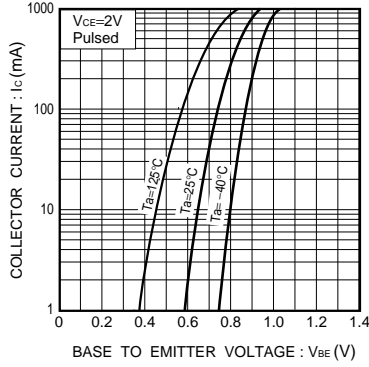


Fig.1 Grounded emitter propagation characteristics

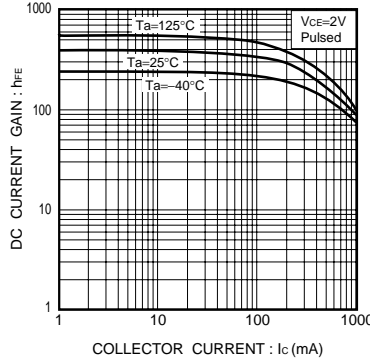


Fig.2 DC current gain vs. collector current

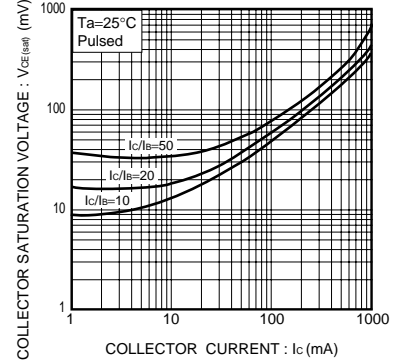


Fig.3 Collector-emitter saturation voltage vs. collector current (I)

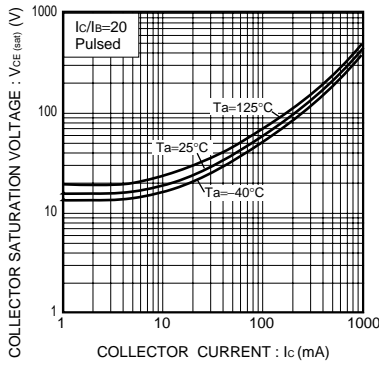


Fig.4 Collector-emitter saturation voltage vs. collector current (II)

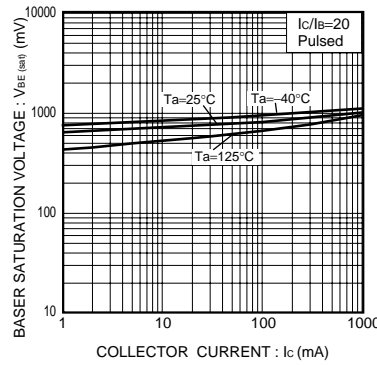


Fig.5 Base-emitter saturation voltage vs. collector current

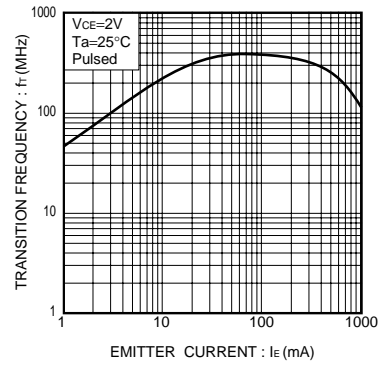


Fig.6 Gain bandwidth product vs. emitter current

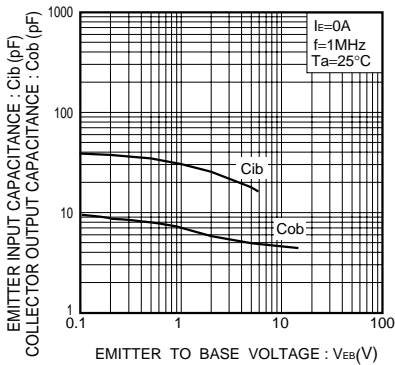


Fig.7 Collector output capacitance vs. collector-base voltage
Emitter input capacitance vs. emitter-base voltage

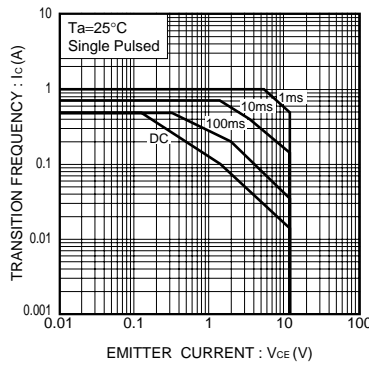


Fig.8 Safe operation area

Transistors

Tr2

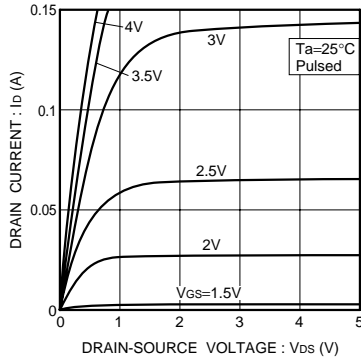


Fig.9 Typical output characteristics

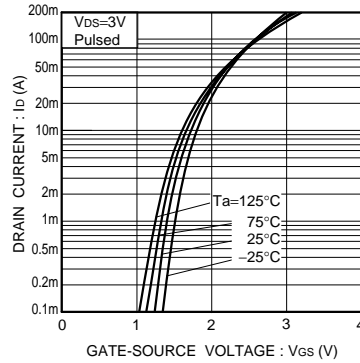


Fig.10 Typical transfer characteristics

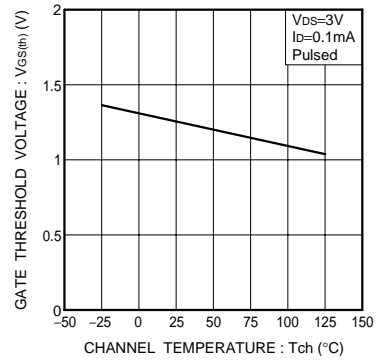


Fig.11 Gate threshold voltage vs. channel temperature

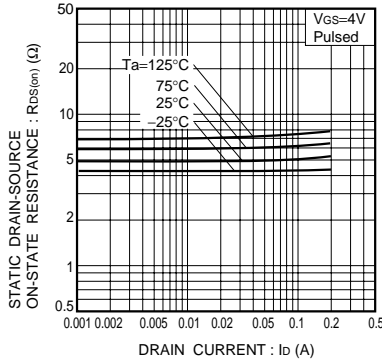


Fig.12 Static drain-source on-state resistance vs. drain current (I)

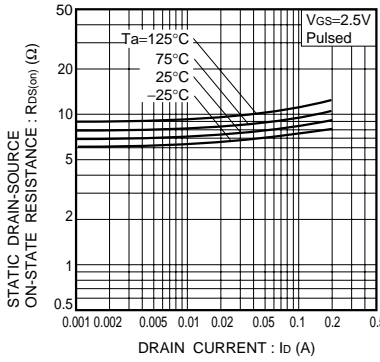


Fig.13 Static drain-source on-state resistance vs. drain current (II)

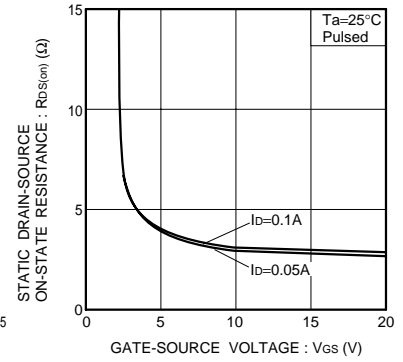


Fig.14 Static drain-source on-state resistance vs. gate-source voltage

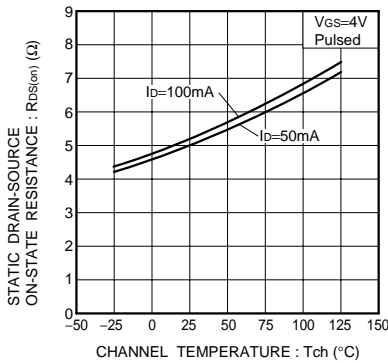


Fig.15 Static drain-source on-state resistance vs. channel temperature

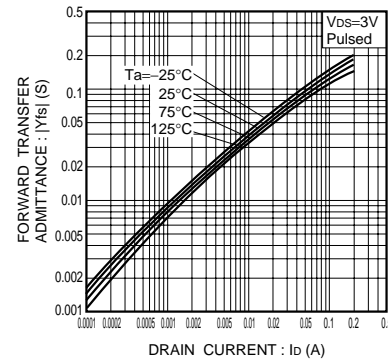


Fig.16 Forward transfer admittance vs. drain current

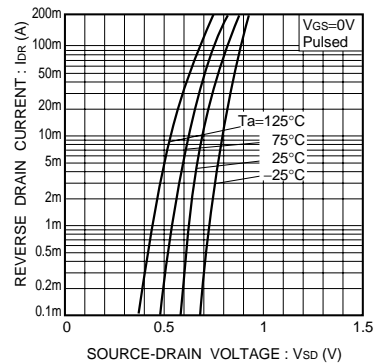


Fig.17 Reverse drain current vs. source-drain voltage (I)

Transistors

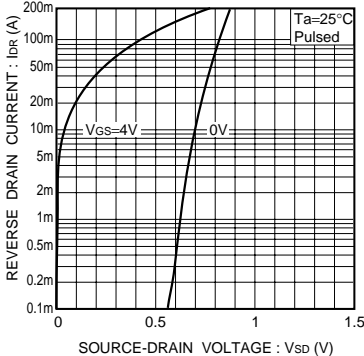


Fig.18 Reverse drain current vs. source-drain voltage (II)

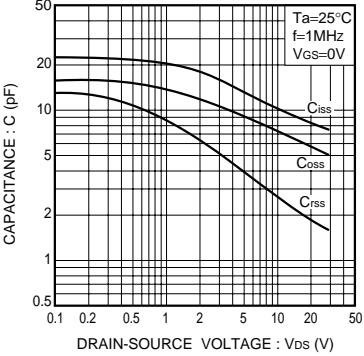


Fig.19 Typical capacitance vs. drain-source voltage

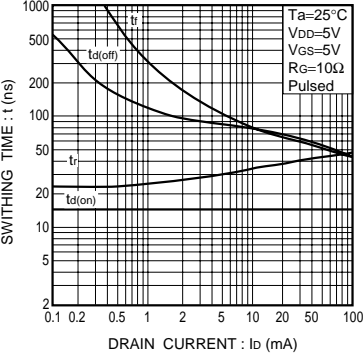


Fig.20 Switching characteristics