



A Product Line of
Diodes Incorporated



SPECIFICATION FOR APPROVAL

CUSTOMER	_____
NOMINAL FREQUENCY	48.000000 MHz
PRODUCT TYPE	TYPE FW 2.0x1.6 SEAM SEALED CRYSTAL
PART NUMBER	FW4800010Z
CUSTOMER P/N	_____
ISSUE DATE	June 8, 2018
VERSION	B

APPROVED	PREPARED	QA
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Diodes Incorporated

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- *Pb-free
- *RoHS Compliant
- *HF-Halogen Free
- *REACH Compliant

TYPE FW 2.0x1.6 SEAM SEALED CRYSTAL

FW4800010Z

VER.B 16-MAY-18

ELECTRICAL SPECIFICATIONS

Item	Symbol	Specifications	Units	Notes
Nominal Frequency	Fn	48.000000	MHz	
Mode of Oscillation	MO	AT Cut-Fundamental		
Calibration Load Capacitance	CL	10	pF	
Calibration Tolerance	FL	± 10	ppm	at 25°C $\pm 3^{\circ}\text{C}$
Operating Temperature Range	TR	-40 to +85	°C	
Frequency Stability(Frequency Deviation over the Operating Temperature Range)	F/T	± 20	ppm	Reference to the Frequency at 25°C
Operating Drive Level		10	μW	
Maximum Drive Level		100	μW	
Equivalent Series Resistance	ESR	80	Ω	Max.
Shunt Capacitance	C0	3	pF	Max.
Aging at 25°C		± 3	ppm	Max, 1st year
Storage Temperature		-55 to +125	°C	
Insulation Resistance		500	M Ω	Min

** This product doesn't include harmful substance that stipulated by SONY SS-00259 Level 1 and S-AT2-001 Level 1 standard. RoHS Compliant (Pb - Free).

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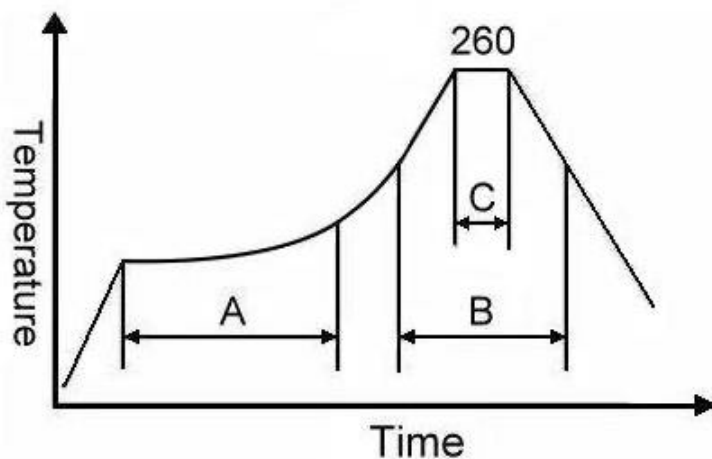
RELIABILITY SPECIFICATIONS

MECHANICAL AND ENVIRONMENTAL RATINGS:

- a) FINE LEAK TEST: JESD22-A109 (Condition 1A)
- b) GROSS LEAK TEST: JESD22-A109 (Condition C)
- c) MOISTURE RESISTANCE: JESD22-A113
- d) SHOCK: JESD22-B104 (Condition B)
- e) SOLDERABILITY : (RoHS version): J-STD-002
- f) VIBRATION: JESD22-B103
- g) SOLVENT RESISTANCE: JESD22-B107
- h) RESISTANCE TO SOLDERING HEAT (RoHS version): J-STD-020D Table 5.2 Pb free devices (3 cycles max)

SUGGESTED IR REFLOW PROFILE

*As per IPC-JEDEC J-STD-020D



Note:

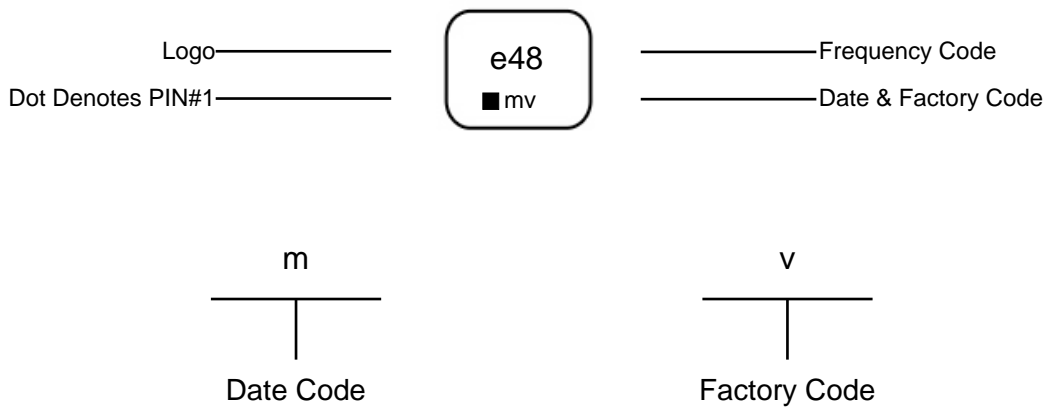
	Stage	Temperature	Time
A	Preheat	150~200°C	60~120 Sec
B	Primary Heat	217°C	60~150 Sec
C	Peak	260°C	10 Sec

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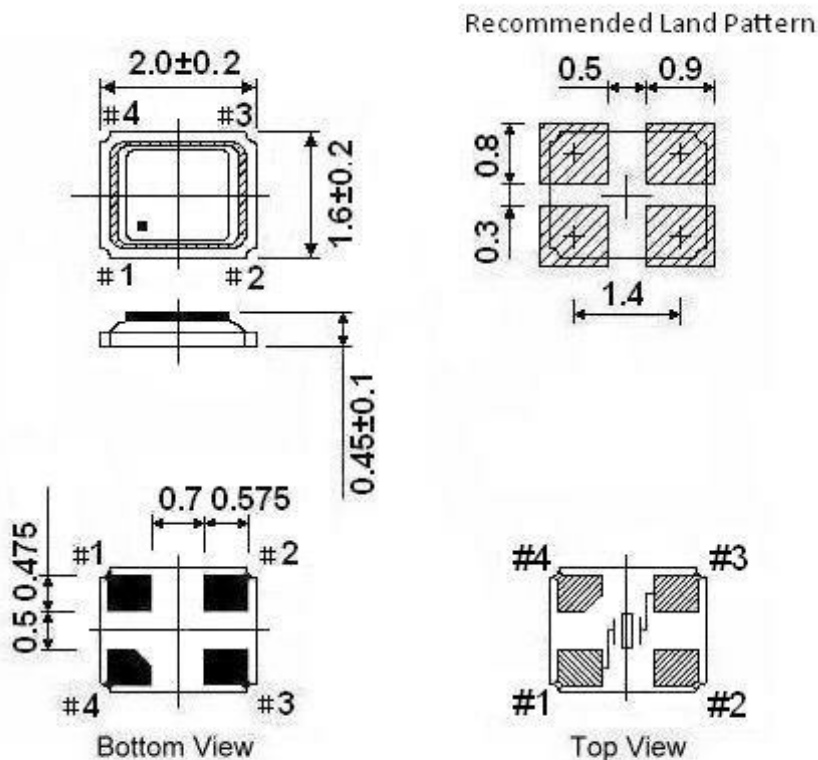
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MARKING



MECHANICAL DRAWINGS (Scale: None. Dimensions are in mm.)



** Recommended - Pin 1 & 3: CRYSTAL
Pin 2 & 4: GND

Notes:

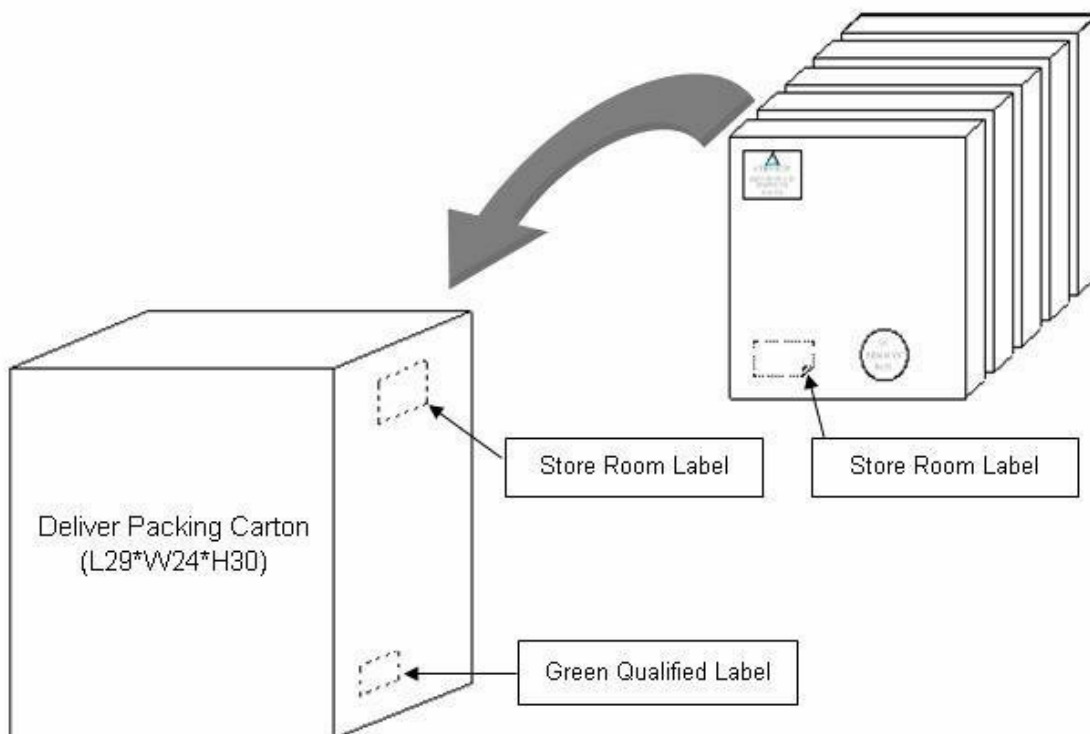
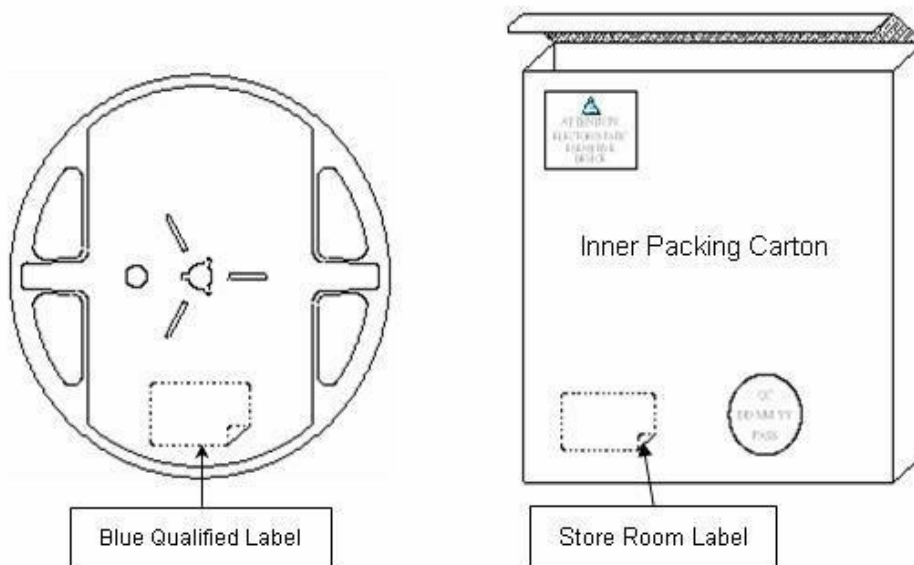
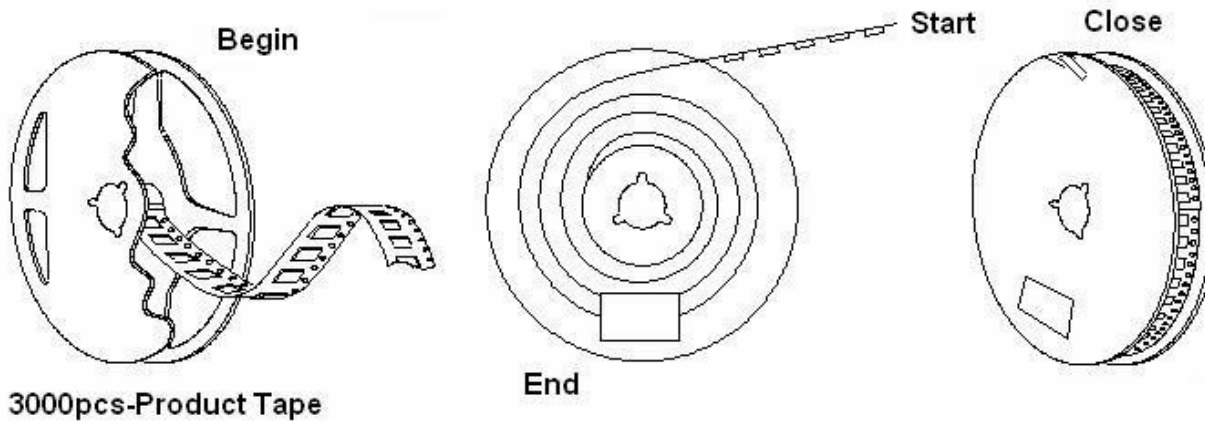
1. Package drawings are for reference only, and the appearances of objects may vary. Actual packages are based on the real product.
2. The marking dot denotes Pin#1.
3. The position and shape of the chamfer pin may vary and are based on the real product.

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PACKING



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VERSION HISTORY

Version No.	Version Date	Description	Notes
A	Aug. 9, 2013	Initial Release	
B	May. 16, 2018	Updated Logo	