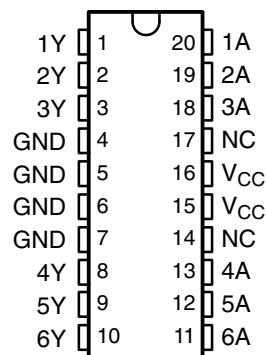


- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (N)

DB, DW, OR N PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

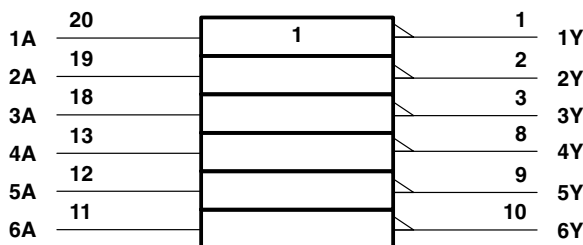
This device contains six independent inverters. It performs the Boolean function  $Y = \bar{A}$ .

The 74AC11004 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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 **TEXAS  
INSTRUMENTS**

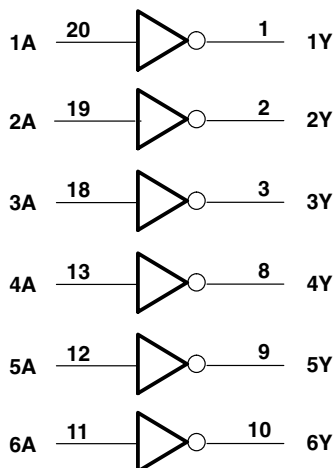
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# 74AC11004 HEX INVERTER

SCAS033B – JANUARY 1988 – REVISED APRIL 1996

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 100$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DW package	1.6 W
DB package	0.6 W
N package	1.3 W
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 5.5 V	3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	V
		V <sub>CC</sub> = 4.5 V		1.35	
		V <sub>CC</sub> = 5.5 V		1.65	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V		-4	mA
		V <sub>CC</sub> = 4.5 V		-24	
		V <sub>CC</sub> = 5.5 V		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V		12	mA
		V <sub>CC</sub> = 4.5 V		24	
		V <sub>CC</sub> = 5.5 V		24	
Δt/Δv	Input transition rise or fall rate	0		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40		85	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9		2.9		V	
		4.5 V	4.4		4.4			
		5.5 V	5.4		5.4			
	I <sub>OH</sub> = -4 mA	3 V	2.58		2.48			
		4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
I <sub>OH</sub> = -75 mA†	5.5 V			3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V			0.1	0.1	V	
		4.5 V			0.1	0.1		
		5.5 V			0.1	0.1		
	I <sub>OL</sub> = 12 mA	3 V			0.36	0.44		
		4.5 V			0.36	0.44		
		5.5 V			0.36	0.44		
I <sub>OL</sub> = 75 mA†	5.5 V				1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1	±1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4	40	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3.5			pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

# 74AC11004 HEX INVERTER

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A	Y	1.5	6.1	9	1.5	10	ns
$t_{PHL}$			1.5	5.2	7.4	1.5	8.2	

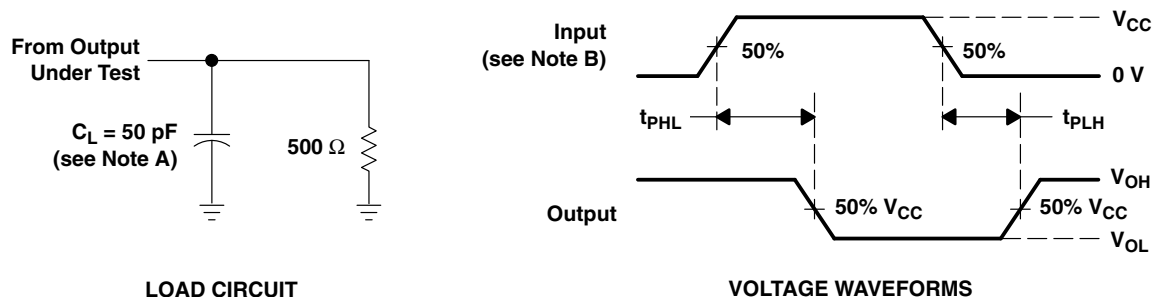
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A	Y	1.5	4.2	6.3	1.5	7.1	ns
$t_{PHL}$			1.5	3.8	5.5	1.5	6	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per inverter	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	29	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AC11004DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11004	<a href="#">Samples</a>
74AC11004DWE4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11004	<a href="#">Samples</a>
74AC11004DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11004	<a href="#">Samples</a>
74AC11004N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	74AC11004N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AC11004DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AC11004DWR	SOIC	DW	20	2000	367.0	367.0	45.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
74AC11004DW	DW	SOIC	20	25	507	12.83	5080	6.6
74AC11004DWE4	DW	SOIC	20	25	507	12.83	5080	6.6
74AC11004N	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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