500 W telecom power supply for 5G small cells using 600 V CoolMOS™ G7 and CFD7 in DDPAK

EVAL_500W_5G_PSU

Author: Alessandro Pevere

About this document

Scope and purpose

This document presents Infineon's complete system solution for a 500 W power supply unit (PSU) targeting the new 5G specifications for outdoor small-cell telecom rectifiers.

The PSU (**Figure 1**) comprises a front-end AC-DC semi-bridgeless dual-boost converter followed by a back-end DC-DC isolated half-bridge (HB) LLC converter. The front-end converter provides power factor correction (PFC) and control of the total harmonic distortion (THD). The LLC converter provides safety isolation and a tightly regulated output voltage at 12 V DC.

The measured peak efficiency of the complete PSU at 230 V AC is around 96.5 percent and 95.6 percent at 115 V AC. The overall outer dimensions of the PSU are 150 mm x 80 mm x 27 mm, which yields a power density in the range of 25 W/inch^3.

This document describes the converter system architecture and hardware, with a summary of the experimental results, including thermal characterization with a water cooling system that enables a constant baseplate temperature of the PSU.

The main Infineon components used in the **EVAL_500W_5G_PSU** are:

- 600 V CoolMOS™ G7 80 mΩ (**IPDD60R080G7**) in the PFC high-frequency MOSFETs
- 600 V CoolMOS™ S7 22 mΩ (**IPT60R022S7**) in the PFC line-rectification MOSFETs
- CoolSiC™ 650 V 8 A (**IDH08G65C6**) in the PFC high-frequency diodes
- 600 V CoolMOS™ CFD7 75 mΩ (**IPDD60R075CFD7**) in the DC-DC primary-side HB
- OptiMOS™ 6 40 V 1.3 mΩ (**IQE013N04LM6**) in the DC-DC secondary-side bridge
- EiceDRIVER™ **1EDN8550** and **1EDI20N12**, for driving the PFC and DC-DC CoolMOS™, respectively
- EiceDRIVER™ **2EDN7524** for driving the OptiMOS™
- **ICE3PCS01G** IC for the PFC control implementation
- **ICE1HS01G-1** IC for the DC-DC control implementation
- **IR11688S** IC for the secondary-side bridge control implementation
- **ICE2QR2280G** for the bias supply implementation

About this document

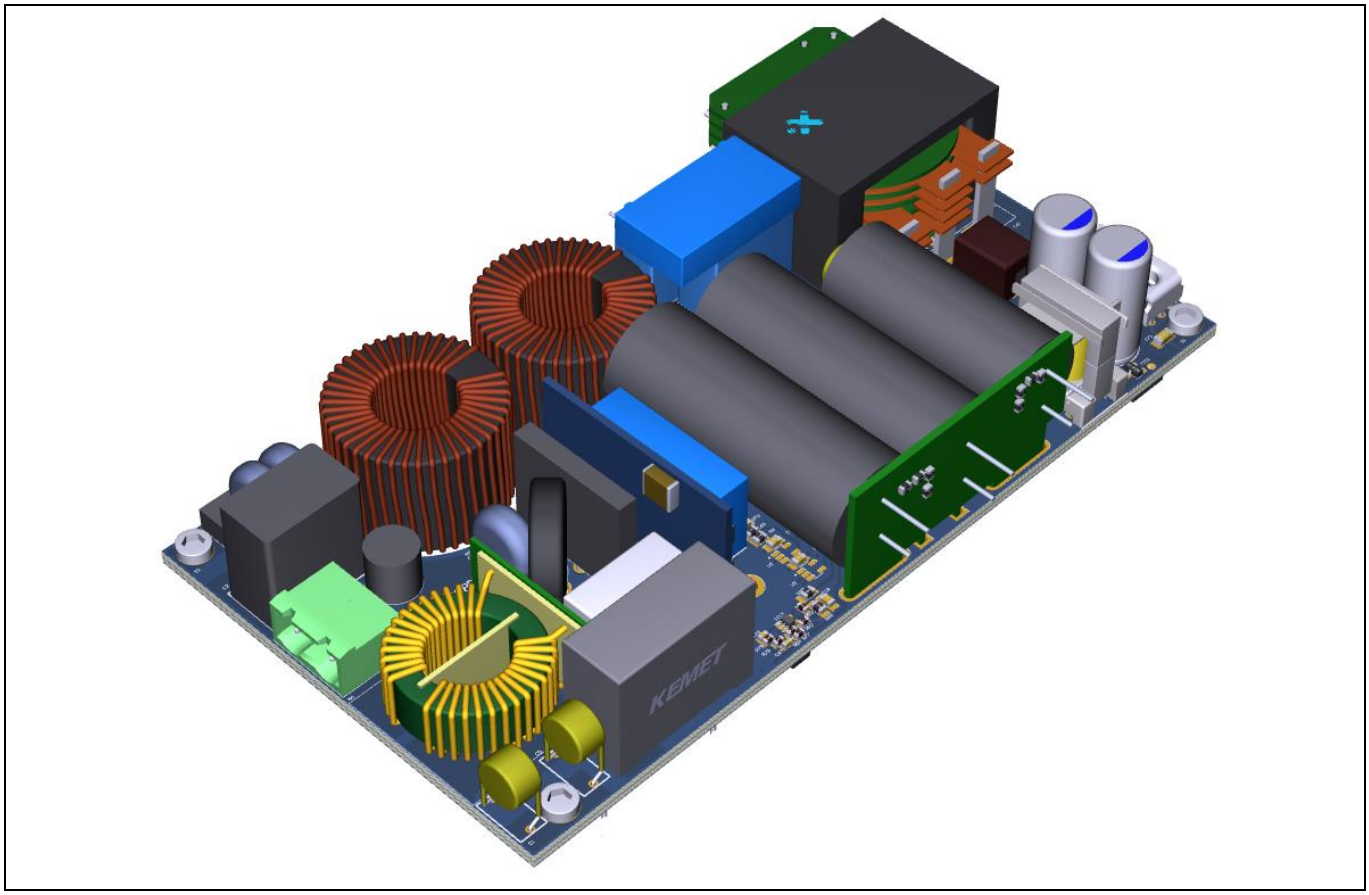

Figure 1 500 W fanless power supply with CoolMOS™ and fully analog control

Evaluation board/kit

Product(s) embedded on a PCB, with focus on specific applications and defined use cases that can include software. PCB and auxiliary circuits are optimized for the requirements of the target application.

Note: Boards do not necessarily meet safety, EMI and quality standards (for example UL, CE) requirements.

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Safety information – your safety is our goal

Please read this document carefully before starting up the device.

Figure 2 Electrical hazard and hot surface warning

Important notice

Evaluation boards, demonstration boards, reference boards and kits are electronic devices typically provided as an open-frame and unenclosed printed circuit board (PCB) assembly. Each board is functionally qualified by electrical engineers and strictly intended for use in development laboratory environments. Any other use and/or application is strictly prohibited. Our boards and kits are solely for qualified and professional users who have training, expertise and knowledge of electrical safety risks in the development and application of high-voltage electrical circuits.

Please note that evaluation boards, demonstration boards, reference boards and kits are provided "as is" (i.e., without warranty of any kind). Infineon is not responsible for any damage resulting from the use of its evaluation boards, demonstration boards, reference boards or kits.

To make our boards as versatile as possible, and to give you (the user) opportunity for the greatest degree of customization, the virtual design data may contain different component values than those specified in the bill of materials (BOM). In this specific case, the BOM data has been used for production.

Before operating the board (i.e., applying a power source), please read the application note/user guide carefully and follow the safety instructions. Please check the board for any physical damage which may have occurred during transport. If you find damaged components or defects on the board, do not connect it to a power source. Contact your supplier for further support. If no damage or defects are found, start the board up as described in the user guide or test report. If you observe unusual operating behavior during the evaluation process, immediately shut off the power supply to the board and consult your supplier for support.

Operating instructions

Do not touch the device during operation, and keep a safe distance.

Do not touch the device after disconnecting the power supply, as several components may still store electrical voltage and can discharge through physical contact. Several parts, like heatsinks and transformers, may still be very hot. Allow the components to cool before touching or servicing.

All work such as construction, verification, commissioning, operation, measurements, adaptations and other work on the device (applicable national accident prevention rules must be observed) must be done by trained personnel. The electrical installation must be completed in accordance with the appropriate safety requirements.

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the converter system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the AC input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the converter before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the converter, power electronics and associated equipment should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A converter that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the cabling, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*

1 Introduction

1.1 Background of the application

In the context of the upcoming 5G technology era, the development of the new generation of communications networks (5G networks, satellite networks, etc.) addresses important challenges, attempting to provide a wide variety of services and applications with unseen data rates.

As a consequence, the requirements of the network power supply are also changing. The 5G equipment is more sensitive to the quality of the electricity supply and must operate in a broad variety of environments, both indoors and outdoors, as shown by the new 5G telecom ecosystem in **Figure 3**.

In this new concept, macro base stations with baseband units and macro cells are coupled with emerging small-cell units.

Small cells are low-powered radio access points that connect mobile devices to mobile networks over a small area. They typically reuse frequencies on an extremely dense basis to take full advantage of the available spectrum.

5G changes this dynamic by allowing mobile cores and core routers to flip rapidly between active and idle states. Higher bandwidths and compression techniques will let 5G networks shuttle more data through systems in a given period, leaving more power-saving idle time.

5G delivers coverage to an area in a different way from 4G. Instead of using large masts that cover up to 30 km in any direction, it relies on “small cells” to provide local coverage over extremely limited areas, usually between 10 m and 2,500 m. Some of these will operate directionally.

However, these changes mean that power supplies need to evolve.

Small cells will need to be able to fit into compact environments, such as traffic lights, utility poles and rooftops. This means PSUs will need to be compact, able to fit comfortably alongside the equipment they power.

All these requirements have been translated in a power supply specification for outdoor small-cell application that has driven the design of **EVAL_500W_5G_PSU**. The full specification is described in the following section.

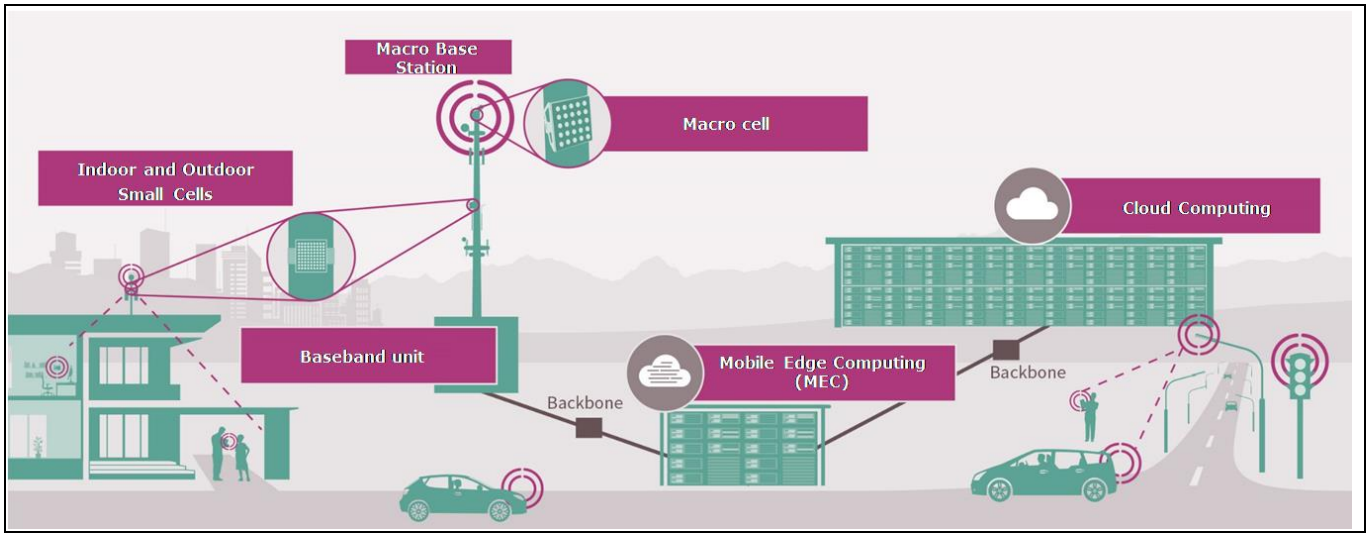


Figure 3 Example of 5G telecom environment

1.2 Main features

This application note provides a detailed description of the design considerations and experimental results of a high-efficiency, high-power-density, ultra-compact telecom rectifier for 5G small-cell applications.

Here are the key features of this demo board:

- Attractive **compact design** in 25 W/in^3 form factor for a 500 W PSU
- **Low profile** – 27 mm maximum PSU height
- Very **high efficiency** for 12 V output PSU: above 96 percent from 60 percent of the rated load upward when V_{in} = 230 V AC, and above 95 percent from 60 percent of the rated load upward when V_{in} = 115 V AC
- **Fanless** design with the possibility of attaching the demo board to a heatsink
- **Fully analog control** implementation using an innovative control scheme for the dual-boost PFC based on standard ICE3 and using ICE1 plus IR11688S for control of the V DC LLC
- **High thermal performance** achieved by using Infineon's best-in-class devices in top-side cooling DDPAK package
- **Robust and reliable** operation under different abnormal conditions:
  - Load-jump reaction and output regulation
  - Inrush current during start-up
- 4 kV line-to-neutral and line-to-GND **surge immunity**
- **Active-line rectification** thanks to CoolMOS™ S7

Table 2 presents a summary of the main specifications and requirements of the telecom rectifier.

Table 2 Summary of the requirements and specifications for the 5G PSU

Requirements	Conditions	Specification
Input voltage V_{in}	85 V AC to 305 V AC	100 V AC to 240 V AC nominal
Output voltage V_{ref}		12 V DC nominal
Output power	85 V AC to 305 V AC 12 V DC	500 W
Efficiency target	230 V AC input, 12 V DC output 115 V AC input, 12 V DC output (Baseplate temperature less than 60°C)	η greater than 96 percent (from 60 percent of load) η greater than 95 percent (from 60 percent of load)
Steady-state V_{out} ripple	Nominal input, 12 V DC output	$\lvert\Delta V_{out}\rvert$ less than 50 mV_{pk-pk}
Power factor and THD	100 V AC to 240 V AC	Greater than 0.9 from 20 percent of load
Load transient	5 A ↔ 35 A, 1 A/µs	$\lvert\Delta V_{out}\rvert$ less than 1.2 V_{pk}
	35 A ↔ 5 A, 1 A/µs	

Requirements	Conditions	Specification
Ambient temperature	PSU operating	-40°C to +85°C
	Non-destructive	+85°C to 100°C
Dimensions	Not including plastic cover	H_{max} = 27 mm W_{max} = 80 mm L_{max} = 150 mm
Cooling		Natural/convection
Hold-up time	80 percent of power	20 ms with V DC greater than 10.8 V
EMI		EN 55022 class A with a 6 dB margin
Surge	IEC61000-4-5 standard (1.2/50 µs, 2 Ω impedance, performance criterion A)	Differential mode: 4 kV Common mode: 4 kV

1.3 Topology selection

Based on the requirements from **Table 2**, a first topology selection was made during the concept phase of this demo board.

Especially for the PFC stage, several topologies have been analyzed in order to understand the most suitable one for this power supply. Furthermore, all the semiconductor technologies have been considered, i.e., standard silicon, silicon carbide (SiC) and gallium nitride (GaN) based MOSFETs.

The benchmarking tree of PFC topologies considered is shown in **Figure 4**.

Multiple aspects have been taken into account during the PFC selection, such as the total number of components (including synchronous rectification MOSFETs, drivers, diodes and magnetic elements), power density, control complexity, device package availability, overall system price and thermal performance.

Out of the topologies shown in **Figure 4**, three candidates were selected as most suitable for this application: Si-based semi-bridgeless dual-boost, SiC-based and GaN-based bridgeless totem-pole PFCs.

Efficiency simulations of the three topologies have been performed in both low-line (115 V AC) and high-line (230 V) input conditions. As shown in **Figure 4**, in all the topologies active-line rectification with CoolMOS™ S7 was considered in order to replace standard bridge diodes.

Figure 5 and **Figure 6** show that all three topologies are capable of meeting the required efficiency specification. The totem pole based on GaN shows the best efficiency performance, even if the delta efficiency benefit compared to the others is relatively small.

Finally, the topology selected for the PFC was the semi-bridgeless dual-boost, thanks to its better thermal dissipation (each leg is operating for only half of the line cycle), lower control complexity (with reduced number of sensors) and power density requirement matching (even though totem-pole topology enabled this to increase further).

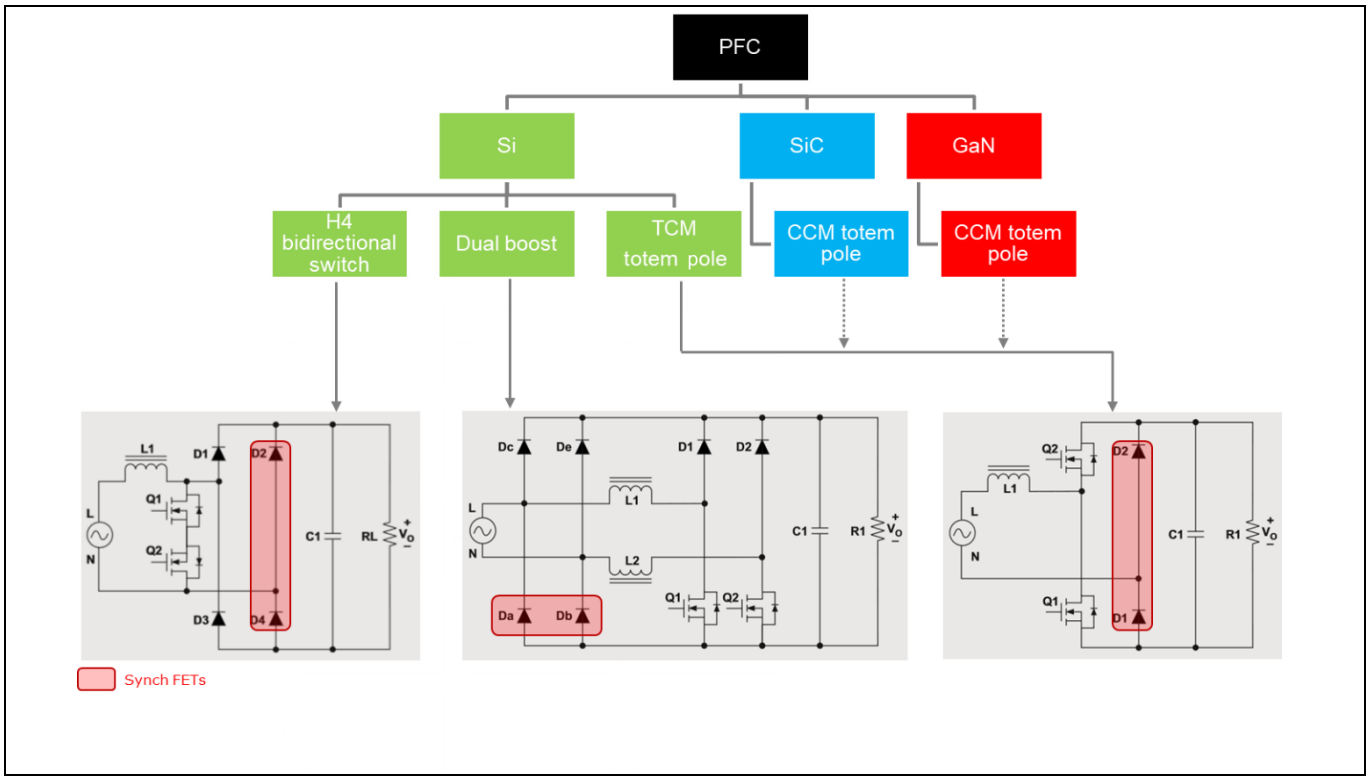


Figure 4 PFC topology selection

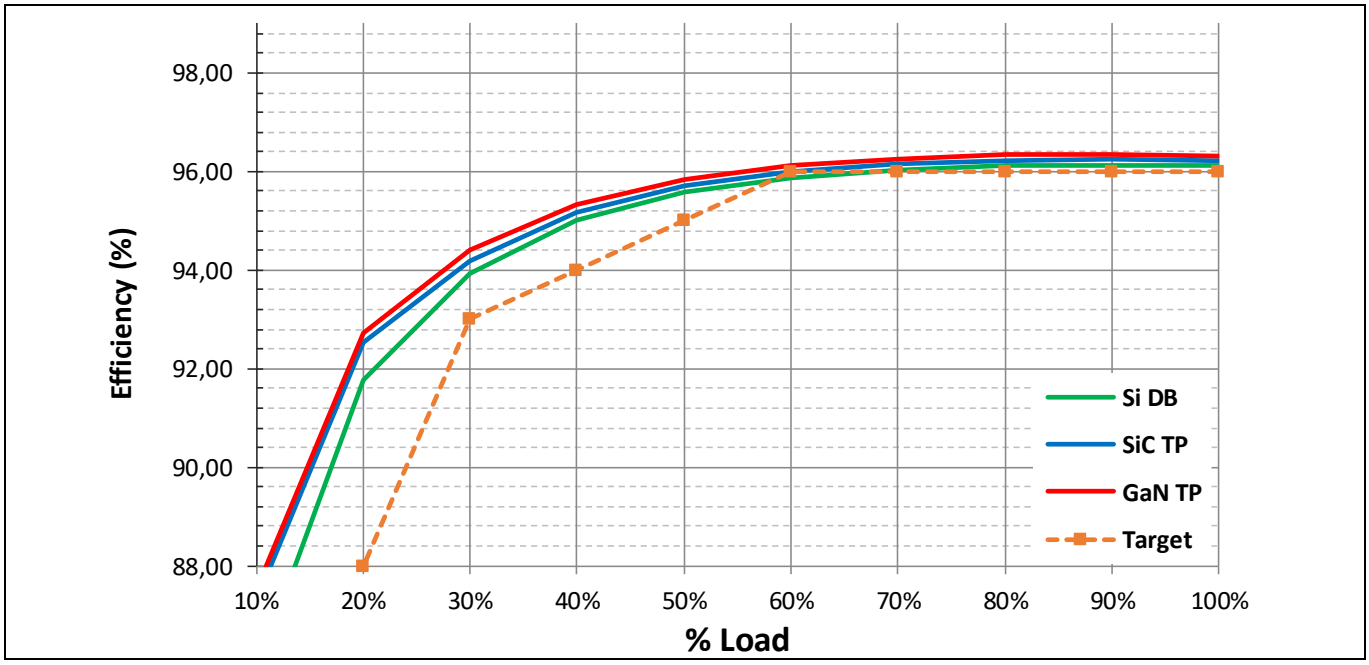


Figure 5 5G 500 W power supply efficiency estimation and target at 230 V AC

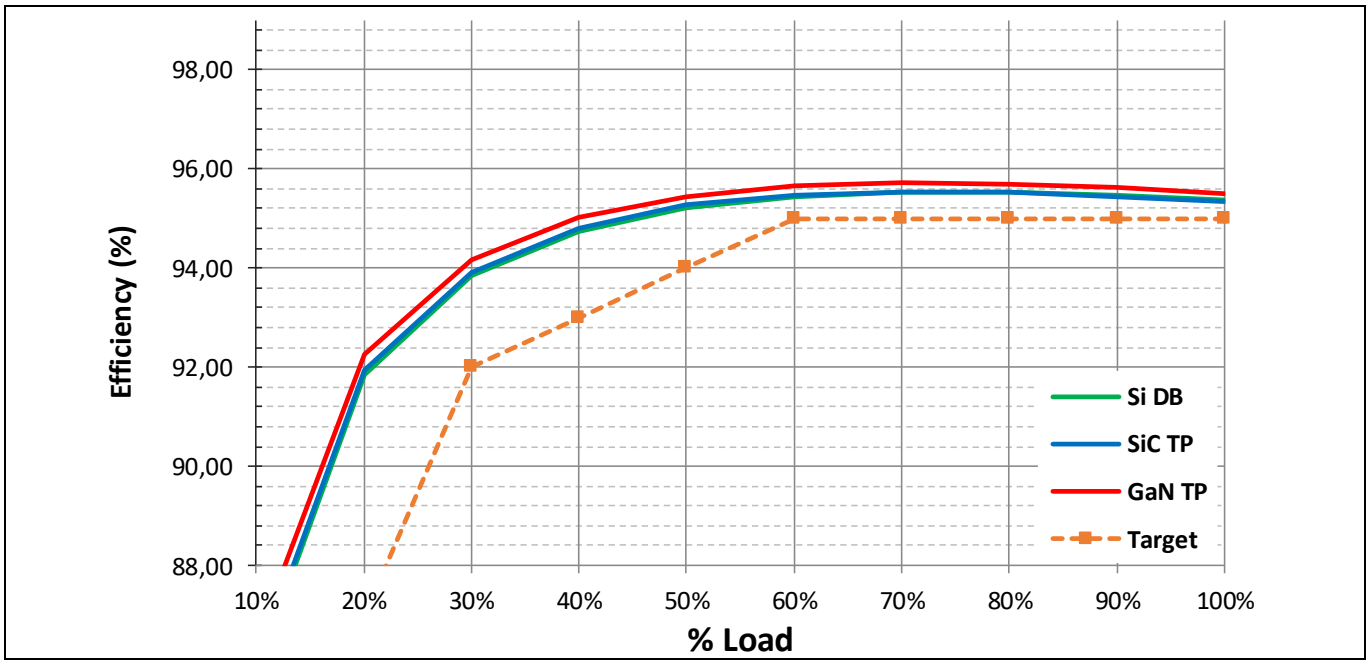


Figure 6 5G 500 W power supply efficiency estimation and target at 115 V AC

2 System architecture description

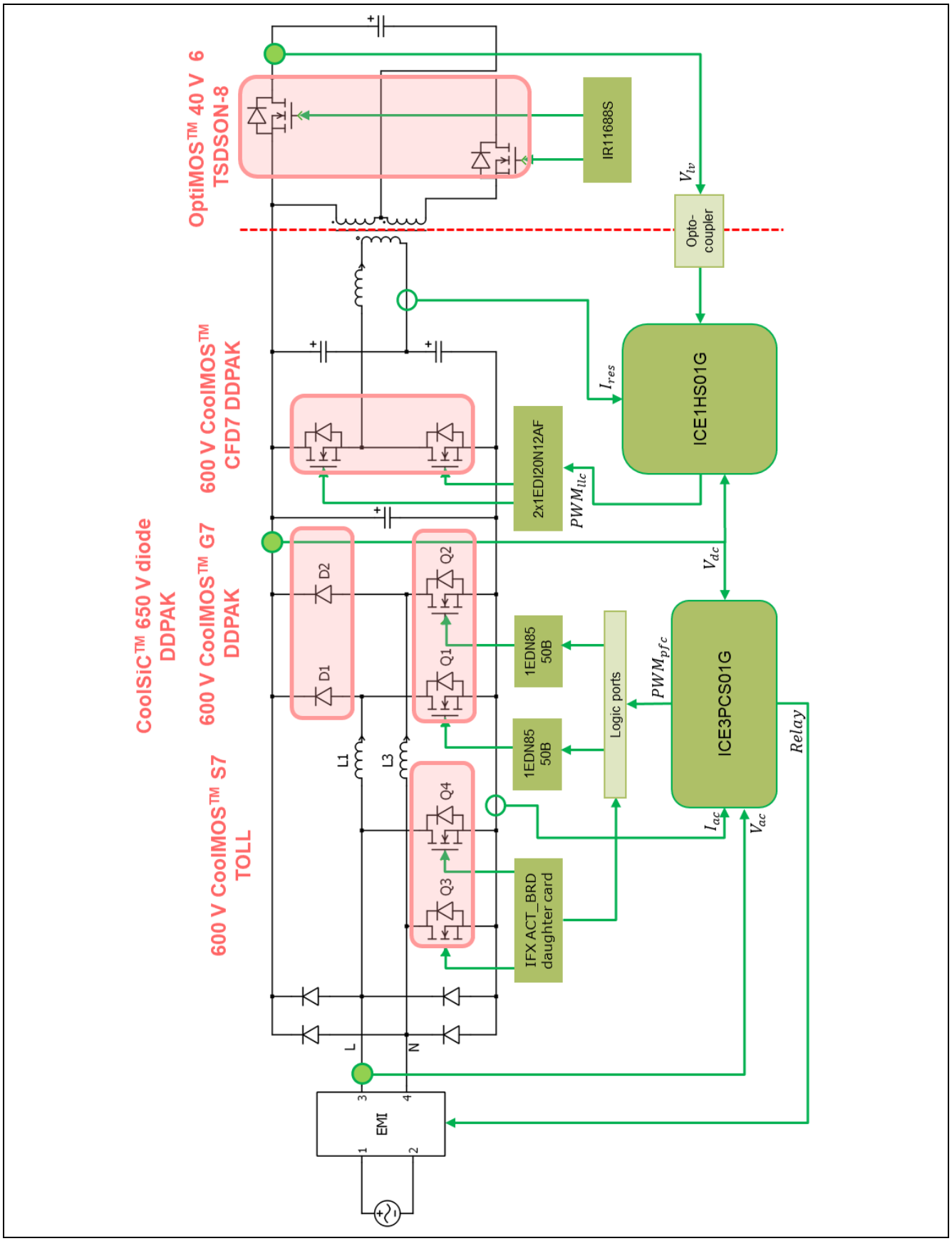


Figure 7 **Simplified schematic of the EVAL_500W_5G_PSU, showing the topologies implemented and the Infineon semiconductors used**

The simplified circuit diagram of the **EVAL_500W_5G_PSU** demo board is shown in **Figure 7**.

The PSU comprises a front-end AC-DC semi-bridgeless dual-boost converter followed by a back-end DC-DC isolated V DC LLC converter. The front-end converter provides power factor correction (PFC) and control of the total harmonic distortion (THD). The LLC converter provides safety isolation and a tightly regulated output voltage at 12 V DC.

The control of the dual-boost AC-DC converter is implemented with the standard CCM boost PFC **ICE3PCS01G** Infineon analog controller, which includes PFC, THD, voltage regulation, input overcurrent protection (OCP), overvoltage protection (OVP), undervoltage protection (UVP), undervoltage lockout (UVLO) and soft-start. Further details about the analog controller and additional functionalities can be found in **[1]**.

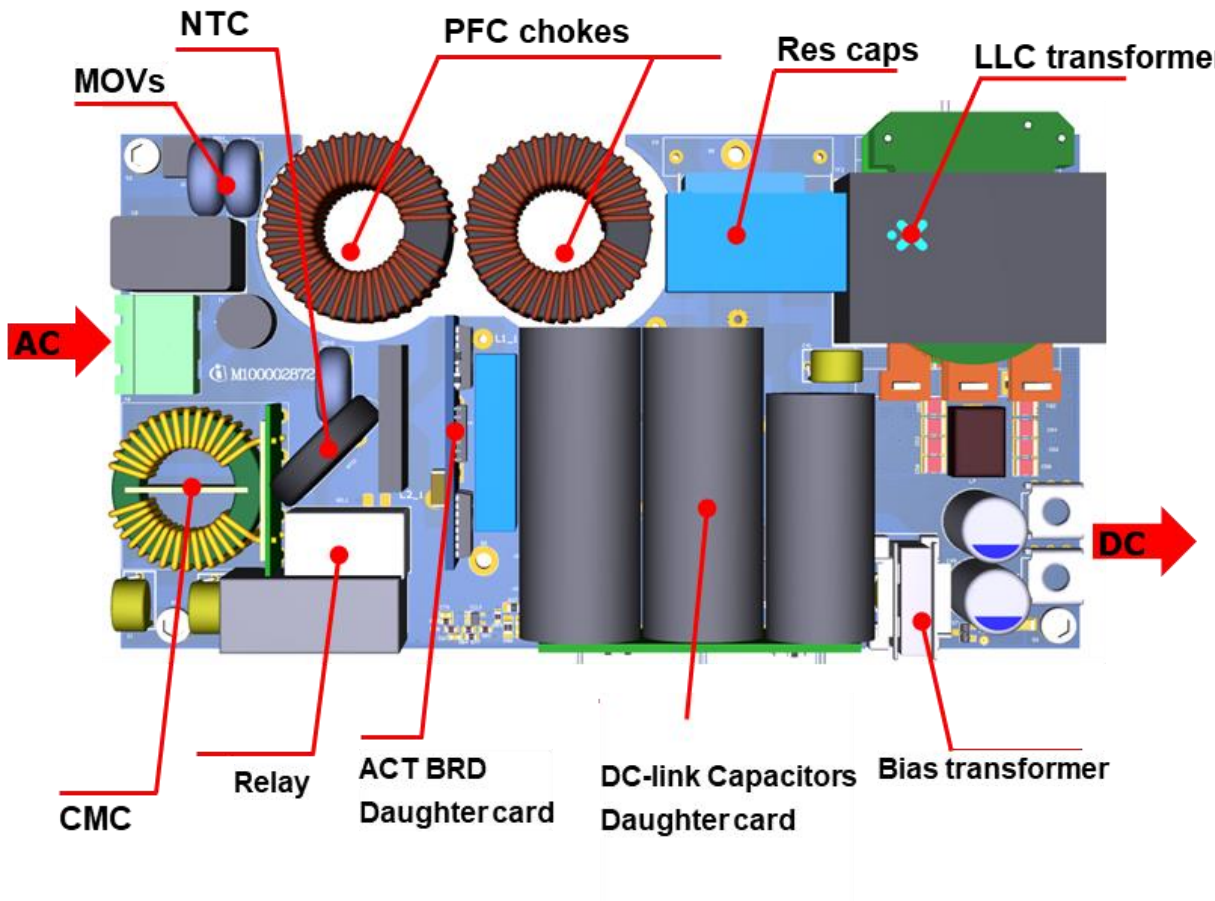
The control circuit of the standard boost PFC has been smartly adapted in order to operate the semi-bridgeless dual-boost topology properly. Furthermore, by just adding simple logic ports, the current-sensing effort has been reduced to only one shunt resistor (as shown in **Figure 7**), thus optimizing the occupied area on the PCB and solving the issue of the return current, described in **[2]**.

The PFC is operated in both high-line (230 V AC) and low-line (115 V AC) in continuous conduction mode (CCM) with 65 kHz of switching frequency. The bulk capacitance is designed to comply with the hold-up time shown in **Table 2**.

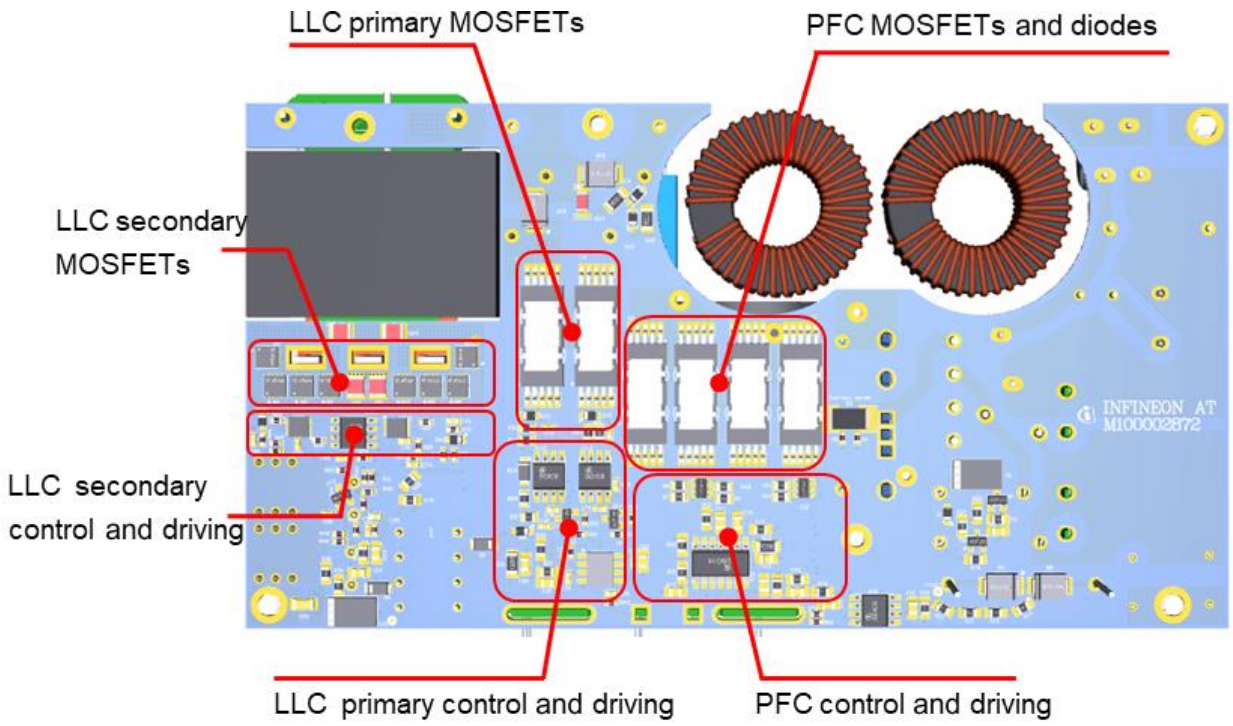
The control of the V DC LLC is implemented with the Infineon V DC resonant analog controller **ICE1HS01G**, which includes open-loop/overload protection with extended blanking time, two levels of OCP: frequency shift and latch off, mains input UVP with adjustable hysteresis, adjustable minimum switching frequency with high accuracy, built-in digital and non-linear soft-start, and burst-mode operation. Further details about the analog controller can be found in **[3]**.

Figure 8 shows the placement of the different sections of the **EVAL_500W_5G_PSU** telecom PSU with Infineon DDPAK semiconductors. The board shown is 150 mm long, with a width of 80 mm and a height of 27 mm.

Immediately after the AC input connector, the fuse and the NTC inrush current limiter are placed together with the input relay, and these are followed by a single-stage EMI filter. The active-line rectification is implemented in a daughter card with integrated controller, without the need for the bias supply voltage. The two PFC chokes are placed in a PCB cutout in order to thermally connect them to the metal baseplate with thermal interface material (TIM). The same concept has been used for the transformer located in the top-right side of the PSU. In the middle part of the board, the daughter card including the bulk capacitors is placed. Finally, all the main switches of both the PSU stages are placed in the bottom-side layer of the main PCB, as well as all controllers and drivers. The bias supply circuit is also implemented in the main board.



a)



b)

Figure 8 PSU implementation and component placement: view from a) top and b) bottom sides

2.1 Dual-boost PFC

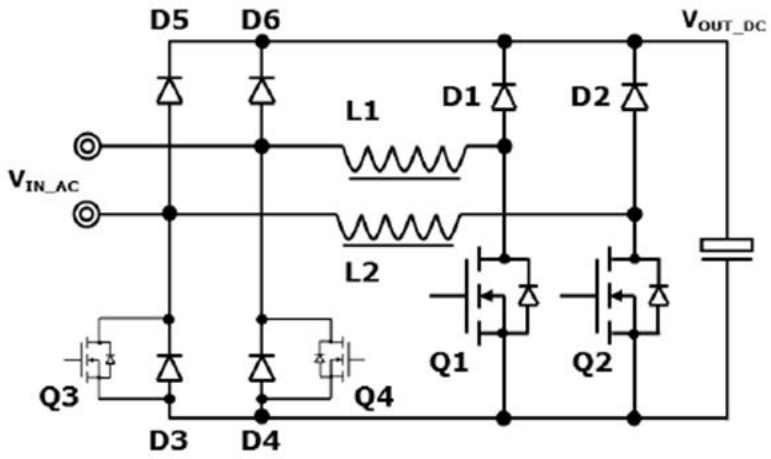


Figure 9 Bridgeless dual-boost PFC

The semi-bridgeless dual-boost topology (**Figure 9**) is a very attractive solution for power supply solutions for the following reasons:

- Compared to the standard/classic PFC rectifier based on a diode bridge (with two active diodes at all times), a single PFC MOSFET and a PFC diode, the dual-boost has lower conduction losses because there are always two power semiconductors (e.g., Q1 + D3 or Q2 + D4) in the current path per AC semi-cycle.
- There is less cooling effort and better heat spot distribution.
- It is more efficient and easier to control compared to an interleaved PFC rectifier, as this is a bridgeless topology with no need for phase shedding between the PFC legs.
- To increase the efficiency further, low $R_{DS(on)}$ MOSFETs (Q3 and Q4) can be placed in parallel with each of the returning path diodes (i.e., D3 and D4). As these MOSFETs will be conducting at the AC-line frequency, the switching losses and gate-driving losses are much lower than conduction ones. This benefit comes at the expense of increasing BOM count and cost, as well as accurate control and driving circuitry.

The estimated efficiency of the dual-boost PFC, part of the complete PSU, is plotted in **Figure 10**. It is worth noticing the very high peak efficiency, nearly 99 percent at 100 percent of the rated load and at high-line.

Benchmarking with a wide bandgap totem-pole has also been done, and this is included in the efficiency map in **Figure 10**. Small efficiency deviations can be seen for these power and switching frequency levels. The GaN totem pole gives the highest efficiency.

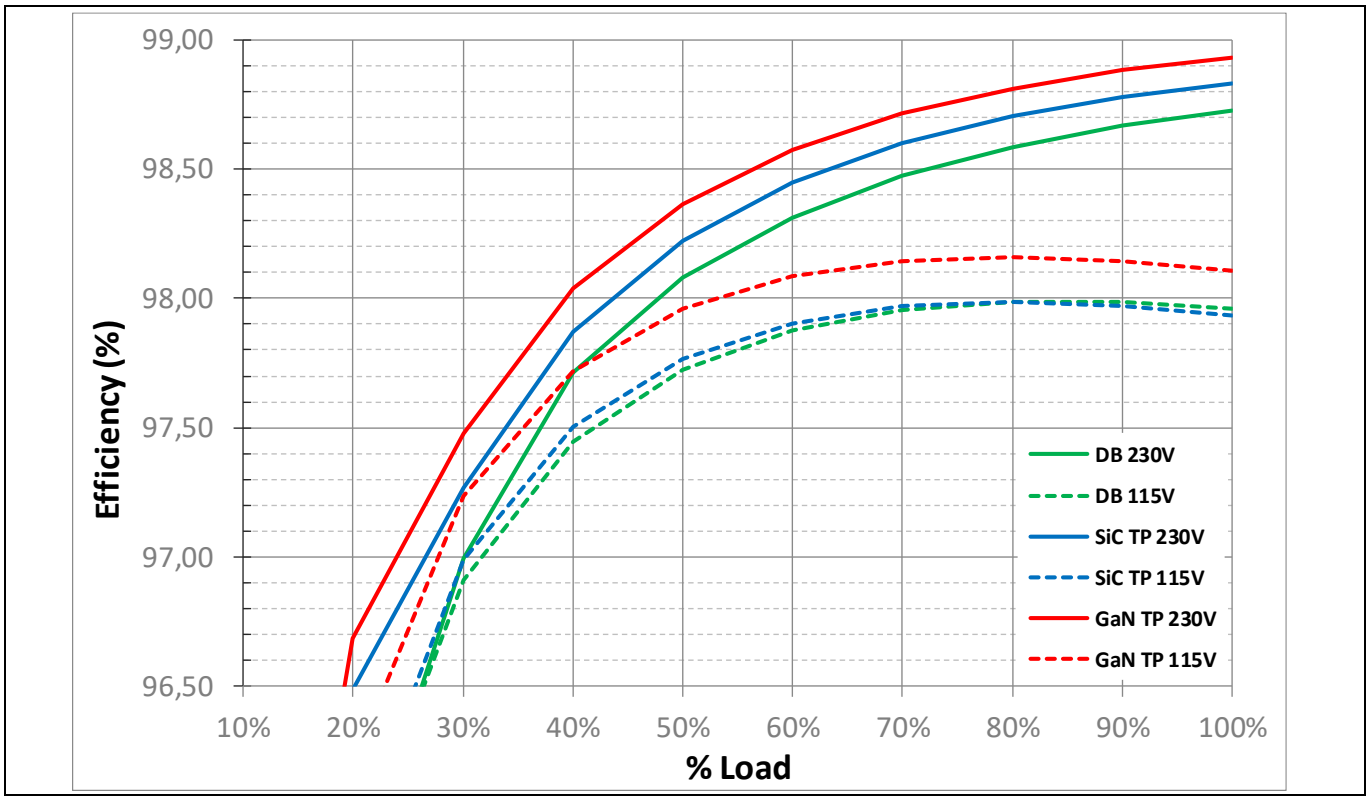


Figure 10 Estimated efficiency of the PFC (at 65 kHz of switching frequency)

The estimated overall distribution of MOSFET losses of the dual-boost PFC converter at both 230 V AC and 115 V AC and 100 percent of the rated load is summarized in **Figure 11**. It can be observed that the main contributors to the losses are the conduction and turn-on losses in the case of low-line input. At high-line, switching losses are dominant.

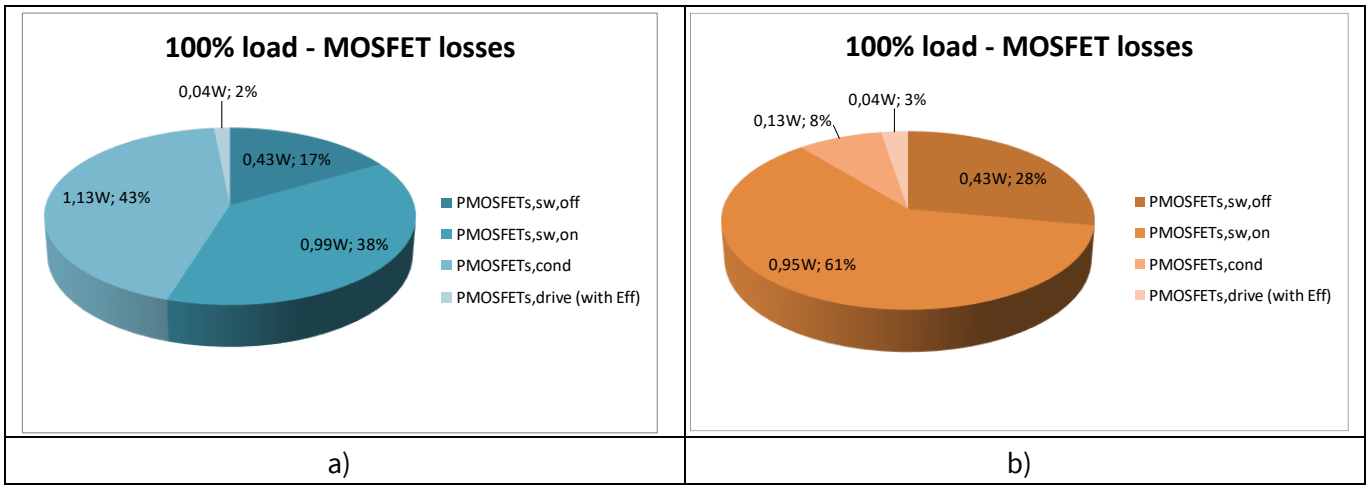


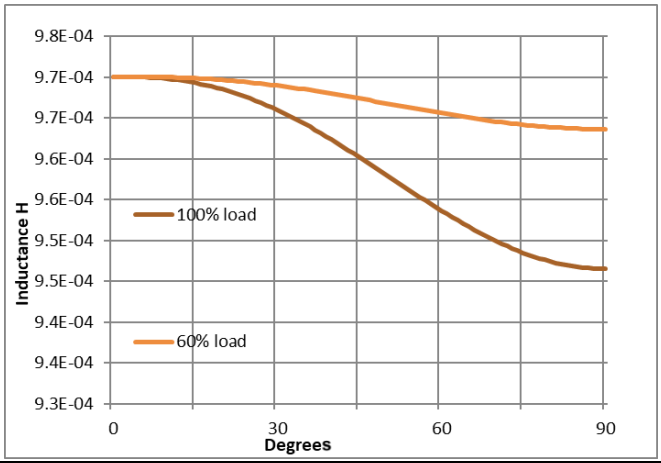
Figure 11 MOSFET breakdown losses for dual-boost PFC: a) at 115 V AC and b) at 230 V AC

2.1.1 PFC magnetics

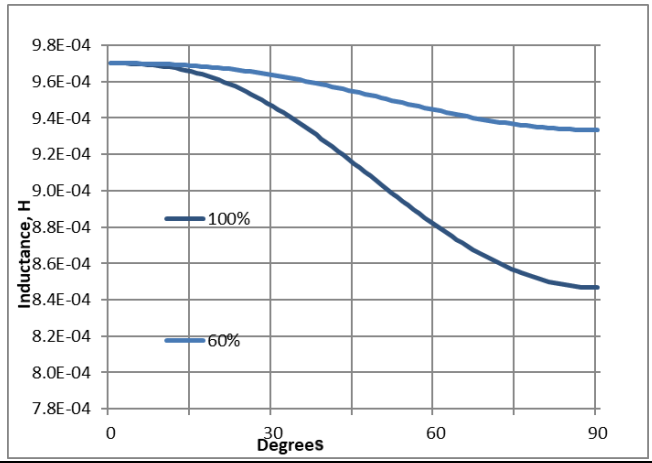
The other main contributors to the losses to consider in the design of the dual-boost AC-DC converter are the main inductor and the EMI filter. The PFC choke design is based on a toroidal high-performance magnetic powder core. Toroidal chokes have a large surface area and allow a good balance, minimizing core and winding losses, and achieving a homogeneous heat distribution without hot spots. For this reason they are suitable for systems that are targeting the highest power density; very small choke sizes are feasible. The chosen core

Figure 12 Image of PFC choke

material is High Flux from Chang Sung Corporation (CSC), which has an excellent DC bias and good core loss behavior. The part number is CH270060GTE18. The outer diameter of the core is 27 mm with a height of 19 mm. The winding was implemented using enameled AWG 18 (1.1 mm diameter) copper wire. The winding covers approximately two layers. This arrangement allows a good copper fill factor, while still having good AC characteristics, and is a preferred fill form factor for high-power toroidal inductors. There are 90 turns, taking advantage of the high permitted DC bias. The resulting small-signal bias inductance is 1 mH. The effective inductance with current bias is determined by the core material B-H characteristics, illustrated in **Figure 13**.



a) 230 V AC



b) 115 V AC

Figure 13 Angle of input current depending on the PFC choke inductance value

2.2 Half-bridge LLC

The estimated efficiency of the V DC LLC converter part of the complete PSU with 400 V input and 12 V output is plotted in **Figure 14**. It is worth mentioning the very high peak efficiency, nearly 97.5 percent at 60 percent of the rated load. Note that the overall efficiency of the complete PSU is the result of multiplying the separate efficiencies of the conforming blocks, and is necessarily lower than any of them separately. However, some of the loss contributions are shared between the two blocks (e.g., auxiliary bias) and therefore, the resulting overall efficiency is still expected to fall within the target specifications.

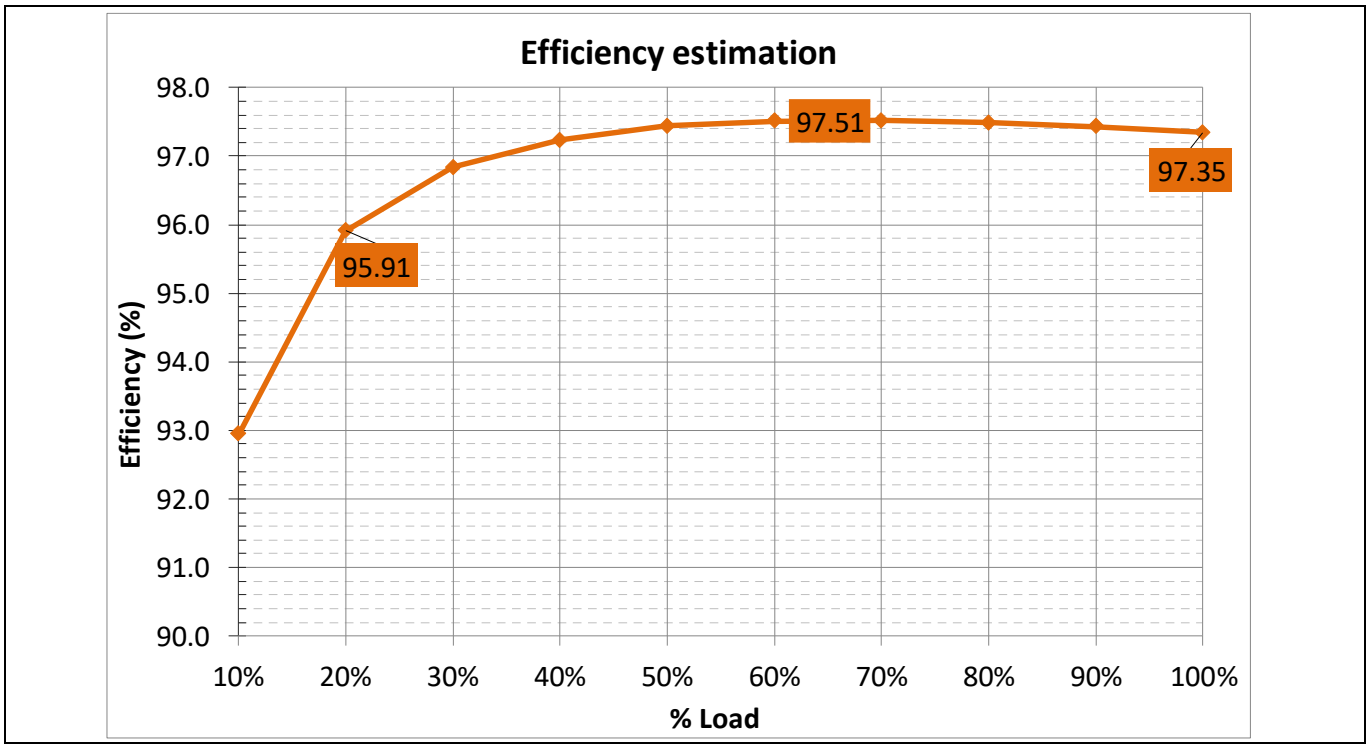


Figure 14 Estimated efficiency of the LLC DC-DC converter at 400 V DC input and 12 V DC output

2.2.1 LLC magnetics

The resonant tank of the V DC LLC series-parallel resonant converter comprises two equivalent inductors and one equivalent capacitor (hence its name).

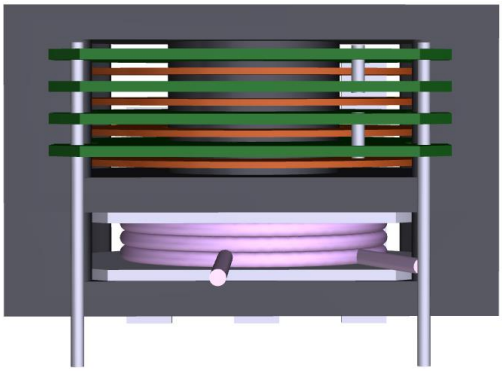
One of the advantages of this topology is that it is possible to realize the series resonant inductor (L_r) by the leakage of the main transformer, and the parallel resonant inductor (L_m) by the magnetizing inductance of the main transformer.

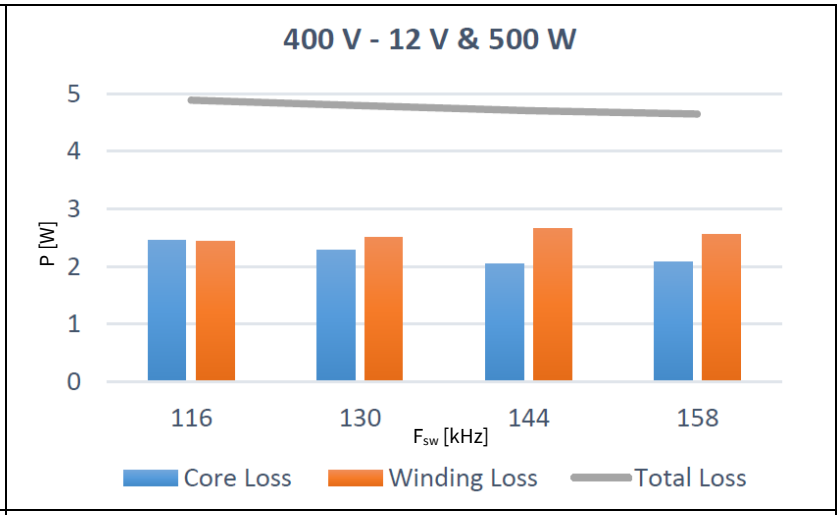
Nevertheless, the full integration approach constrains the design and compromises the performance of the converter. Therefore, in the PSU the series inductor (L_r) has been realized as discrete components, although L_r is integrated within the same magnetic structure of the main transformer.

Figure 15a shows a simplified view of the construction of the resonant inductor (L_r) and the main transformer. The resonant inductor is built with a 3C95 PQ38/8/25 core from Ferroxcube, while the main transformer is built with two cores of the same material. The L_r is stacked on the bottom of the main transformer and wound in the same direction as the primary-side winding. As a result of this, the flux in part of the volume is effectively canceled and the total core loss is partly reduced. The windings of the transformer are made with four PCBs for the primary and with four Cu stamps for the secondary. The secondaries are arranged in a center-tapped mode. The winding of L_r is made of six turns of Litz wire with 225 strands of 0.05 mm diameter (with total diameter of 1.19 mm).

In **Figure 15b** the estimated losses of the overall magnetic structure have been reported as a function of the switching frequency of the LLC converter. Note that at 116 kHz the balance between core and winding losses is almost equal with a total amount of losses around 5 W. By increasing the switching frequency, the copper losses became more dominant, even though the total amount of loss is slightly reducing.

For the final demonstration, the resonance frequency of the LLC has been fixed at around 85 kHz, resulting in a switching frequency of around 100 kHz at full load and around 120 kHz at half-load.





a) b)

Figure 15 Integrated transformer: a) planar structure and b) losses at different switching frequencies

Due to the height limitation of the PSU (27 mm) the main board needs to be cut out to accommodate the height of the integrated L_r plus the main transformer structure (approximately 25 mm). Thermal connection of the magnetic core with the aluminum baseplate is done with a 2 mm TIM.

The assembled structure is shown in **Figure 16**.

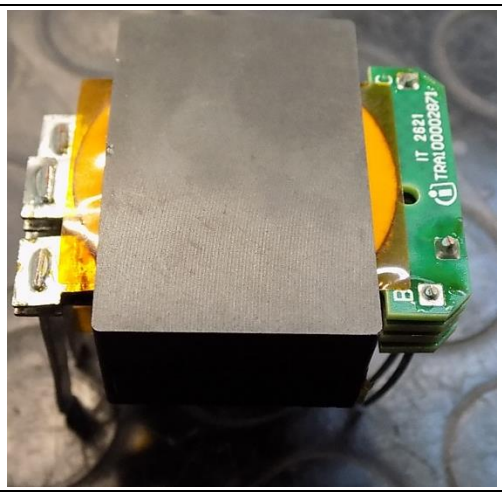


Figure 16 Photo of the assembled integrated structure of the transformer plus the parallel resonant inductor

3 Experimental results

This section is a summary of the main experimental results of each of the conforming blocks separately (semi-bridgeless dual-boost PFC and V DC LLC), and of the complete PSU.

3.1 Dual-boost PFC

3.1.1 Steady-state operation

The main steady-state waveforms of the PFC are presented for both low-line 115 V AC (**Figure 17**) and high-line 230 V AC (**Figure 18**) at nominal load conditions. As it can be seen, each PFC choke is conductive during only half of the line cycle (Ch2 and Ch3). Input current is purely sinusoidal (Ch1), and the bulk voltage is stable at 400 V (Ch6). No issue of returning current is experienced with the actual demonstrator for all load conditions. In addition, input voltage and the V_{DS} across one of the two PFC MOSFETs are also reported in Ch4 and Ch5, respectively. PFC is almost always working in CCM.

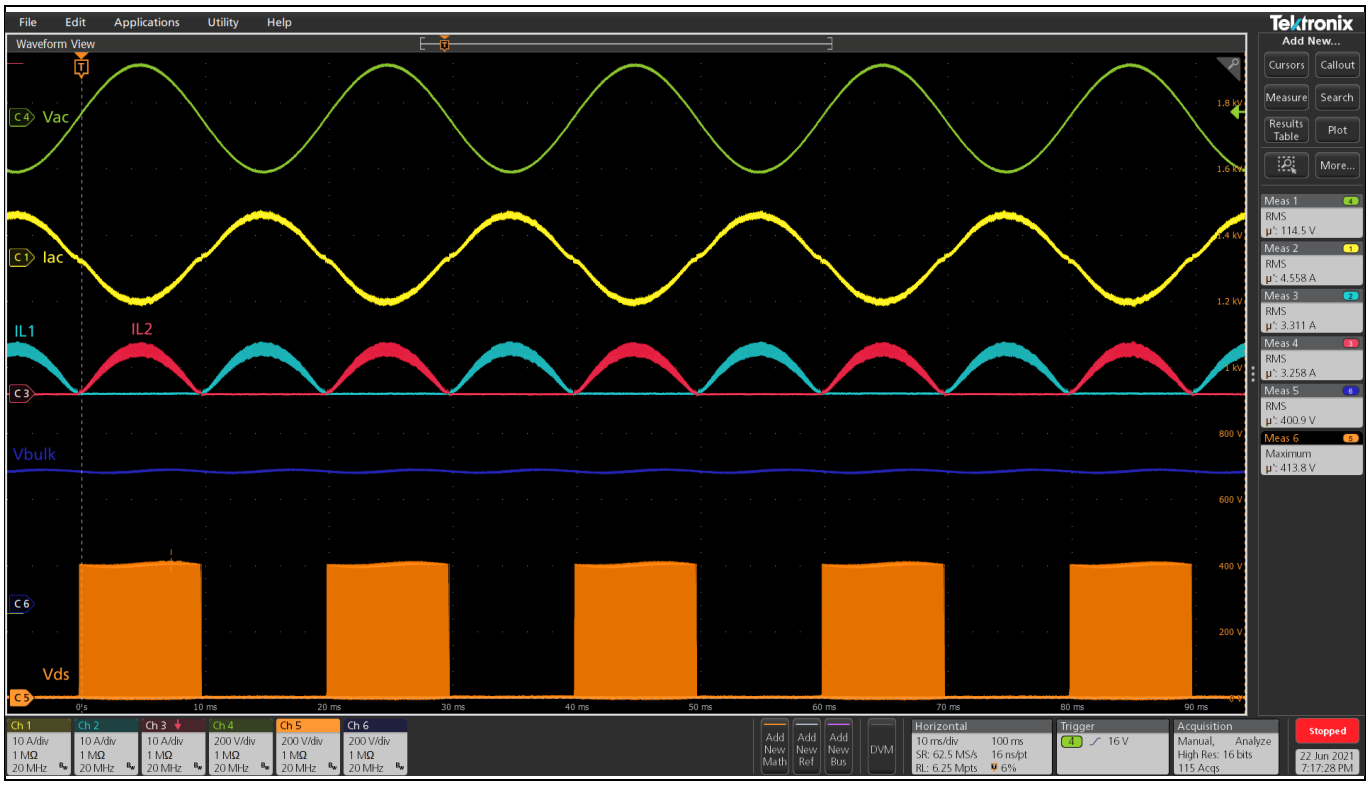


Figure 17 PFC steady-state waveforms at 115 V AC and at full load

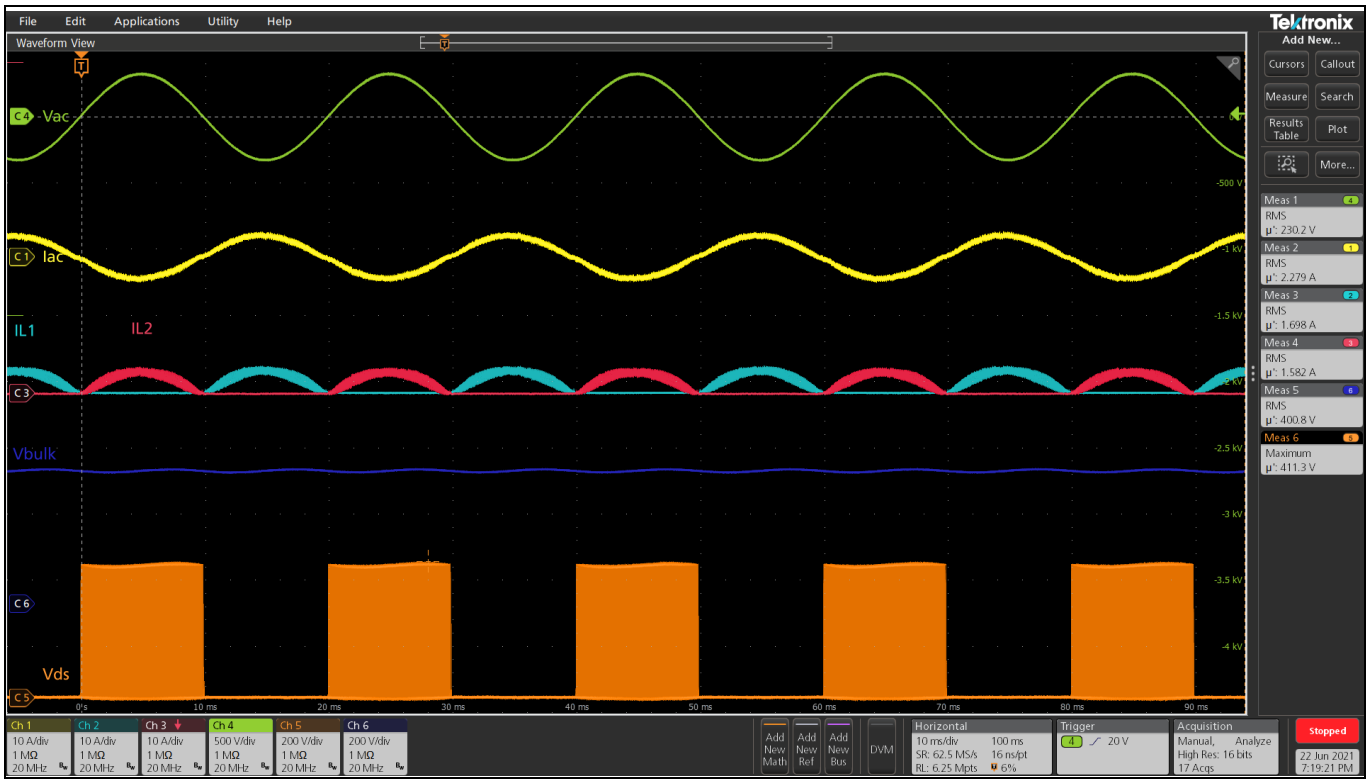


Figure 18 PFC steady-state waveforms at 230 V AC and at full load

3.1.2 Active-line rectification

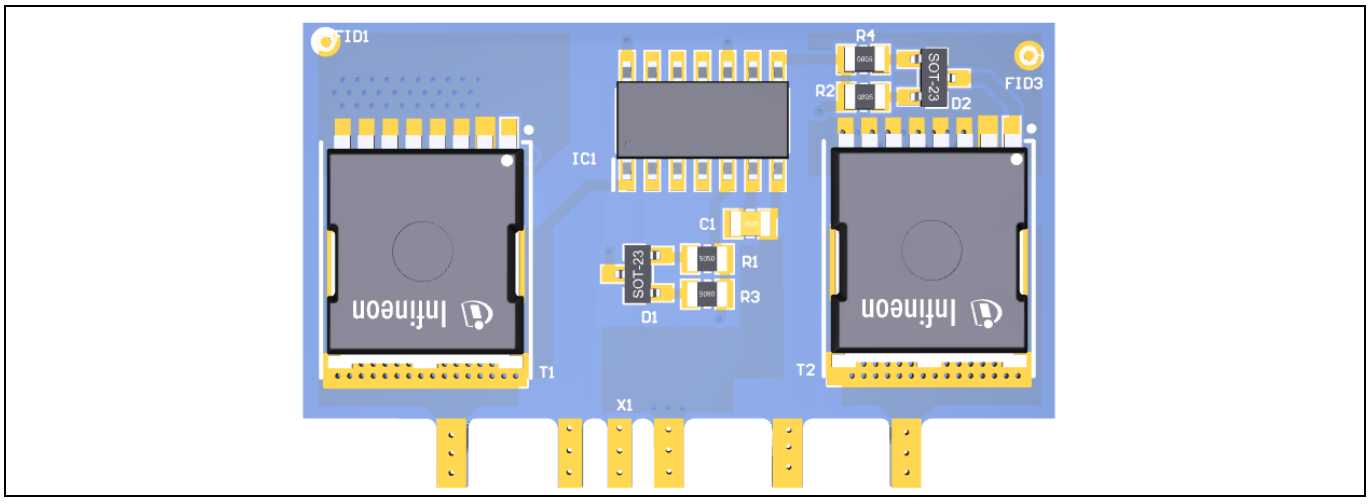


Figure 19 Daughter card for PFC active-line rectification

In order to boost the efficiency of the topology, active rectification MOSFETs Q3 and Q4 are added, as previously shown in **Figure 9**.

The active rectification is implemented with an additional daughter card PCB with two 22 mΩ CoolMOS™ S7s connected to the main board and placed in a vertical positon. The active bridge MOSFETs are controlled thanks to an integrated driver/controller with self-bias cell, as shown in **Figure 19**. The daughter card has a total height of 20 mm, with all SMD components in one layer.

3.1.3 PFC efficiency

The efficiency of the only PFC stage was measured at ambient temperature after running the converter for 30 minutes at full load in order to reach steady-state temperature of the chokes. Efficiency results at both low- and high-line are shown in **Figure 20**.

Note that at 230 V AC the efficiency reaches an outstanding peak of almost 99 percent near 500 W of output power. The PFC is cable of working even up to 1 kW at high-line with a quite flat efficiency shape, as shown in **Figure 20**. At 115 V AC the efficiency has a peak of 98.3 percent at around 250 W, while at full load (500 W) the efficiency drops to aroud 98 percent.

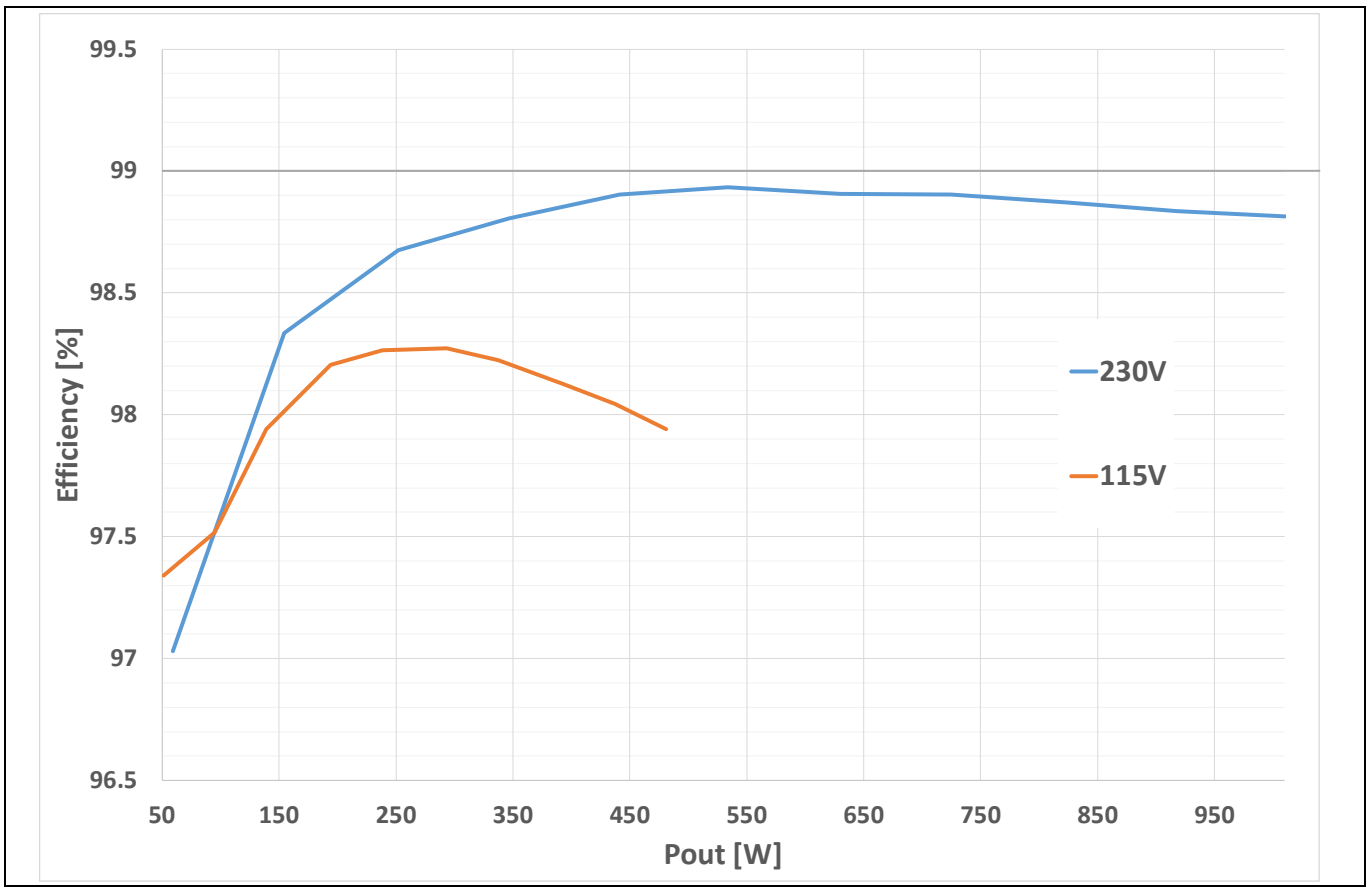


Figure 20 Measured PFC efficiency

3.2 Half-bridge LLC

The V DC LLC can achieve zero-voltage-switching (ZVS) turn-on in the primary-side V DC along all the load range. On the other hand, the turn-off is hard-switched. However, if the dv/dt is not limited by the device during the resonant transition, the turn-off transition becomes lossless.

3.2.1 Steady-state operation

The main steady-state waveforms of the LLC are presented for both 100 percent load (**Figure 21**) and 50 percent load (**Figure 22**) at nominal input/output voltages. Figures show the following waveforms: load current (Ch1), resonant current (Ch2), output voltage (Ch3), secondary MOSFETs drain-to-source voltages (Ch4 and Ch5), and secondary MOSFETs gate-to-source voltage (Ch6). As can be seen, output voltage is kept stable at 12 V. The LLC works above resonant frequency and OptiMOS™ drain voltage spikes are below 28 V, thus enabling use of 40 V MOSFETs.

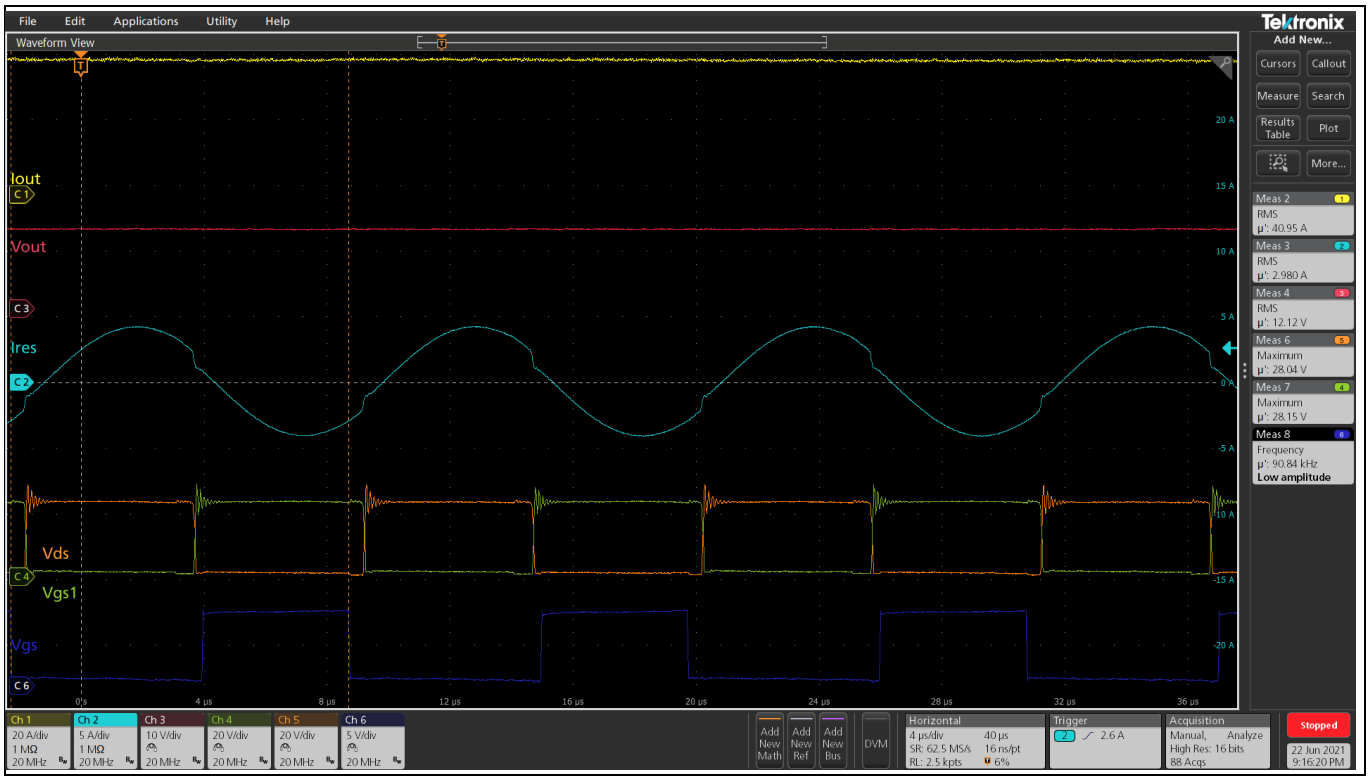


Figure 21 Steady-state operation at 100 percent of the rated load and at 400 V input voltage

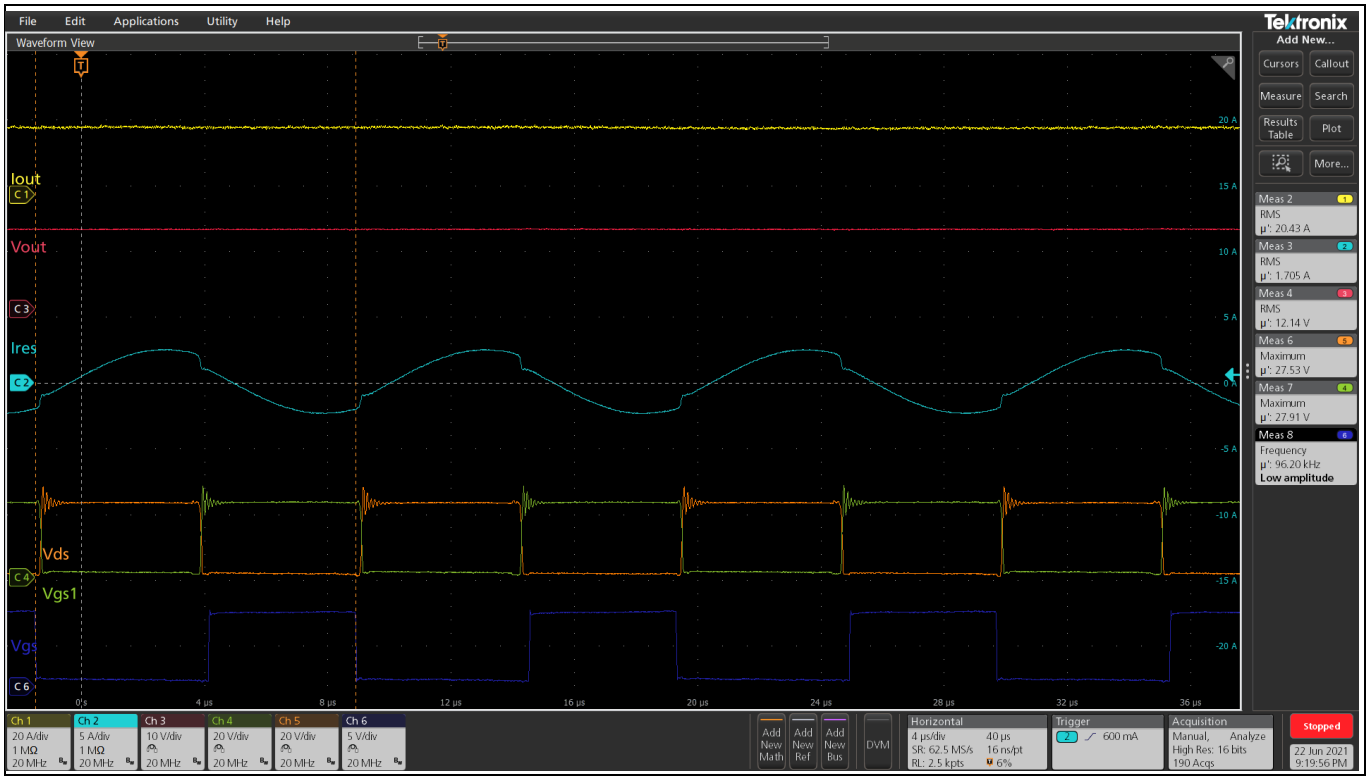


Figure 22 Steady-state operation at 50 percent of the rated load and at 400 V input voltage

3.2.2 LLC efficiency

The efficiency of the only LLC stage has been measured at ambient temperature after running the converter for 15 minutes at full load in order to reach steady-state temperature of the integrated transformer. In **Figure 23**, efficiency results are presented, comparing two different arrangements of the secondary-side windings of the LLC transformer in **Figure 16**. One transformer has the secondary windings interleaved, the other one does not.

The LLC efficiency reaches an outstanding peak of almost 97.3 percent near 380 W of output power in the case of non-interleaved secondary windings. On the other hand, if interleaving is applied, the efficiency peak is lower (almost 97.2 percent) and it is reached at higher power (around 420 W). For both winding arrangements, the efficiency at full load is close to 97.1 percent. Furthemore, the efficiency is above 97 percent above 50 percent of the output load.

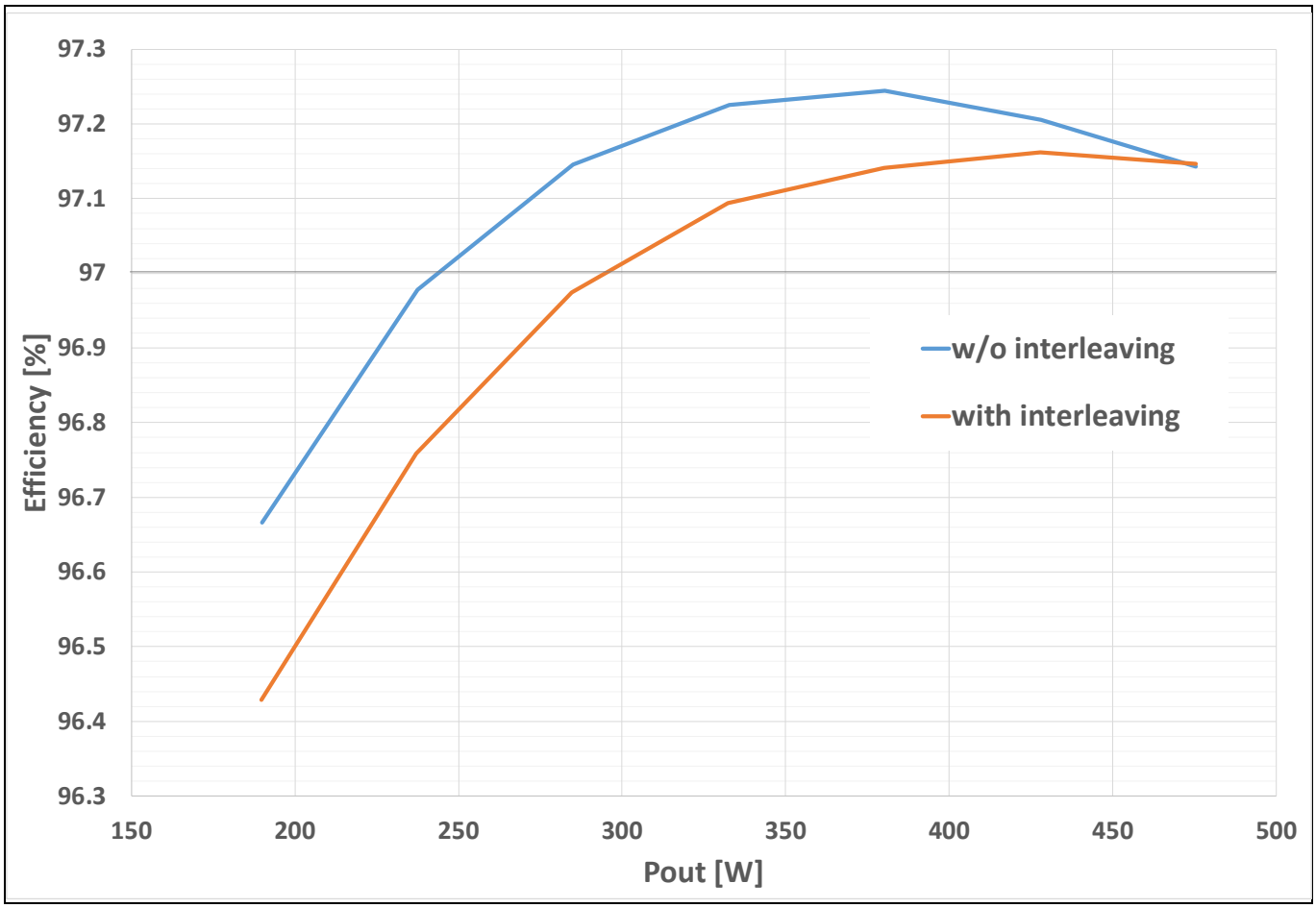


Figure 23 Measured LLC efficiency at 400 V input and 12 V output

3.3 Full power supply unit

This section provides a summary of experimental results of the complete power supply.

3.3.1 Efficiency

The efficiency of the complete power supply was measured after running the converter for 30 minutes at full load. The baseplate was pre-heated with a constant temperature of 40°C to emulate a standard working condition. The synchronous rectification MOSFETs were connected to the baseplate through a soft thermal interface.

Figure 24 presents the efficiency results for 230 V AC input and 12 V DC output.

At high-line input voltage, the **EVAL_500W_5G_PSU** reaches an outstanding peak of almost 96.5 percent near 420 W. The PSU is fully compliant with the initial specification (red dashed curve in **Figure 24**). Futhermore, the efficiency is above 96 percent from around 45 percent of the load up to full load.

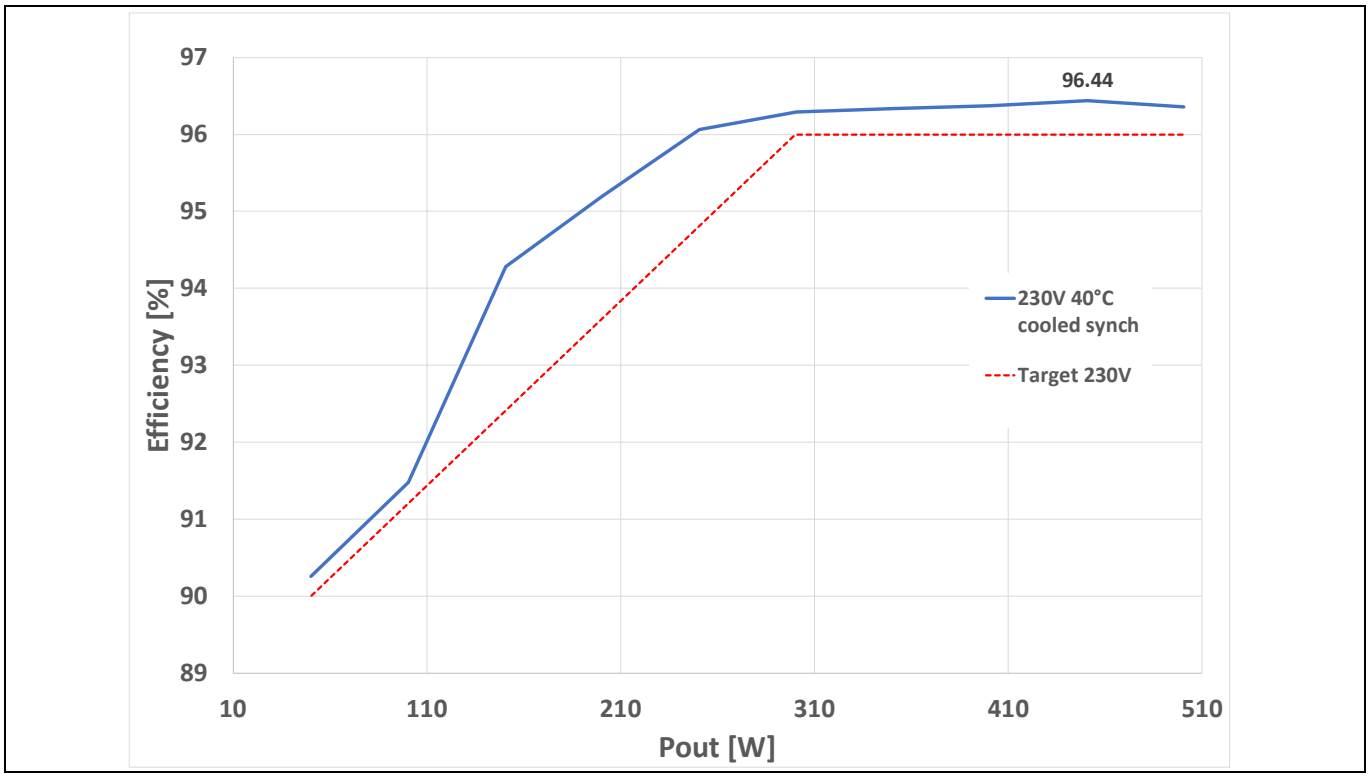


Figure 24 Measured efficiency of the complete PSU at 230 V AC

Figure 25 presents the efficiency results for 115 V AC input and 12 V DC output.

At low-line input voltage, the **EVAL_500W_5G_PSU** reaches an outstanding peak of almost 95.6 percent near 300 W. The PSU is fully compliant with the initial specification (red dashed curve in **Figure 25**). Futhermore, the efficiency is above 95 percent from around 45 percent of the load up to full load.

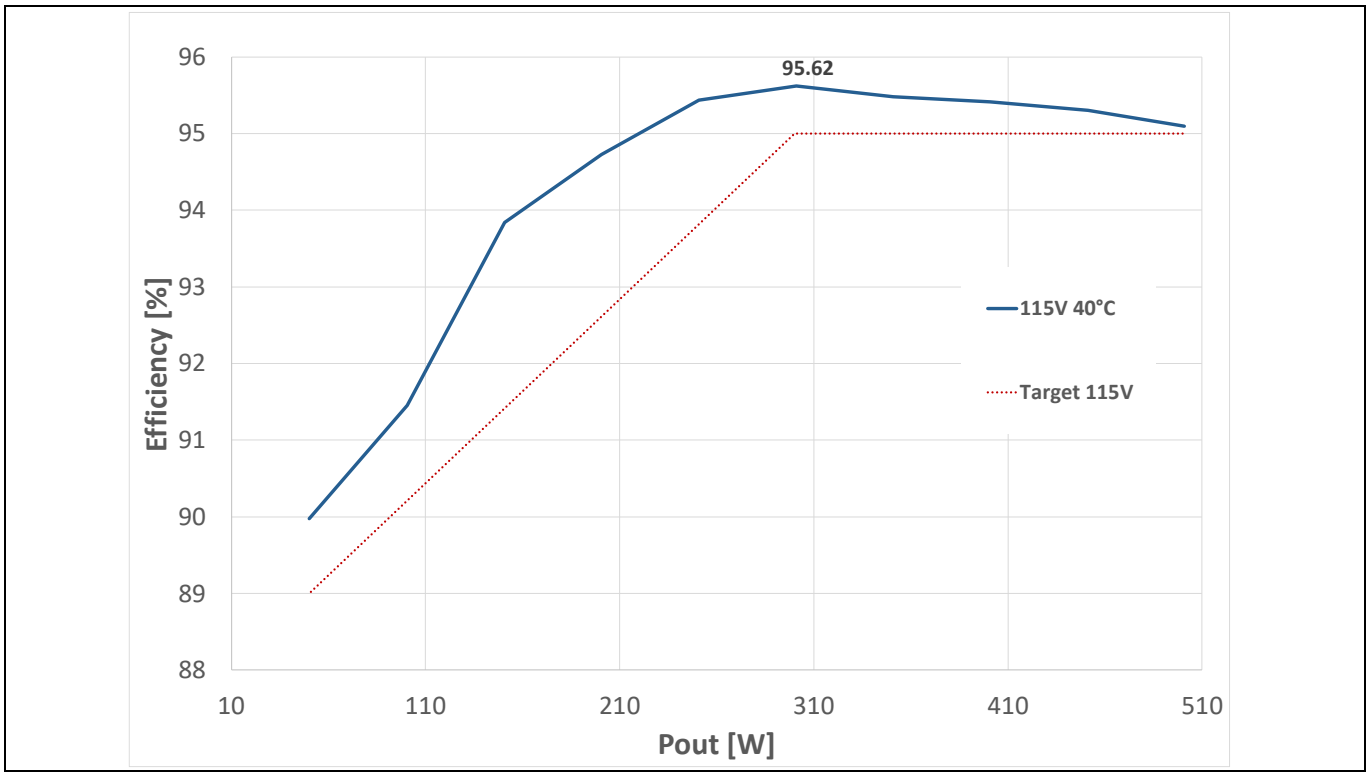


Figure 25 Measured efficiency of the complete PSU at 115 V AC

3.3.2 Start-up

Figure 26, **Figure 27** and **Figure 28** present the PSU start-up sequence at 85 V AC, 260 V AC and 305 V AC, respectively.

Figures show the following waveforms: PFC input current (Ch1), LLC resonant current (Ch2), PFC bulk voltage (Ch3), PFC input voltage (Ch4), LLC low-side MOSFETs drain-to-source voltage (Ch5), PFC MOSFETs drain-to-source voltage (Ch6).

As shown in **Figure 26**, at 85 V AC (minimum operating voltage), V_{DS} peak is 428 V for the PFC MOSFET and 417 V for the LLC MOSFET. The bulk voltage's maximum value is 413 V during start-up from the rectified voltage to the target 400 V value. The input current has a peak of 14 A.

As shown in **Figure 27**, at 260 V AC, V_{DS} peak is 418 V for the PFC MOSFET and 411 V for the LLC MOSFET. The bulk voltage's maximum value is 407 V during start-up from the rectified voltage to the target 400 V value. The input current has a peak of 10 A. From **Figure 27** the pre-charge of the bulk before PFC start-up and the subsequent starting of LLC operation can also be seen.

Figure 28 shows PSU start-up when the AC voltage is at the maximum 305 V AC. The PSU can still operate in this condition, but the power factor cannot be guaranted, because the rectified peak voltage is higher than the target bulk voltage. The PFC is not able to boost in some conditions, and behaves as a passive rectifier. Higher ripple is experienced in the bulk voltage, with effects on the resonant current of the LLC that is trying to compensate it.

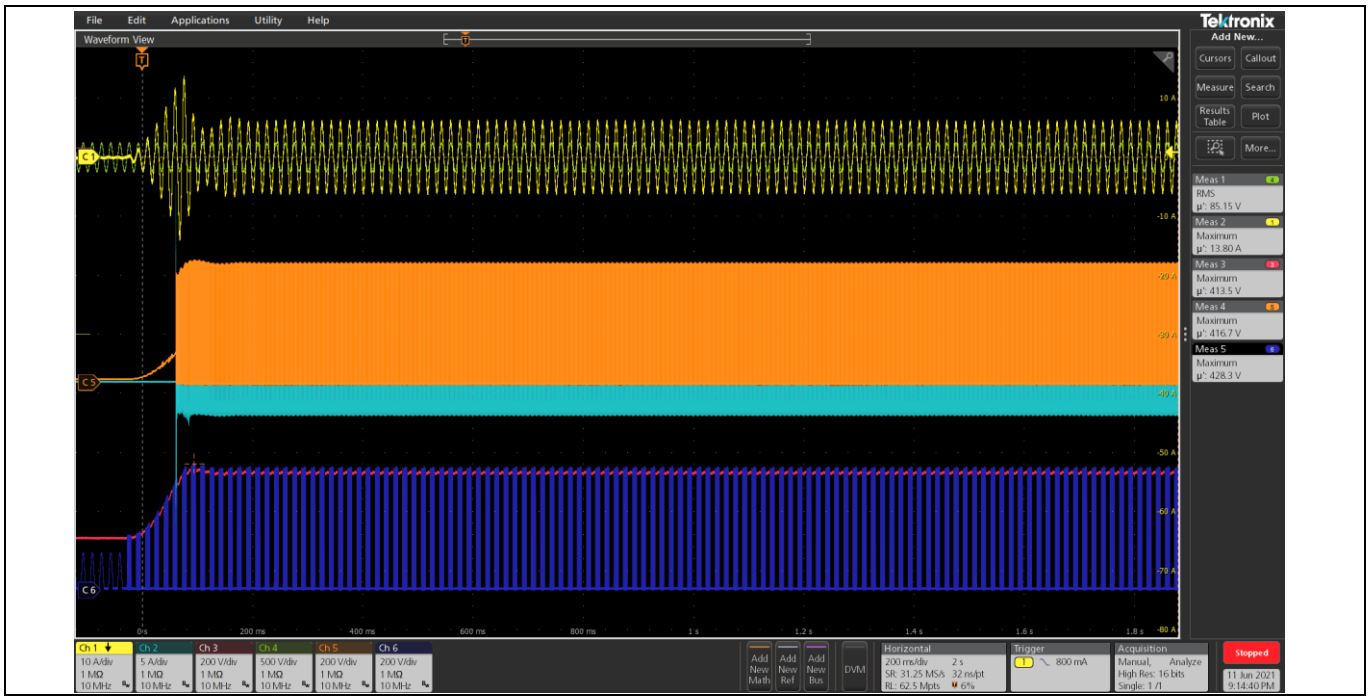


Figure 26 Start-up sequence of the full PSU at full load at 85 V AC

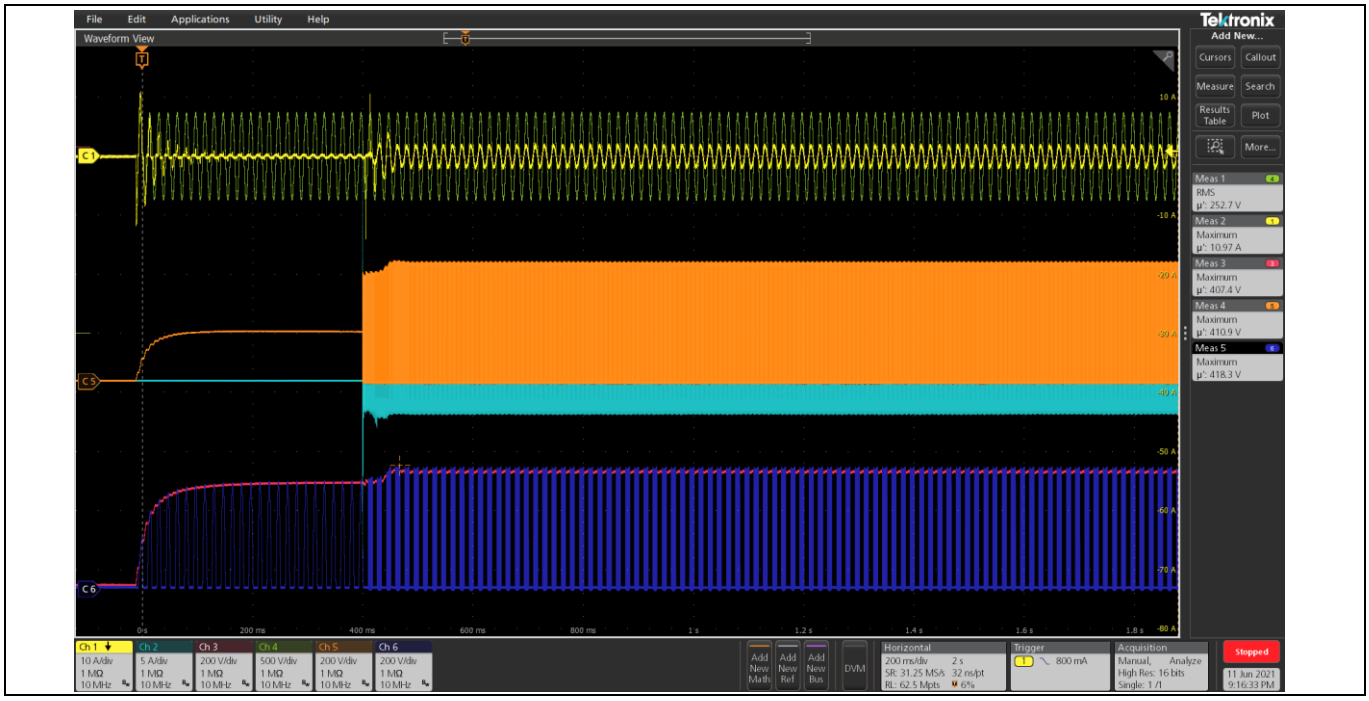


Figure 27 Start-up sequence of the full PSU at full load at 260 V AC

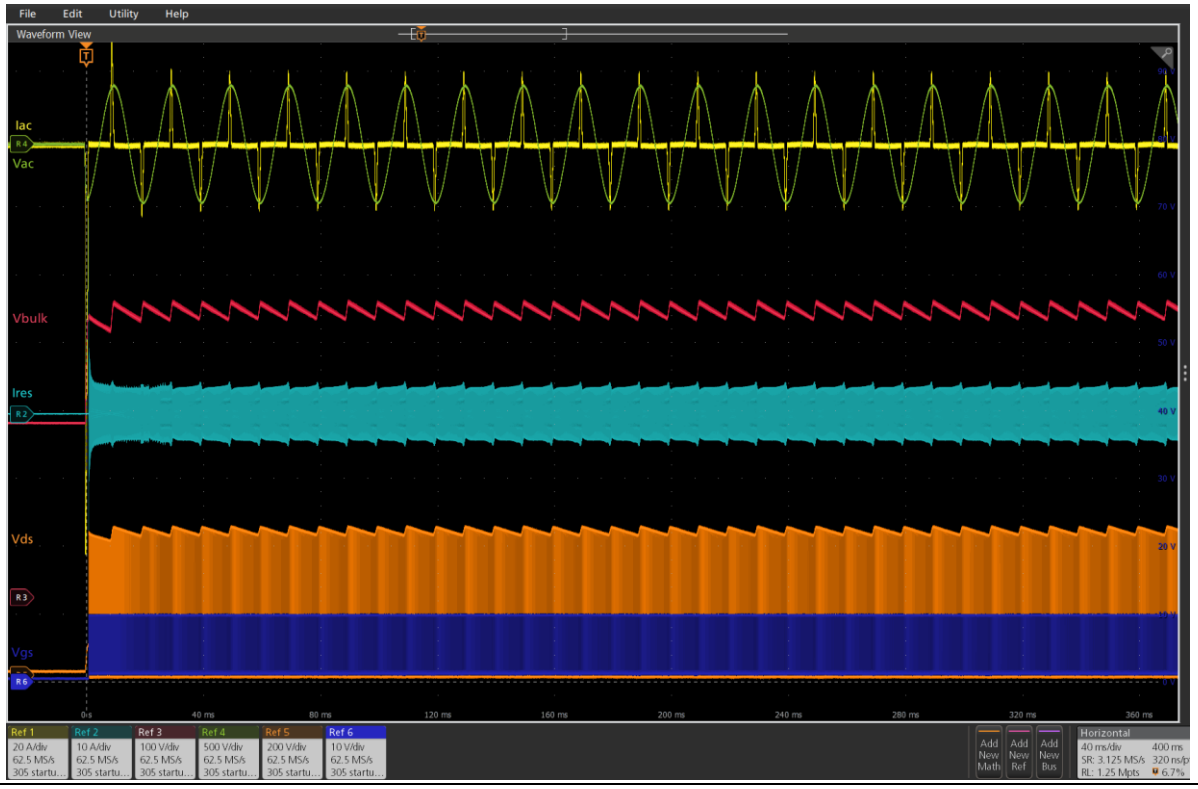


Figure 28 Start-up sequence of the full PSU at full load at 305 V AC

3.3.3 Power factor and THD

The power factor (PF) and THD have been measured at both low- and high-line V AC, as shown in **Figure 29**.

The PF is higher than 0.9 from 18 percent of the load at 230 V AC, and always above 0.98 at 115 V AC.

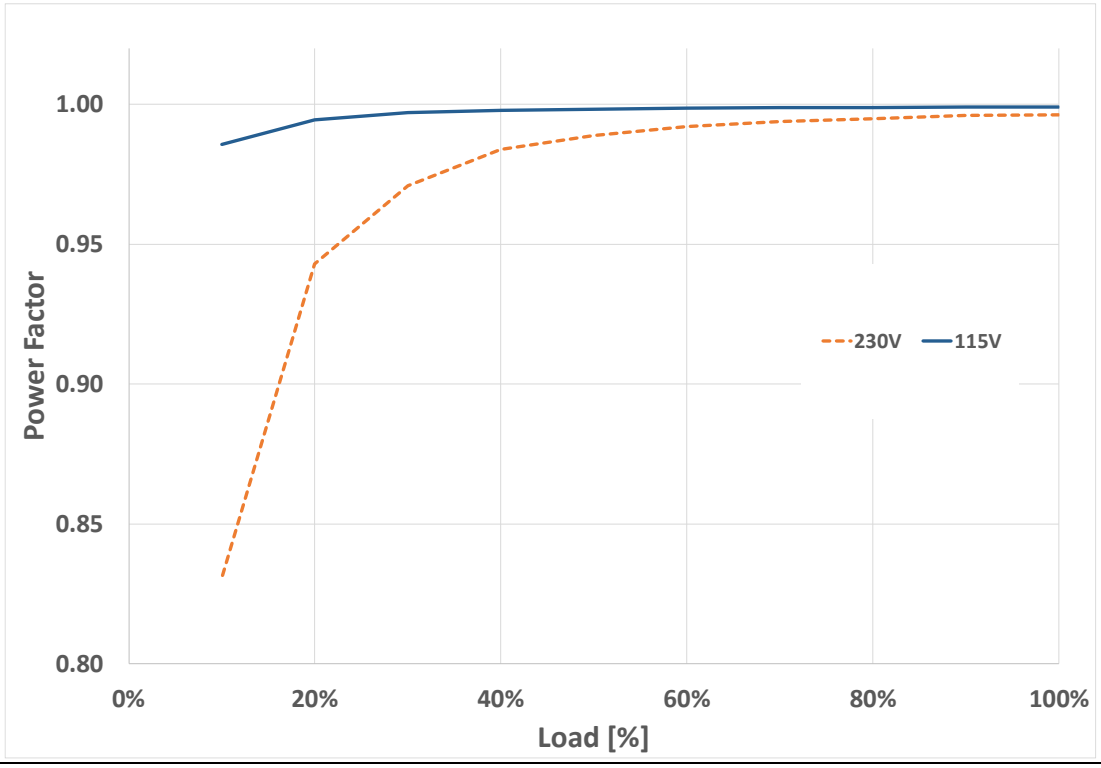


Figure 29 Measured PF of the complete power supply prototype

3.3.4 Output voltage ripple

At the output of the designed LLC converter there is an additional inductor that forms a CLC filter, which helps reduce the output voltage ripple of the converter, as well as the common-mode noise injected into the output.

The high-frequency ripple is within 230 mV peak-to-peak in steady-state and at full load (**Figure 30**).

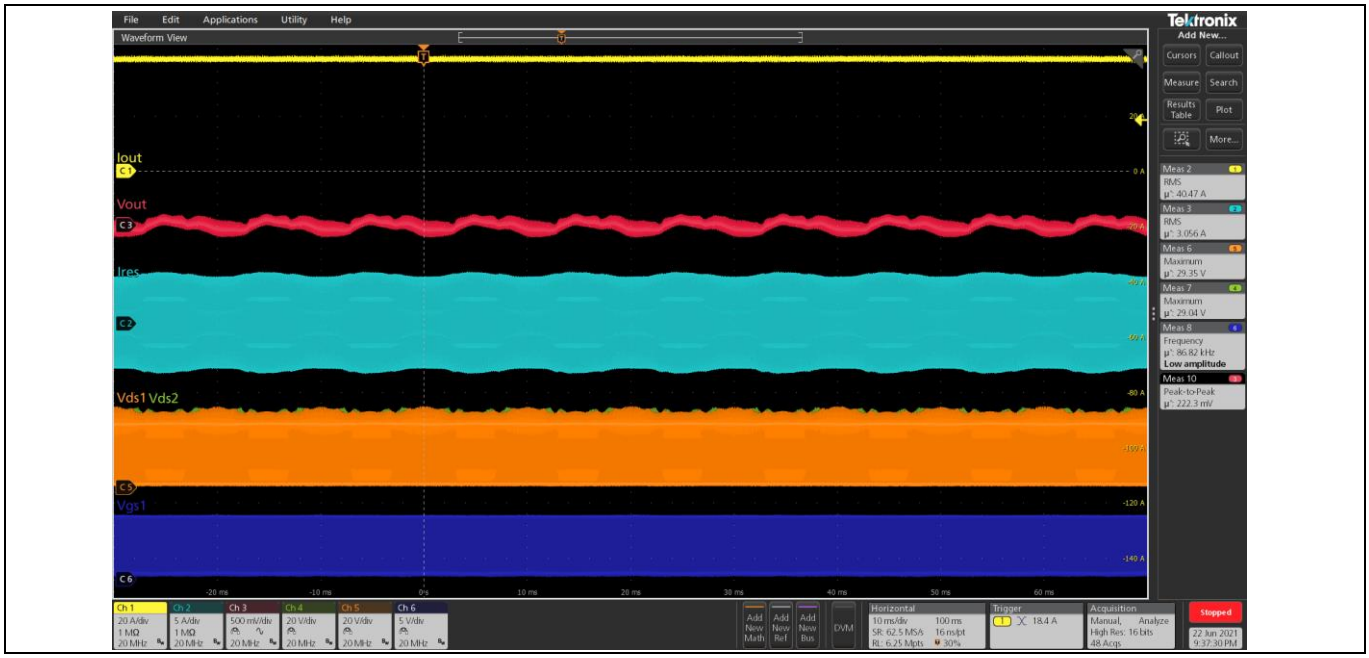


Figure 30 Output voltage ripple at full load

The high-frequency ripple is within 150 mV peak-to-peak in steady-state and at 40 percent load (**Figure 31**).

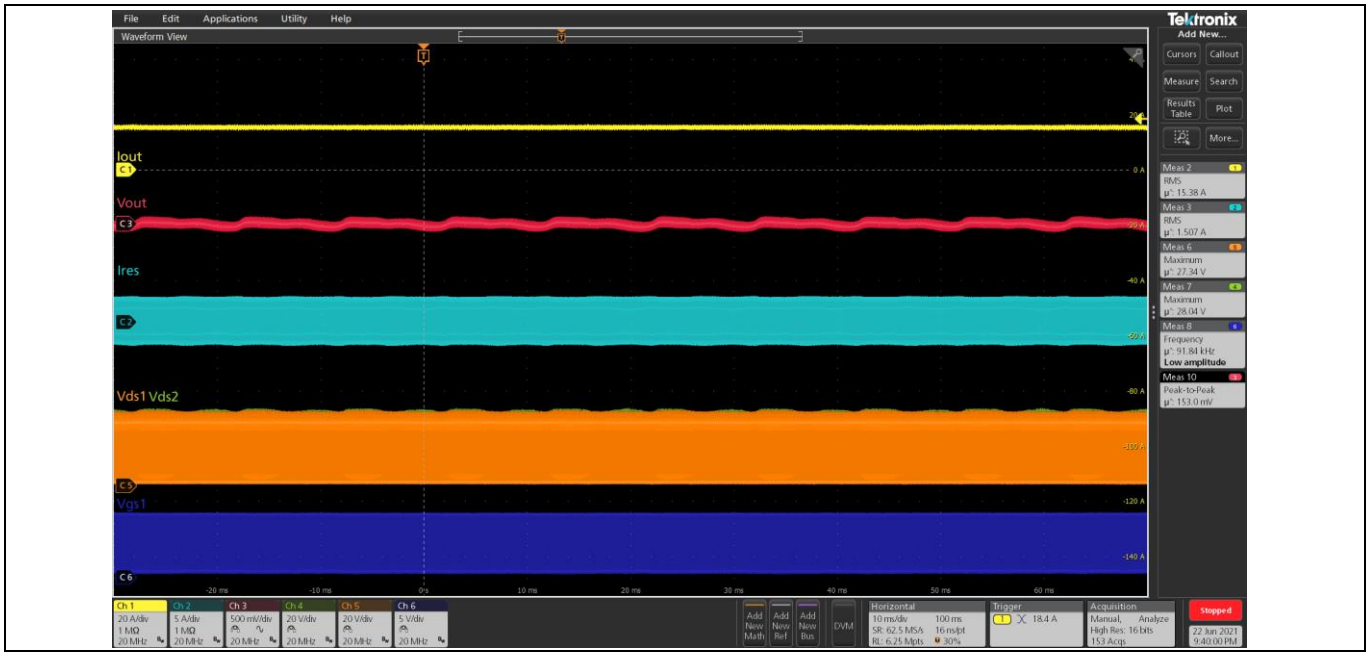


Figure 31 Output voltage ripple at 40 percent load

3.3.5 Hold-up time

The PSU specification requires up to 20 ms hold-up time at 80 percent of the full power, although the output voltage of the PSU is allowed to drop down to 10.8 V DC.

Figure 32 shows a capture of the dual-boost PFC response and the output voltage of the PSU during a 20 ms hold-up time at 80 percent load, repeatedly. Bulk voltage drops to a minimum value of around 340 V DC and the output voltage has a peak-to-peak variation of 1.2 V DC, thus complying with the specification.

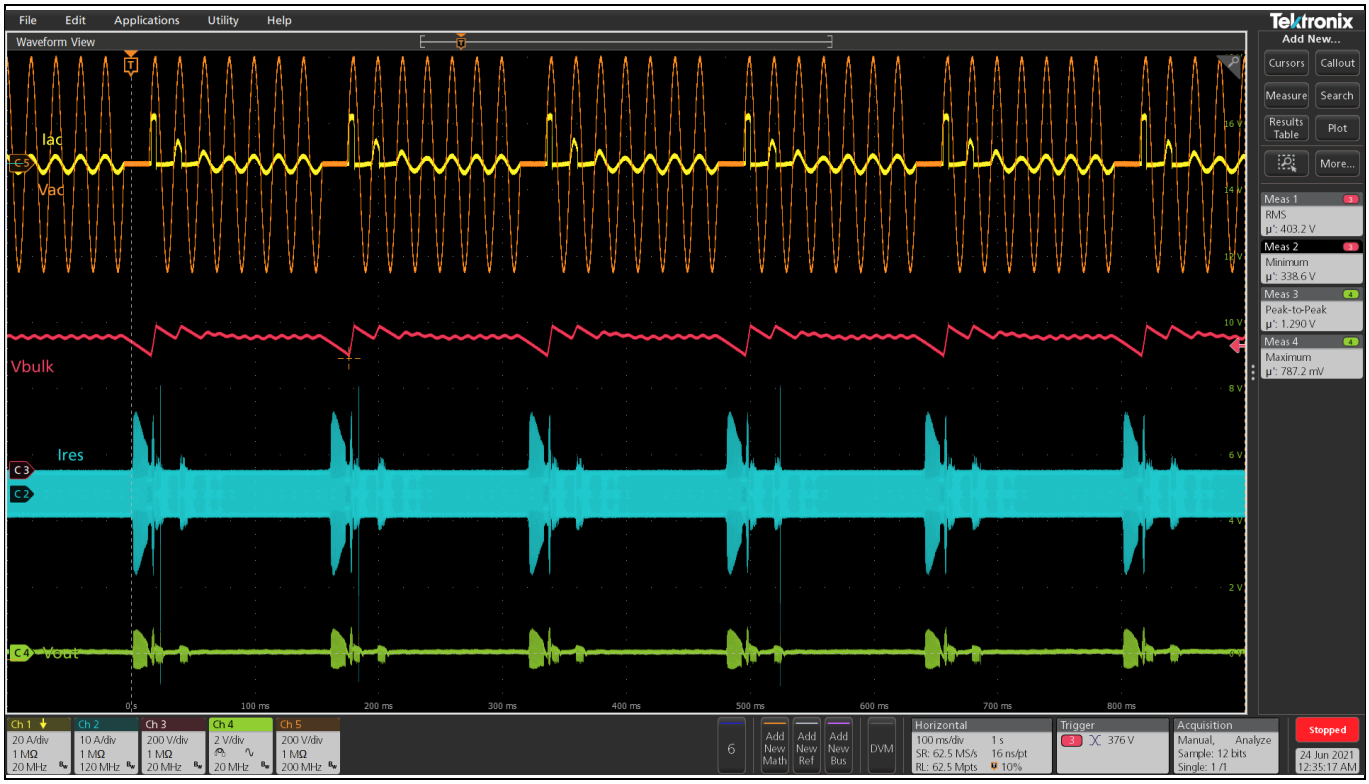


Figure 32 20 ms hold-up time at 80 percent load and 230 V AC

Meanwhile **Figure 33** shows a capture of the response of the dual-boost PFC and the LLC during a 10 ms hold-up time at full power, repeatedly.

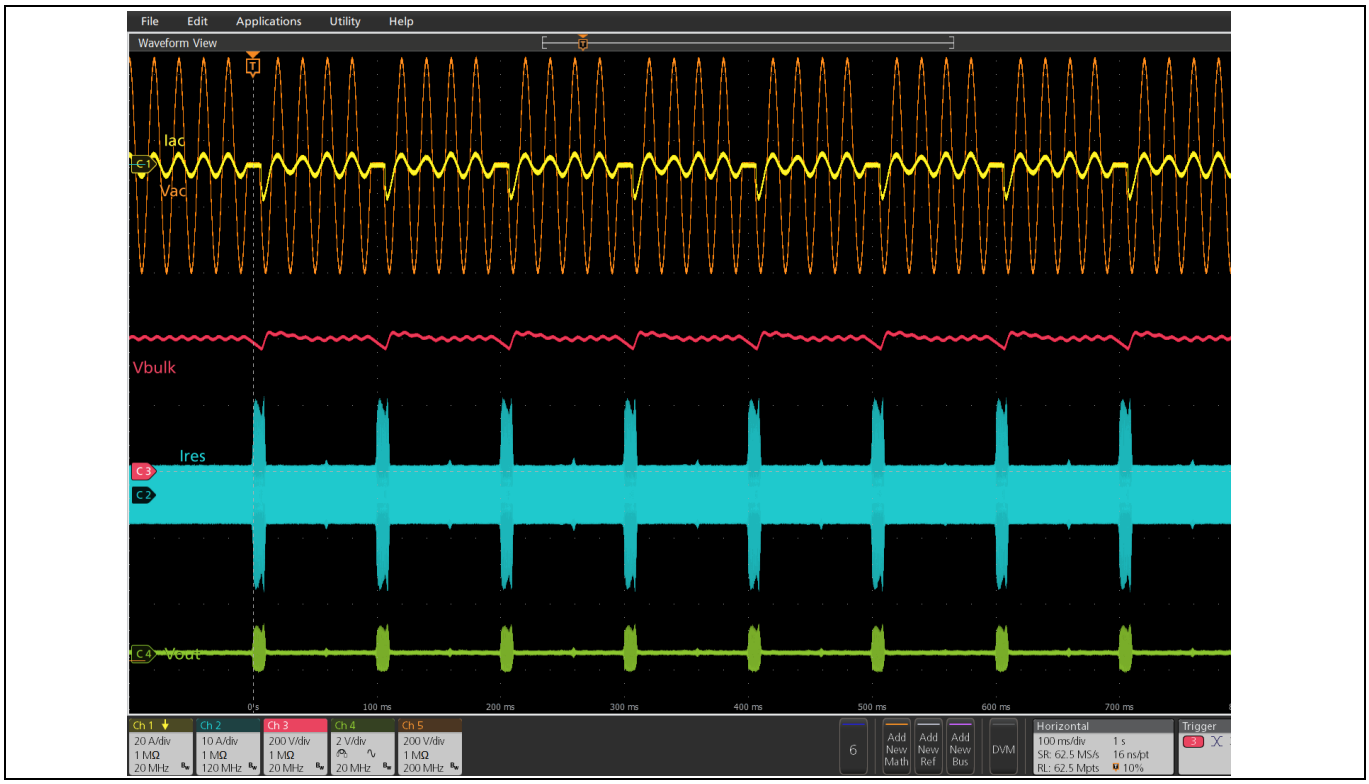


Figure 33 10 ms hold-up time at full load and 230 V AC

3.3.6 Load-jump

Figure 34 and **Figure 35** show a load-jump of the PSU output current from 5 A to 35 A and from 35 A to 5 A, respectively.

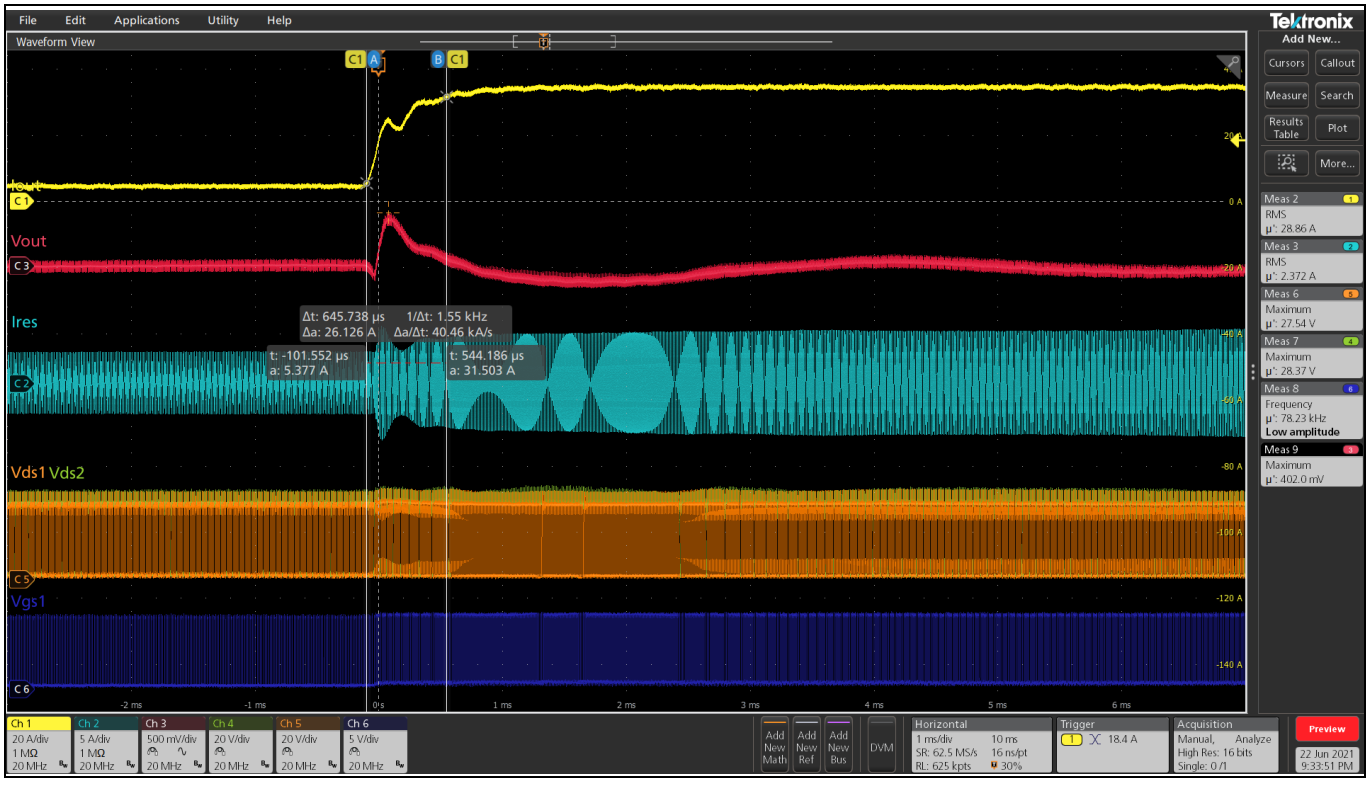


Figure 34 Load-jump of the complete PSU from 5 A to 35 A

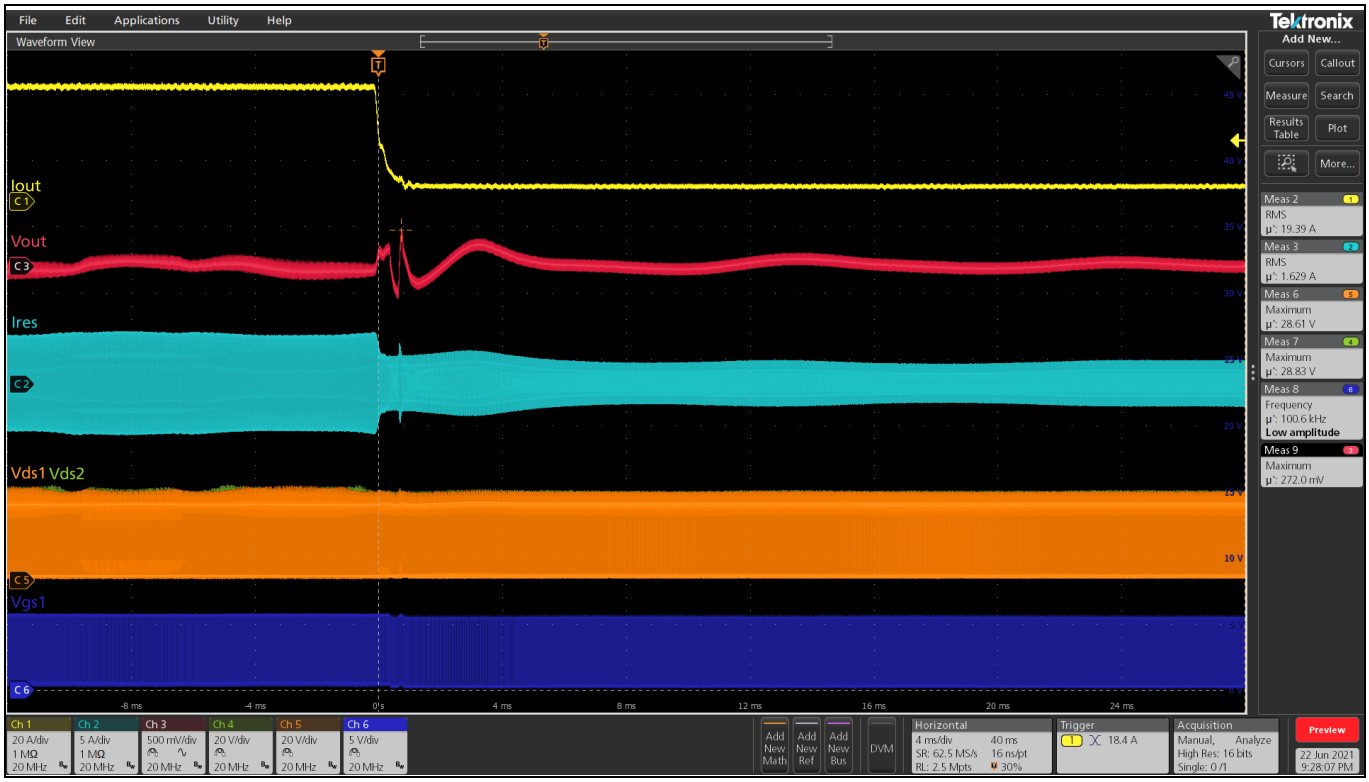


Figure 35 Load-jump of the complete PSU from 35 A to 5 A

3.3.7 Thermal characterization

The PSU has been thermally characterized with a water cooling setup, as shown in **Figure 36**. The demo board's metal baseplate has been attached to a cold plate with water temperature controlled by a chiller from Julabo, as shown in **Figure 36**. Thermocouples have been attached to the main components of the power supply to sense the temperature over a wide baseplate temperature range (from 20°C to 80°C). Efficiency was also measured during the thermal measurements.

PSU efficiency complies with the specification over a wide range of temperatures in both low- and high-line voltage conditions, as shown in **Figure 37** and **Figure 38**.

All main PSU component temperatures are shown in the following figures.

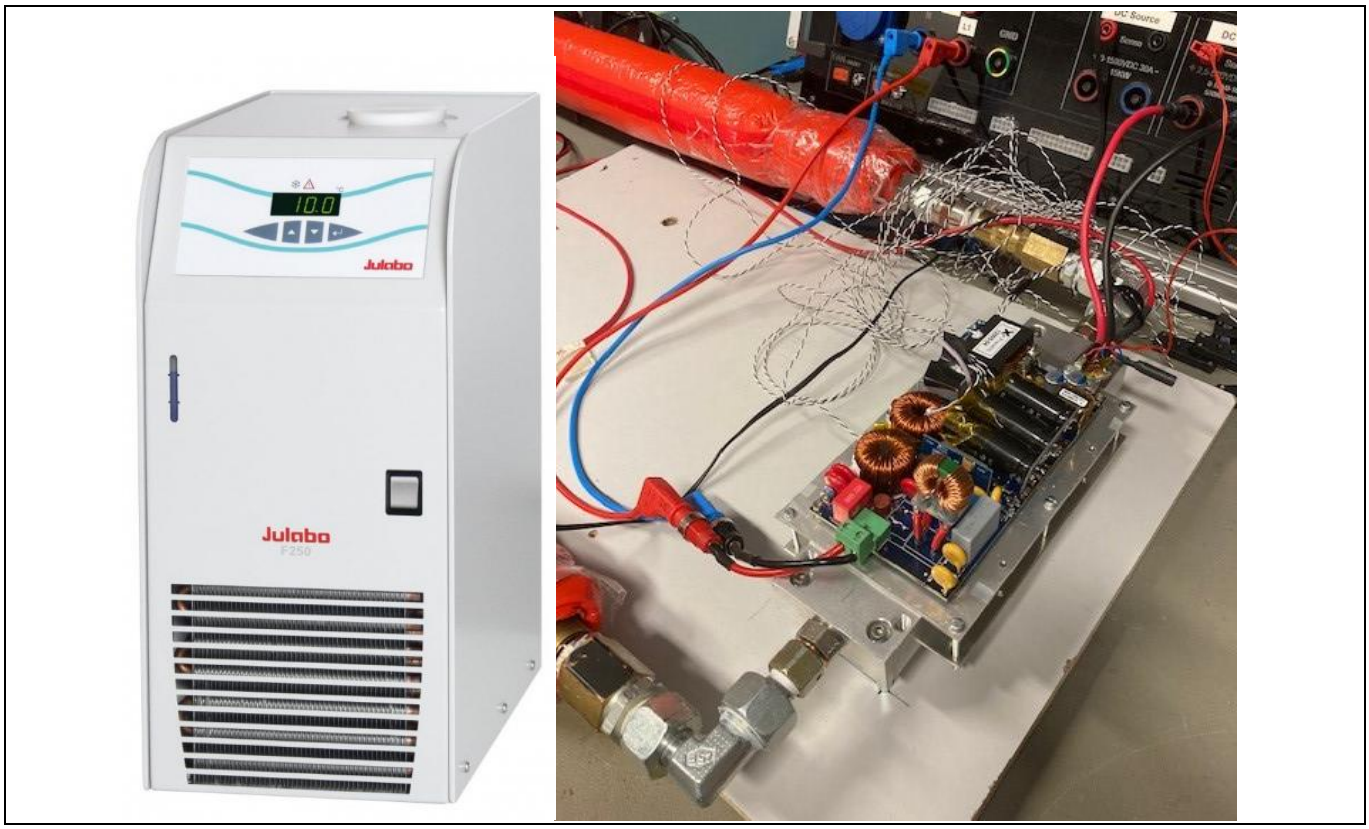


Figure 36 **Thermal characterization test bench based on water cooling**

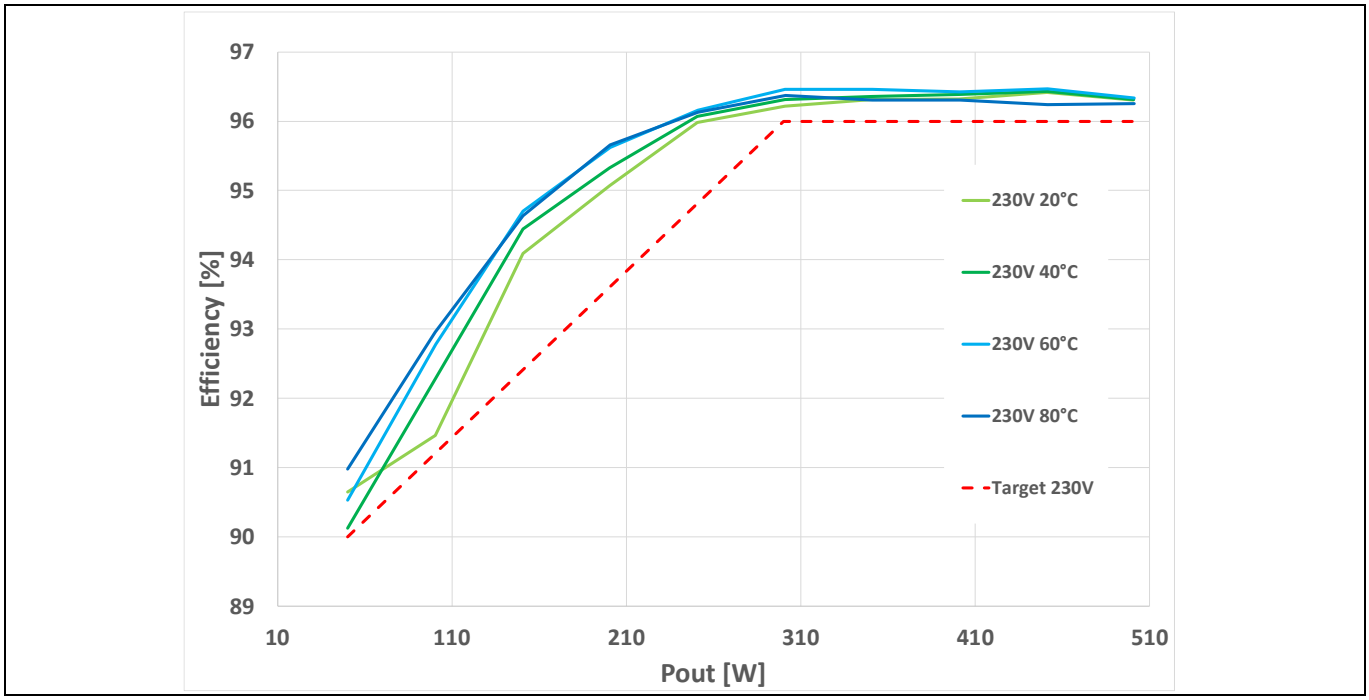


Figure 37 **Measured efficiency of the complete power supply for different baseplate temperatures at 230 V AC**

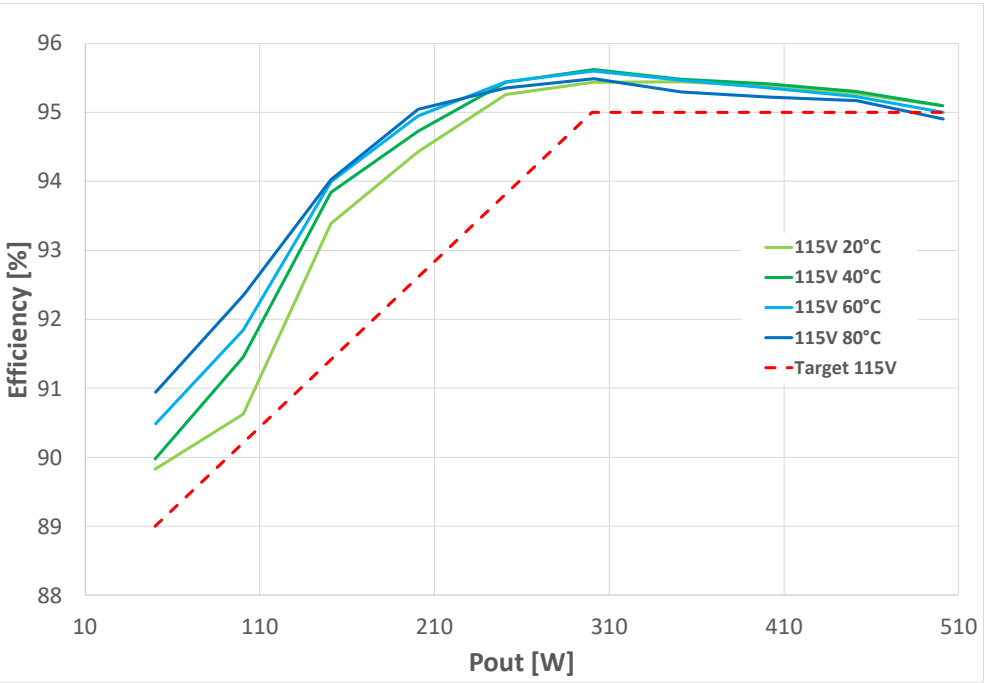
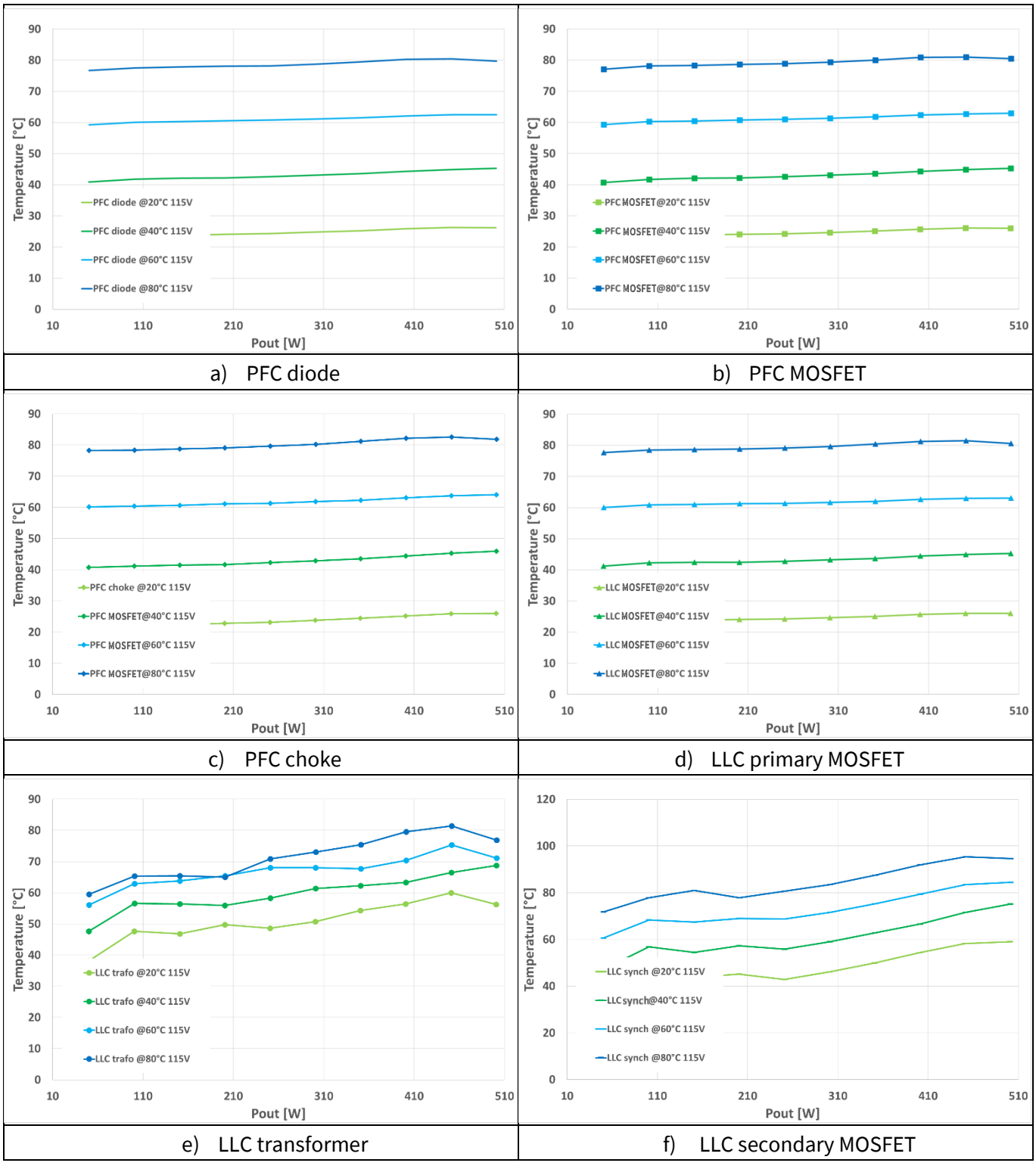


Figure 38 **Measured efficiency of the complete power supply for different baseplate temperatures at 115 V AC**



a) PFC diode | b) PFC MOSFET

c) PFC choke | d) LLC primary MOSFET

e) LLC transformer | f) LLC secondary MOSFET

Figure 39 Measured temperature of the PSU main components for different baseplate temperatures at 115 V AC

3.3.8 EMI

The conducted electromagnetic interference (EMI) of the converter has been measured operating at 500 W power with a passive resistive load. **Figure 40** and **Figure 41** show the results of the average and the positive peak measurements at 115 V AC and 230 V AC, respectively.

Experimental results

As can be seen, the PSU is fully compliant with class A limits in both peak and average. Furthermore, positive peak measurements represent a worst case compared to the quasi-peak of the standard. A margin of 6 dB is always achieved.

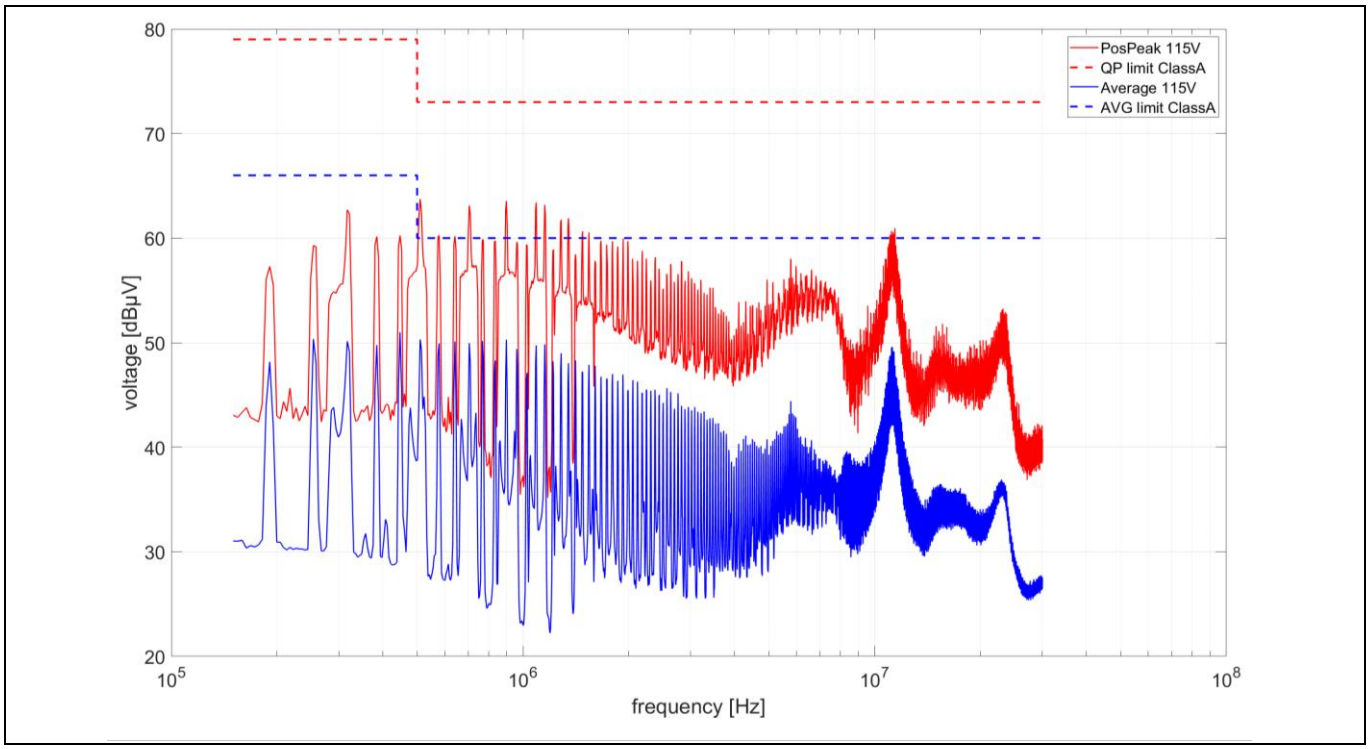


Figure 40 Measured EMI spectrum of the complete power supply prototype at 115 V AC and 500 W

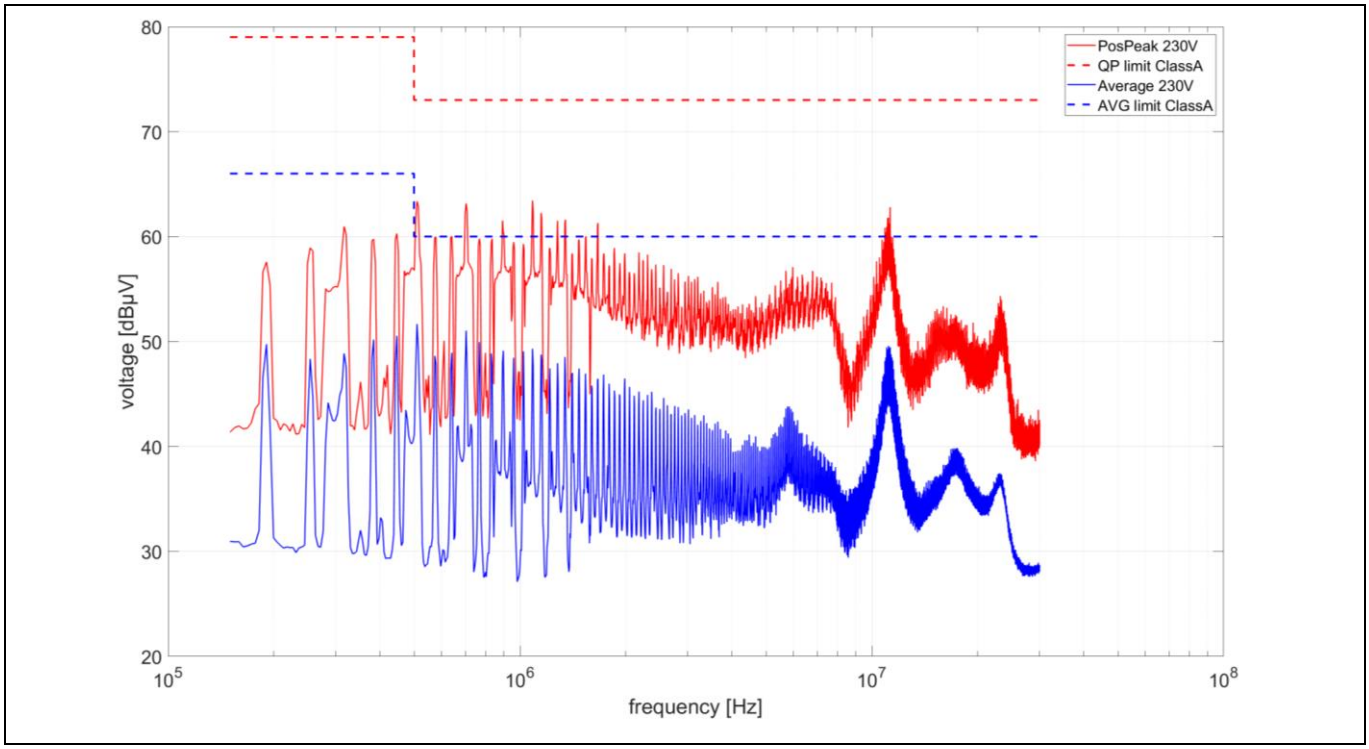


Figure 41 Measured EMI spectrum of the complete power supply prototype at 230 V AC and 500 W

3.3.9 Surge protection

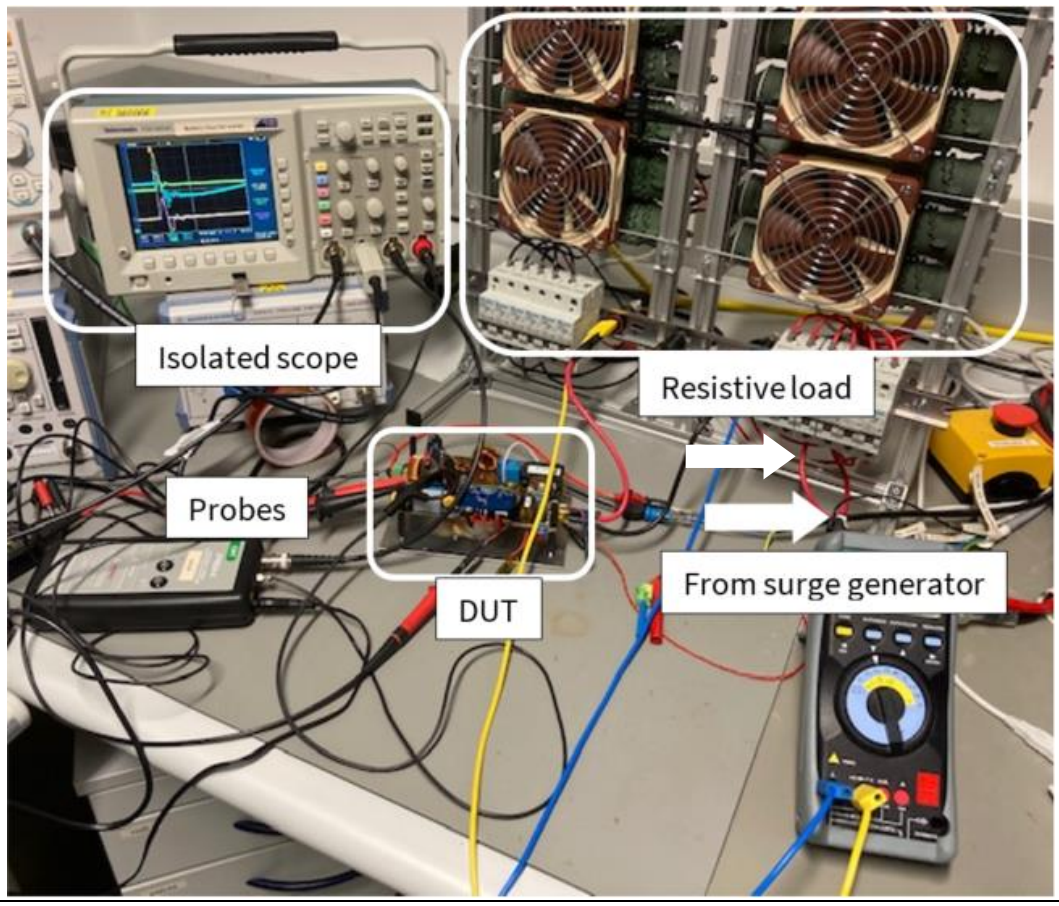


Figure 42 Surge measurement test bench

The test bench for surge pulse testing is shown in **Figure 42.** The surge generator NSG 3040 is coupled with a standard AC source. CWG of 1.2/50 µs with a series resistor of 2 Ω is applied by the surge generator to the line and neutral conductors. Only differential mode surge is considered in this application note. The load is a passive resistor. Rogowski coils are used for current measurements, and a battery isolated oscilloscope is used for acquisitions.

The surge pulse is applied during the positive peak of the AC voltage (at 90 degrees of the sinusoid), as shown in **Figure 43**, with a pulse amplitude to a maximum of 3.5 kV. The V_{bulk} (green line) and V_{GS} (blue) of **Figure 43** are related to the pre-charge MOSFET. Input voltage (light blue) and input current (magenta) are captured before the EMI filter.

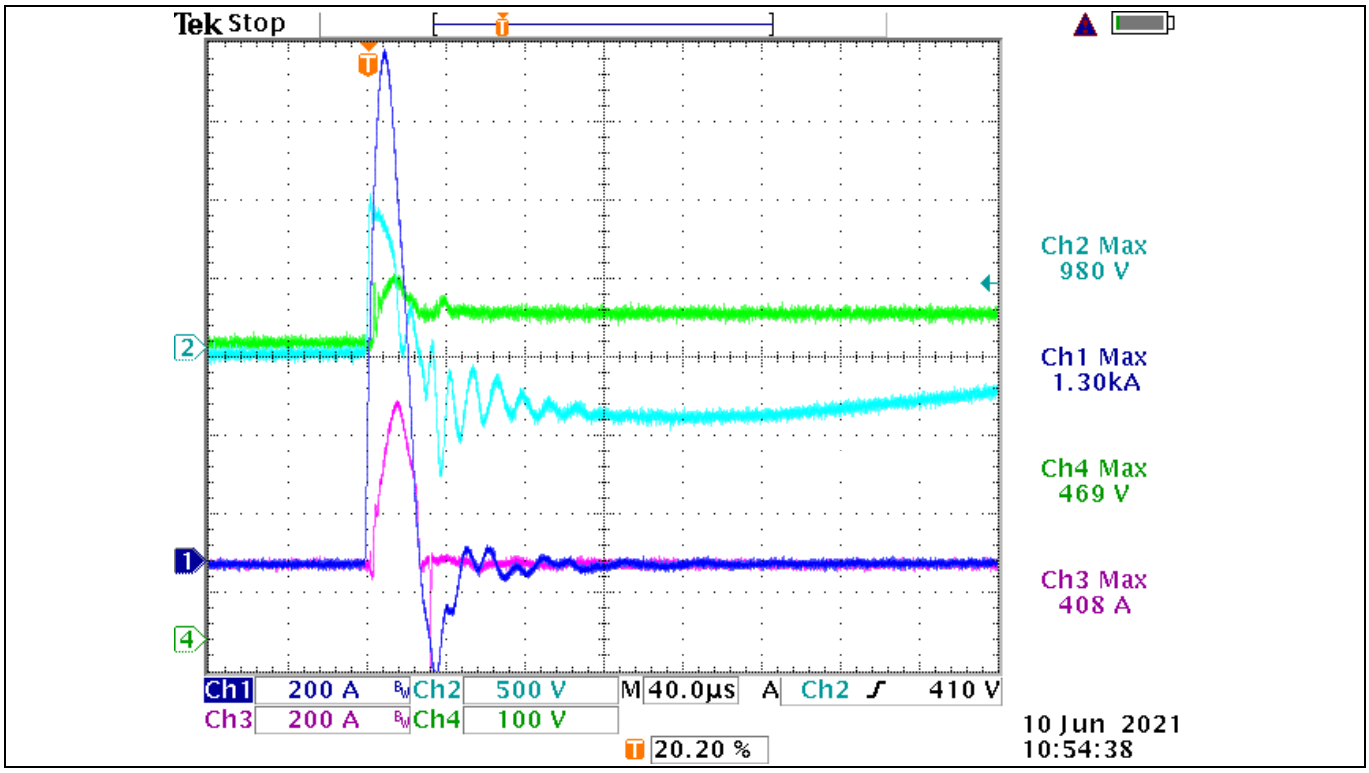


Figure 43 Surge pulse at 3.5 kV and 90 degrees

The surge pulse is applied during the positive peak of the AC voltage (at 90 degrees of the sinusoid), as shown in **Figure 44**, with a pulse amplitude of 4 kV. The V_{bulk} (green line) and V_{GS} (blue) are related to the pre-charge MOSFET. Input voltage (light blue) and input current (magenta) are captured before the EMI filter.

The surge pulse is applied during the positive peak of the AC voltage (at 0 degrees of the sinusoid), as shown in **Figure 45**, with a pulse amplitude of 4 kV. The V_{bulk} (green line) and V_{GS} (blue) are related to the pre-charge MOSFET. Input voltage (light blue) and input current (magenta) are captured before the EMI filter.

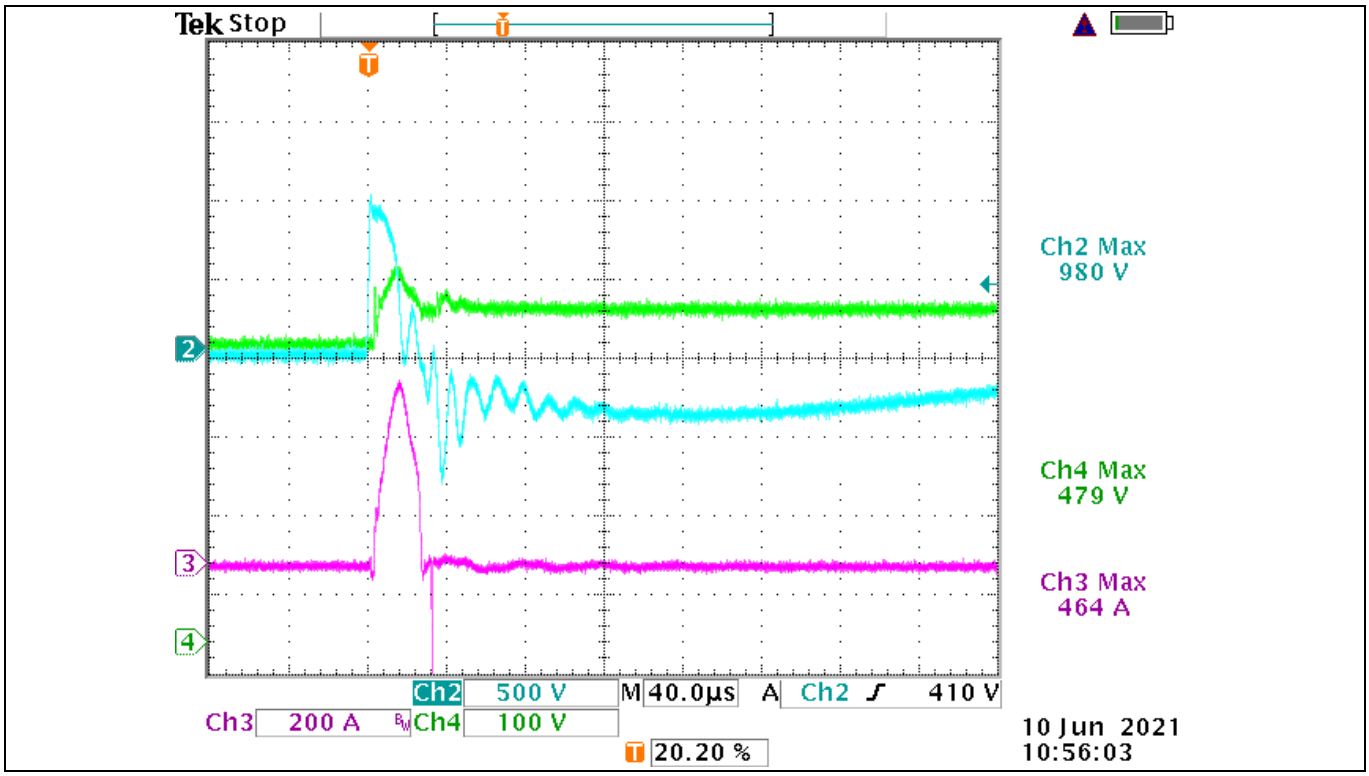


Figure 44 Surge pulse at 4 kV and 90 degrees

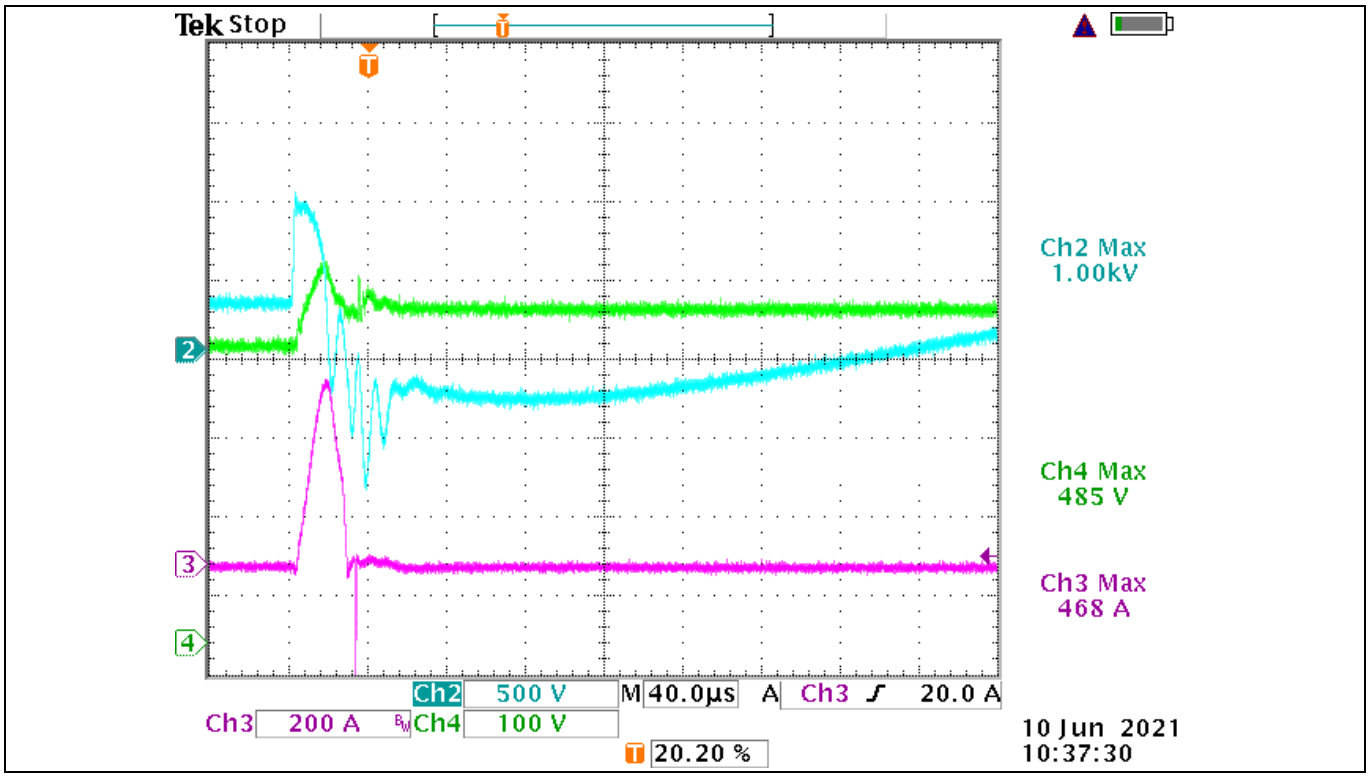


Figure 45 Surge pulse at 4 kV and 0 degrees

4 Schematics

4.1 Main board

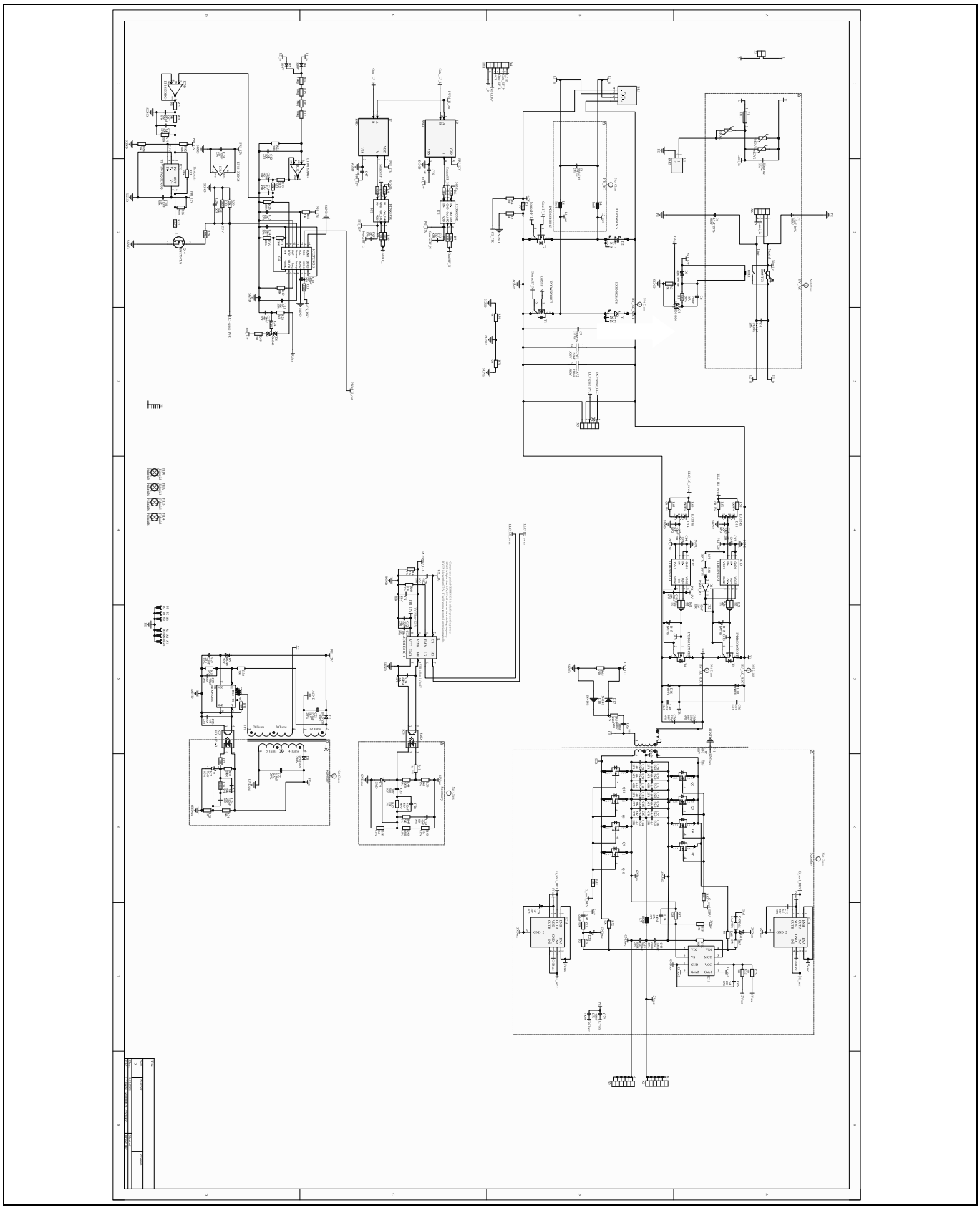


Figure 46 Main board

4.2 Control cards

4.2.1 Active-line rectifier board

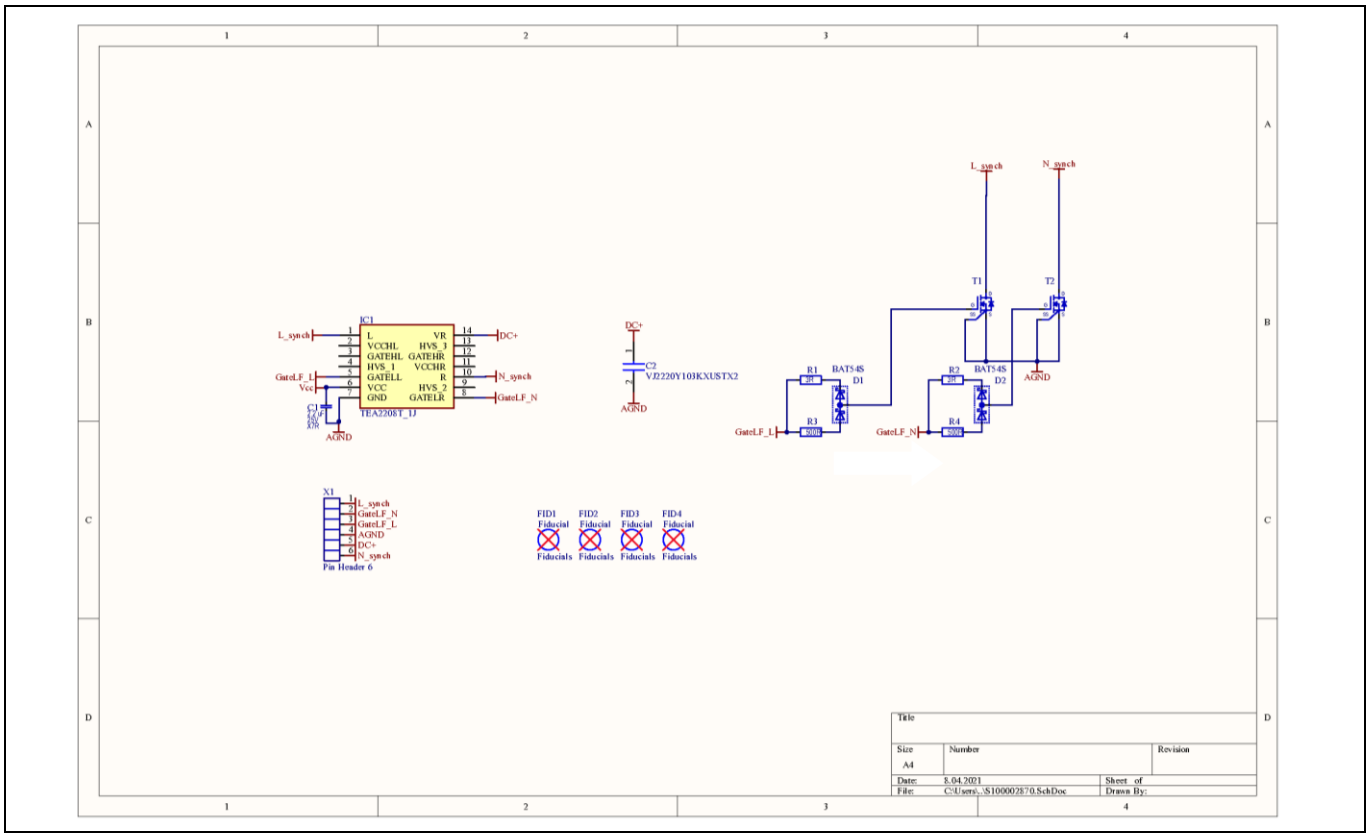


Figure 47 Active-line rectifier board

4.2.2 DC-link capacitor board

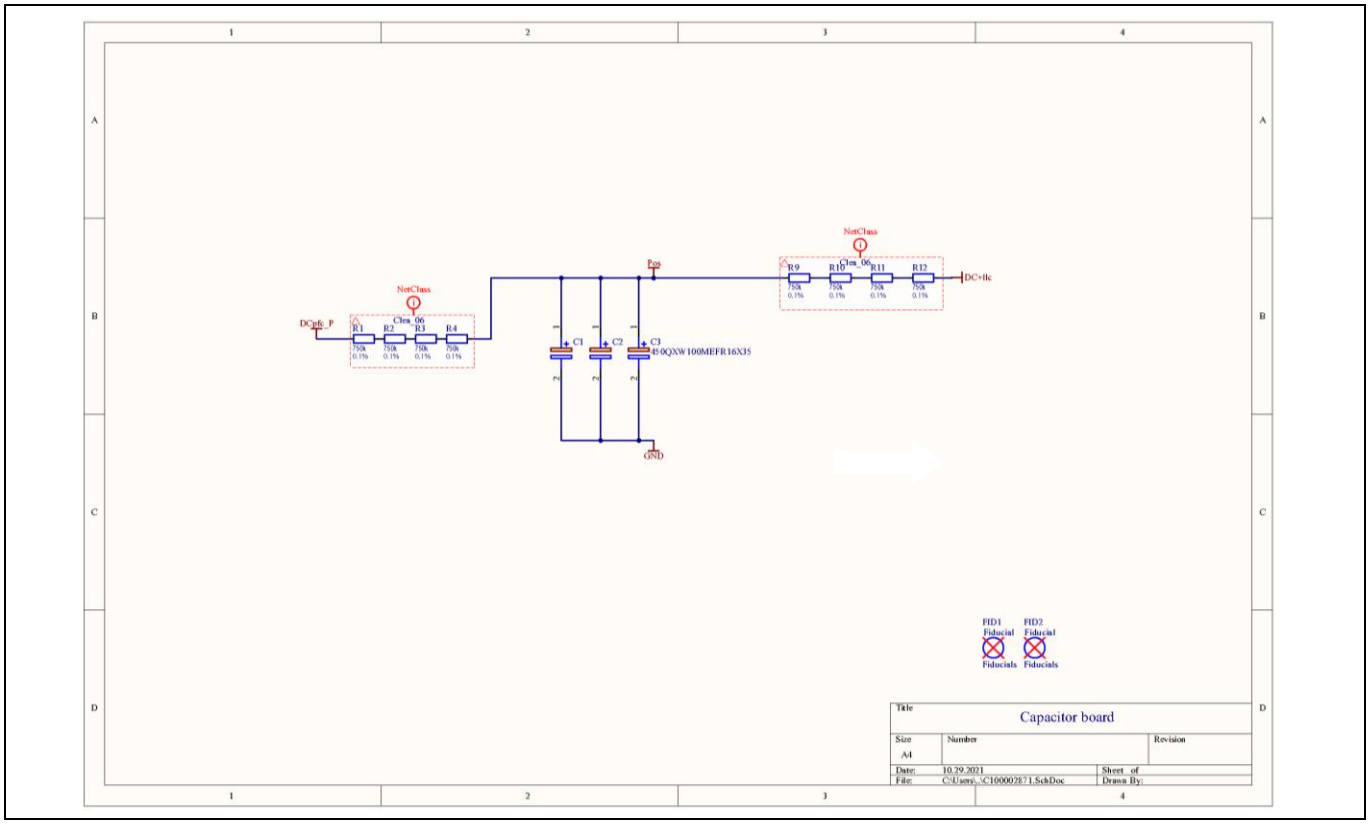


Figure 48 Active-line rectifier board

4.3 Bill of materials

The complete BOM is available from the downloads section of the Infineon website. A log-in is required to download this material.

Table 3 BOM of the main board

S. no.	Ref. designator	Description	Manufacturer	Part no.
2	D1, D9	Schottky diode	Infineon	BAT165
2	D2, D3	CoolSiC™ 650 V Schottky diode	Infineon	IDDD08G65C6
2	D12, D15	Schottky diode	Infineon	BAT165E-6327
2	IC1, IC2	Gate-driver IC	Infineon	1EDN8550BXTSA1
1	IC4	CCM PFC controller	Infineon	ICE3PCS01GXUMA1
1	IC6	Flyback controller	Infineon	ICE2QR2280G-1
2	IC10, IC12	Gate-driver IC	Infineon	1EDI20N12AFXUMA1
1	IC11	SR controller	Infineon	IR11688STRPBF
2	IC14, IC15	Gate-driver IC	Infineon	2EDN7524GXTMA1
1	Q1	Signal MOSFET	Infineon	BSS138N
8	Q2, Q3, Q4, Q5, Q8, Q9, Q10, Q11	Low-voltage power MOSFET	Infineon	IQE013N04LM6ATMA1
2	T1, T2	600 V power MOSFET	Infineon	IPDD60R080G7XTMA1

S. no.	Ref. designator	Description	Manufacturer	Part no.
2	**T3, T4**	**600 V power MOSFET**	**Infineon**	**IPDD60R075CFD7XTMA1**
1	**U4**	**V DC resonant controller**	**Infineon**	**ICE1HS01G-1**
1	BR1	Bridge rectifier	Vishay	GBUE2560-M3/P
3	C1, C5, C41	Ceramic capacitor 0.0047 µF 300 V AC Y5V 20% (10.5 x 5 x 13.5 mm) radial 7.5 mm 125°C	Vishay	VY2472M41Y5VS63V7
2	C2, C8	Foil capacitor	Würth Electronics	890324025045CS
1	C4	Foil capacitor	Kemet	R46KN415040P1M
3	C6, C21, C22	Polarized capacitor	Panasonic	1CTQC15173F1
1	C9	Foil capacitor	Kemet	R46KN368000P0M
1	C10	Ceramic capacitor		470 pF
1	C11	Ceramic capacitor		4n7
2	C12, C20	Ceramic capacitor		1 nF
9	C13, C16, C39, C47, C66, C68, C69, C77, C78	Ceramic capacitor		1 µF
7	C14, C17, C18, C19, C72, C73, C74	Ceramic capacitor		100 nF
1	C15	Ceramic capacitor		470 nF
2	C23, C26	Ceramic capacitor		1 nF
5	C24, C37, C42, C44, C46	Ceramic capacitor		100 nF
4	C25, C30, C38, C45	Ceramic capacitor		100 pF
1	C27	Polarized capacitor	Panasonic	20TQC33MYFD
1	C28	Ceramic capacitor		220 nF
1	C31	Ceramic capacitor		22 nF
1	C32	Ceramic capacitor		10 µF
1	C33	Ceramic capacitor		100 nF
1	C34	Ceramic capacitor		680 pF
1	C35	Ceramic capacitor		10 nF
2	C36, C48	Foil capacitor	TDK Epcos	B32642B6823J000
2	C40, C43	Ceramic capacitor		0.1 nF
2	C49, C57	Polarized capacitor	United Chemi-Con	APSG160ELL222MJ20S
14	C50, C51, C52, C53, C54, C55, C56, C58, C59, C60, C61, C62, C63, C64	Ceramic capacitor	TDK	C3225X7R1C226K250AC
1	C65	Ceramic capacitor		330 pF

S. no.	Ref. designator	Description	Manufacturer	Part no.
1	C67	Ceramic capacitor		470 nF
2	C75, C76	Ceramic capacitor	Kyocera AVX	12067A221JAT2A
1	C79	Ceramic capacitor		1 µF
2	CAP1, CAP2	Capacitor	Kemet	C1808W154KCRACTU
2	D4, D5	Standard diode	STMicroelectronics	STTH208U
1	D6	Small signal dual Schottky diode		
2	D7, D8	Diode	Diodes	DFLS1200-7
2	D10, D16	Diode	ON Semiconductor	MURS360BT3G
2	D11, D14	Schottky diode	ON Semiconductor/ Fairchild	BAT54S
1	D13	Diode	Taiwan Semiconductor	RSFJLR3
2	D17, D18	High-conductance fast diode	ON Semiconductor/ Fairchild	1N4148WS
2	D19, D20	Schottky diode	NXP Semiconductors	BA591, 115
1	F1	Fuse	Littelfuse Wickmann	38321000000
1	H1	Heatsink for 5G_Board_Pevere_V1	Semicore	
1	IC3	Dual precision op-amp	Texas Instruments	LT1013DDG4
1	IC5	Integrated circuit	Vishay Semiconductors	VOL617A-3X001T
1	IC7	Integrated circuit	Texas Instruments	TL431BCDBZR
1	IC8	Optocoupler	Vishay Semiconductors	VO618A-3X017T
1	IC9	TL431 – adjustable precision shunt regulator	Texas Instruments	TL431ACDBZR
1	IC13	Integrated circuit		
2	L4, L6	PFC choke		
1	L7	Magnetic choke	Eaton Coiltronics	FP1008R1-R180-R
3	MOV1, MOV2, MOV3	Varistor	Littelfuse	V320LA20AP
1	NTC1	NTC resistor	Ametherm	SL1830006
1	Q14	MOSFET (N-channel)		BS170FTA
2	R1, R33	Resistor		390 R
2	R2, R32	Resistor		15k
1	R3	Resistor		0R015 – 3 W
5	R4, R56, R59, R63, R71	Resistor		0 R
4	R6, R9, R69, R70	Resistor		100k
2	R7, R10	Resistor		1R2

S. no.	Ref. designator	Description	Manufacturer	Part no.
2	R8, R11	Resistor		13 R
3	R12, R24, R49	Resistor		15 R
1	R13	Resistor		510 R
4	R14, R15, R16, R17	Resistor		1 Meg
1	R18	Resistor		30k2
2	R19, R23	Resistor		68k
1	R20	Resistor		3k3
1	R21	Resistor		330k
4	R22, R66, R73, R82	Resistor		100k
3	R25, R26, R79	Resistor		200k
1	R27	Resistor		4k7
3	R29, R67, R74	Resistor		20k
1	R30	Resistor		300k
5	R31, R54, R57, R58, R62	Resistor		4R7
2	R34, R48	Resistor		3k6
1	R35	Resistor		68 R
1	R36	Resistor		866 R
2	R37, R38	Resistor		2K7
1	R39	Resistor		2k2
1	R40	Resistor		13k
1	R41	Resistor		1k
1	R42	Resistor		12k
1	R43	Resistor		27k
1	R44	Resistor		820 R
1	R46	Resistor		680 R
1	R47	Resistor		22k
2	R50, R60	Resistor		150 R
2	R51, R61	Resistor		30 R
1	R52	Resistor		10 R
2	R53, R55	Resistor		0 R
1	R64	Resistor		220 R
1	R65	Resistor		75 R
1	R68	Resistor		50
1	R72	Resistor		50 R
1	R76	Resistor		82k
2	R77, R78	Resistor		56k
1	R83	Resistor		576k

S. no.	Ref. designator	Description	Manufacturer	Part no.
1	R84	Resistor		25k
1	R85	Resistor		47K
1	R86	Resistor		470k
1	R87	Resistor		270 R
1	REL1	Relais	TE Connectivity OEG	1721539-5
1	TF1	Bias supply transformer	ICE	8032.0205.017
1	TF2	Integrated transformer EQ38 – 3C95	ICE	8077.0304.001
1	U1	GDT – surge arrester		SL1002A600SP
2	U2, U3	AND gate IC single-channel 5-SSOP BU4S81G2-TR		BU4S81G2-TR
1	X1	Connector	Phoenix Contact	1766233
2	X2, X5	Pin-header, 6 contacts	ERNI	214788
1	X3	Electrolytic capacitor daughter card		C100002871
1	X4	AC-line rectification daughter card		S100002870
1	X6	Pin-header, 4 contacts		EMI100002870

Table 4 BOM of the active-line rectifier board

S. no.	Ref. designator	Description	Manufacturer	Part no.
2	**T1, T2**	**N-channel MOSFET**	**Infineon**	**IPT60R022S7**
1	IC1	Integrated circuit	NXP	TEA2208T_1J
1	C1	Ceramic capacitor		2.2 µF
2	D1, D2	Schottky diode		BAT54S
2	R1, R2	Resistor		3 R
2	R3, R4	Resistor		500 R

Table 5 BOM of the DC-link capacitor board

S. no.	Ref. designator	Description	Manufacturer	Part no.
2	C1, C2	Polarized capacitor	Rubycon	450HXW220MEFR18X45
1	C3	Polarized capacitor	Rubycon	450QXW100MEFR16X35
8	R1, R2, R3, R4, R9, R10, R11, R12	Resistor		750k 0.1%

5 References and appendices

5.1 Abbreviations and definitions

Table 6 Abbreviations

Abbreviation	Meaning
CE	Conformité Européenne
EMI	Electromagnetic interference
UL	Underwriters Laboratories

5.2 References

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[3] "**200 W 24 V 6 A & 12 V 5 A SMPs demonstrator with ICE1HS01G-1**", AN-EVAL-1HS01G-1-200W, Infineon Technologies, June 2015

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