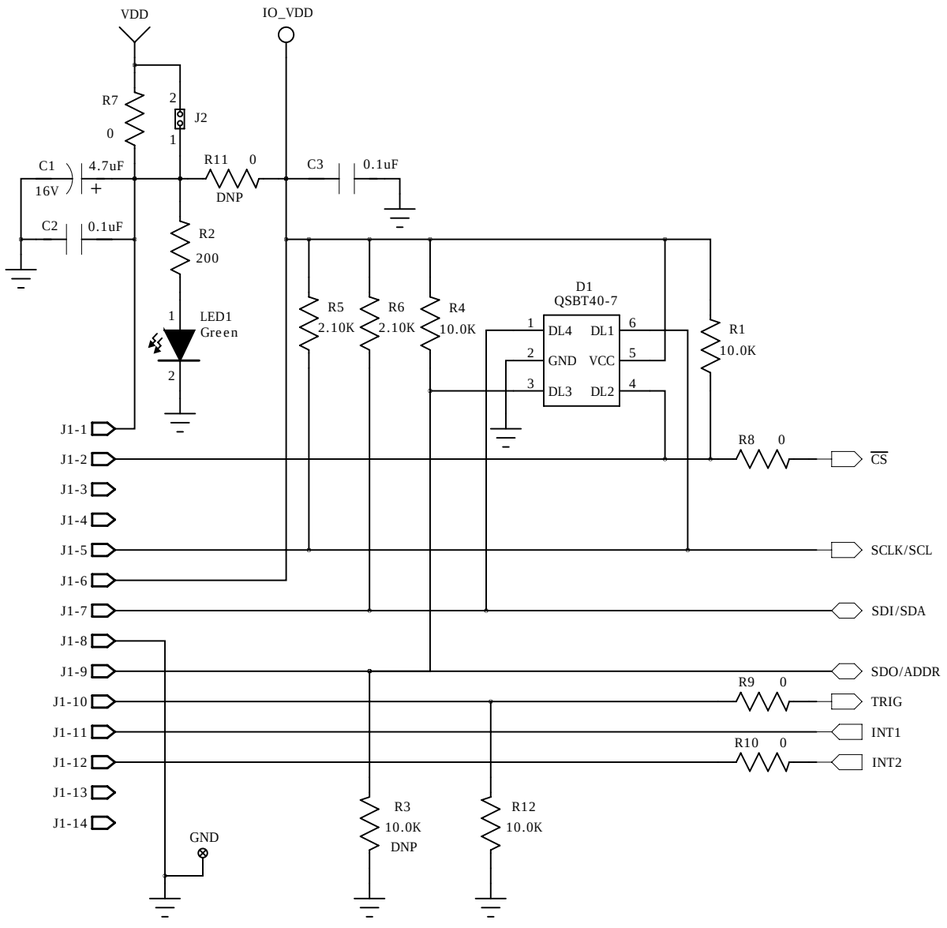

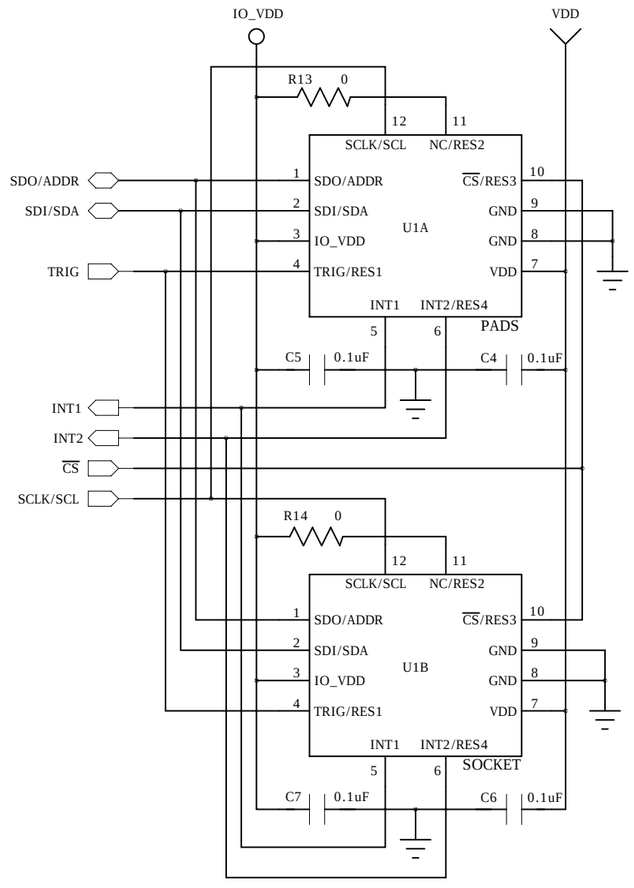

PIN	KX021,KX022, KX112,KX122, KX222,KX116, KX126	KXTJ2	KXTJ3
1	SDO/ADDR	ADDR	ADDR
2	SDI/SDA	SDA	SDA
3	IO_VDD	IO_VDD	IO_VDD
4	TRIG	RES****	RES****
5	INT1	INT1	INT1
6	INT2	GND*	GND*
7	VDD	VDD	VDD
8	GND	GND	GND
9	GND	GND	GND
10	nCS	VDD**	VDD**
11	NC	IO_VDD	IO_VDD***
12	SCLK/SCL	SCL	SCL

* GND pins 6, 8, and 9 are internally tied together. Thus, pin 6 may be left floating.
** VDD pins 7, and 10 are internally tied together. Thus, pin 10 may be left floating.
*** IO_VDD pins 3, and 11 are internally tied together. Thus, pin 11 may be left floating. (Does not apply to KXTJ2)
**** RES pin 4 connect to GND. Do not leave floating.

NOTES:

1) All resistors are 1%, 1/10W, 0603 unless otherwise specified.
2) All capacitors are 0.1uF, 10%, 50WVDC, 0603 unless otherwise specified.
3) U1B Socket: Loranger, 020SQ 012J6618A.
4) Supported device and 7-bit I2C address:
   a) KX022: 1Eh, 1Fh.
   b) KX112: 1Eh, 1Fh.
   c) KX122: 1Eh, 1Fh.
   d) KX021: 1Eh, 1Fh.
   e) KX222: 1Eh, 1Fh.
   f) KXTJ2: 0Eh, 0Fh.
   g) KXTJ3: 0Eh, 0Fh.
   h) KX126: 1Eh, 1Fh.
   i) KX116: 1Eh, 1Fh.
5) Population-
   a) KX021, KX022, KX112, KX122, KX116, KX126, KX222:
      i. R1, R2, R4, R5, R6, R7, R8, R9, R10, R12
      ii. Remove: R3, R11, R13, R14
   b) KXTJ2:
      i. Populate R1 (don't care), R2, R4, R5, R6, R7, R9, R12, R13, R14
      ii. Remove: R3, R8, R10, R11
   c) KXTJ3:
      i. Populate R1 (don't care), R2, R4, R5, R6, R7, R9, R12, R13 (don't care), R14 (don't care)
      ii. Remove: R3, R8, R10, R11

DRAWN: J Zappala	DATED: 03/05/2018		
CHECKED: A Chernyakov	DATED: 03/05/2018		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		

COMPANY: Kionix Inc.

TITLE: 2x2 LGA 12-Pin Evaluation Board

CODE:	SIZE:	DRAWING NO:	REV:
DWG987	B	KMAEDA001R00	G

SCALE: NONE SHEET: 1 OF 2

REVISION RECORD				
DATE:	DRAWN BY:	DESCRIPTION:	CHECKED BY:	DATE:
11/29/2016	J Zappala	Initial release.		
11/30/2016	J Zappala	1) General rearrangement.		
		2) Add devices, Note 4f and 4g.		
		3) Remove D2.		
11/30/2016	J Zappala	1) Add R7, J2, and GND PTH.		
12/01/2016	J Zappala	1) Remove DNP from R10, R9, R13, R14; add DNP to R3.		
		2) Add DNP to R3.		
		3) Add Note 5.		
12/06/2016	J Zappala	1) Swap D1 pins for better layout.		
		2) Add fiducials.		
12/22/2017	J Zappala	1) Add KX126, update Notes 4 and 5.		
03/05/2018	J Zappala	1) Add KX116, update Notes 4 and 5.		

MTHOLE1 MTHOLE150
MTHOLE2 MTHOLE150
MTHOLE3 MTHOLE150
MTHOLE4 MTHOLE150
FD1 FIDUCIAL_40MIL
FD2 FIDUCIAL_40MIL
FD3 FIDUCIAL_40MIL

LOGO1
Kionix Inc.
LOGO

DRAWN: J Zappala	DATED: 03/05/2018
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: Kionix Inc.

TITLE: 2x2 LGA 12-Pin Evaluation Board

CODE:	SIZE:	DRAWING NO:	REV:
DWG987	B	KMAEDA001R00	G

SCALE: NONE SHEET: 2 OF 2