# Off-Line PWM Controllers with Integrated Power MOSFET
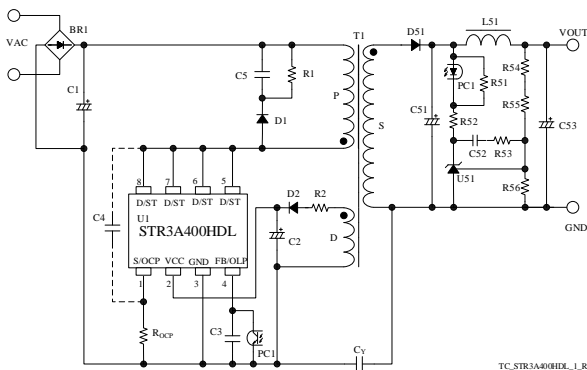# STR3A475HDL

**SanKen**

# Data Sheet

## Description

The STR3A475HDL is power ICs for switching power supplies, incorporating a MOSFET and a current mode PWM controller IC.

The low standby power is accomplished by the automatic switching between the PWM operation in normal operation and the burst-oscillation under light load conditions. The product achieves high cost-performance power supply systems with few external components.

## Features

- Bare Lead Frame: Pb-free (RoHS Compliant)
- Low Thermal Resistance Package
- Improving circuit efficiency (Since the step drive control can keep $V_{RM}$ of secondary rectification diodes low, the circuit efficiency can be improved by low $V_F$)
- Noise Reduction
- Current Mode Type PWM Control
- Soft Start Function
- Automatic Standby Function
  No Load Power Consumption <15 mW
- Operation Mode
  Normal Operation --------------------------- PWM Mode
  Light Load Operation ----------------------- Green-Mode
  Standby -------------------------- Burst Oscillation Mode
- Random Switching Function
- Slope Compensation Function
- Leading Edge Blanking Function
- Bias Assist Function
- Protections
  Two Types of Overcurrent Protection (OCP):
  Pulse-by-Pulse, built-in compensation circuit to minimize OCP point variation on AC input voltage
  Overload Protection (OLP): Auto-restart
  Overvoltage Protection (OVP): Auto-restart
  Thermal Shutdown (TSD): Auto-restart with hysteresis

## Package

DIP8
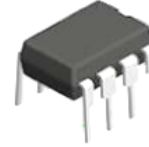
Not to Scale

## Specifications

- $f_{OSC(AVG)}$(typ.) = 100 kHz
- $V_{DSS}$ (min.) = 800 V
- $R_{DS(ON)}$ (max.) = 1.7 Ω
- Output Power, $P_{OUT}$*

| Part Number | $P_{OUT}$ (Adapter) | | $P_{OUT}$ (Open frame) | |
|---|---|---|---|---|
| | AC230V | 85 to 265VAC | AC230V | 85 to 265VAC |
| STR3A475HDL | 39 W | 29 W | 57 W | 36 W |

\* The output power is actual continues power that is measured at 50 °C ambient. The peak output power can be 120 to 140% of the value stated here. Core size, duty cycle, and thermal design affect the output power. It may be less than the value stated here.

## Applications

- AC/DC Adapter
- White Goods
- Other SMPS

## Typical Application



TC_STR3A400HDL_1_R1

# Contents

## 1.   Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified $T_A$ = 25 °C, 5 pin = 6 pin = 7 pin = 8 pin.

| Parameter | Symbol | Conditions | Pins | Rating | Units | Notes |
|---|---|---|---|---|---|---|
| Drain Peak Current[1] | $I_{DPEAK}$ | Single pulse | 8 − 1 | 5.8 | A | |
| Avalanche Energy[2][3] | $E_{AS}$ | | 8 − 1 | 64 | mJ | |
| S/OCP Pin Voltage | $V_{S/OCP}$ | | 1 − 3 | −2 to 6 | V | |
| VCC Pin Voltage | $V_{CC}$ | | 2 − 3 | 32 | V | |
| FB/OLP Pin Voltage | $V_{FB}$ | | 4 − 3 | −0.3 to 14 | V | |
| FB/OLP Pin Sink Current | $I_{FB}$ | | 4 − 3 | 1.0 | mA | |
| D/ST Pin Voltage | $V_{D/ST}$ | | 8 − 3 | −1 to $V_{DSS}$ | V | |
| MOSFET Power Dissipation[4] | $P_{D1}$ | [5] | 8 − 1 | 1.81 | W | |
| Control Part Power Dissipation | $P_{D2}$ | | 2 − 3 | 1.3 | W | $V_{CC} \times I_{CC}$ |
| Operating Ambient Temperature | $T_{OP}$ | | — | −40 to 125 | °C | |
| Storage Temperature | $T_{STG}$ | | — | −40 to 125 | °C | |
| Junction Temperature | $T_J$ | | — | 150 | °C | |

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[1] See Section 4.2.

[2] See Figure 4-2.

[3] Single pulse, $V_{DD}$ = 99 V, L = 20 mH

[4] See Section 4.3.

[5] When embedding this hybrid IC onto the printed circuit board (cupper area in a 15 mm × 15 mm).

## 2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified $T_A$ = 25 °C, $V_{CC}$ = 18 V, 5 pin = 6 pin = 7 pin = 8 pin.

| Parameter | Symbol | Conditions | Pins | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| **Power Supply Startup Operation** | | | | | | | | |
| Operation Start Voltage | $V_{CC(ON)}$ | | 2 − 3 | 13.8 | 15.0 | 16.2 | V | |
| Operation Stop Voltage[1] | $V_{CC(OFF)}$ | | 2 − 3 | 7.6 | 8.5 | 9.2 | V | |
| Circuit Current in Operation | $I_{CC(ON)}$ | $V_{CC}$ = 12 V | 2 − 3 | — | 2.1 | 3.8 | mA | |
| Startup Circuit Operation Voltage | $V_{ST(ON)}$ | | 8 − 3 | 40 | 47 | 55 | V | |
| Startup Current | $I_{CC(ST)}$ | $V_{CC}$ = 13.5 V | 2 − 3 | −4.5 | − 2.5 | −1.2 | mA | |
| Startup Current Biasing Threshold Voltage | $V_{CC(BIAS)}$ | $I_{CC}$=−500µA | 2 − 3 | 8.0 | 9.6 | 10.5 | V | |
| **Normal Operation** | | | | | | | | |
| Average Switching Frequency | $f_{OSC(AVG)}$ | | 8 − 3 | 90 | 100 | 110 | kHz | |
| Switching Frequency Modulation Deviation | $\Delta f$ | | 8 − 3 | — | 8.4 | — | kHz | |
| Maximum Feedback Current | $I_{FB(MAX)}$ | $V_{CC}$ = 12 V | 4 − 3 | −110 | −72 | −40 | µA | |
| Minimum Feedback Current | $I_{FB(MIN)}$ | | 4 − 3 | −21 | −13 | −5 | µA | |
| **Light Load Operation** | | | | | | | | |
| FB/OLP Pin Starting Voltage of Frequency Decreasing | $V_{FB(FDS)}$ | | 4 − 3 | 2.88 | 3.60 | 4.32 | V | |
| FB/OLP Pin Ending Voltage of Frequency Decreasing | $V_{FB(FDE)}$ | | 4 − 3 | 2.48 | 3.10 | 3.72 | V | |
| Minimum Switching Frequency | $f_{OSC(MIN)}$ | | 8 − 3 | 21.5 | 30.0 | 38.5 | kHz | |
| **Standby Operation** | | | | | | | | |
| Oscillation Stop FB Voltage | $V_{FB(OFF)}$ | | 4 − 3 | 1.41 | 1.54 | 1.67 | V | |
| **Protection** | | | | | | | | |
| Maximum Duty Cycle | $D_{MAX}$ | | 8 − 3 | 70 | 75 | 80 | % | |
| Leading Edge Blanking Time | $t_{BW}$ | | — | — | 330 | — | ns | |
| OCP Compensation Coefficient | DPC | | — | — | 25.8 | — | mV/µs | |
| OCP Compensation Duty Cycle | $D_{DPC}$ | | — | — | 36 | — | % | |
| OCP Threshold Voltage at Zero Duty Cycle | $V_{OCP(L)}$ | | 1 − 3 | 0.735 | 0.795 | 0.855 | V | |
| OCP Threshold Voltage at 36% Duty Cycle | $V_{OCP(H)}$ | | 1 − 3 | 0.843 | 0.888 | 0.933 | V | |
| OCP Threshold Voltage During LEB ($t_{BW}$) | $V_{OCP(LEB)}$ | | 1 − 3 | — | 1.69 | — | V | |
| OLP Threshold Voltage | $V_{FB(OLP)}$ | | 4 − 3 | 6.8 | 7.3 | 7.8 | V | |
| OLP Operation Current | $I_{CC(OLP)}$ | $V_{CC}$ = 12 V | 2 − 3 | — | 260 | — | µA | |
| OLP Delay Time | $t_{OLP}$ | | — | 55 | 75 | 90 | ms | |
| FB/OLP Pin Clamp Voltage | $V_{FB(CLAMP)}$ | | 4 − 3 | 10.5 | 11.8 | 13.5 | V | |

[1] $V_{CC(BIAS)}$ > $V_{CC(OFF)}$ always.

## STR3A475HDL

| Parameter | Symbol | Conditions | Pins | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| OVP Threshold Voltage | $V_{CC(OVP)}$ | | 2 − 3 | 27.0 | 29.1 | 31.2 | V | |
| Thermal Shutdown Operating Temperature | $T_{J(TSD)}$ | | — | 127 | 145 | — | °C | |
| Thermal Shutdown Hysteresis Temperature | $T_{J(TSD)HYS}$ | | — | — | 80 | — | °C | |
| **MOSFET** | | | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{DSS}$ | $I_{DS} = 300\ \mu A$ | 8 – 1 | 800 | — | — | V | |
| Drain Leakage Current | $I_{DSS}$ | $V_{DS} = V_{DSS}$ | 8 – 1 | — | — | 300 | μA | |
| On Resistance | $R_{DS(ON)}$ | $I_{DS} = 0.4\ A$ | 8 – 1 | — | — | 1.7 | Ω | |
| Switching Time | $t_f$ | | 8 – 1 | — | — | 300 | ns | |
| **Thermal Resistance** | | | | | | | | |
| Junction to Case Thermal Resistance[2] | $\theta_{J\text{-}C}$ | | — | — | — | 17 | °C/W | |

[2] $\theta_{J\text{-}C}$ is thermal resistance between junction and case. Case temperature ($T_C$) is measured at the center of the case top surface.

## 3.  Mechanical Characteristics

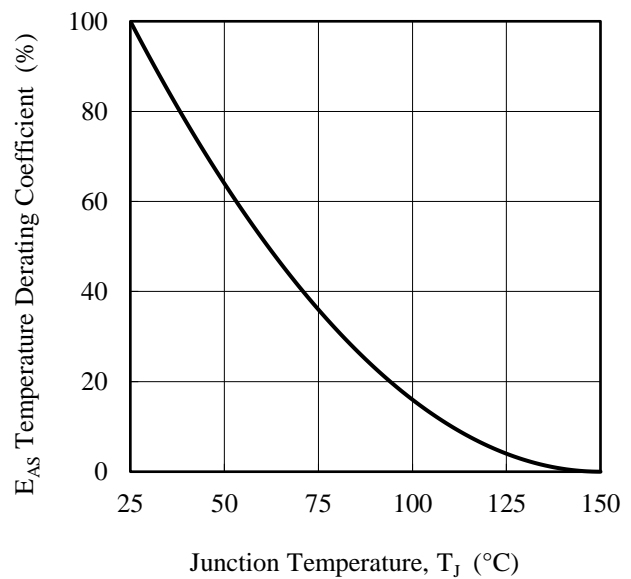| Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Package Weight | | — | 0.51 | — | g |

## 4.  Performance Curves
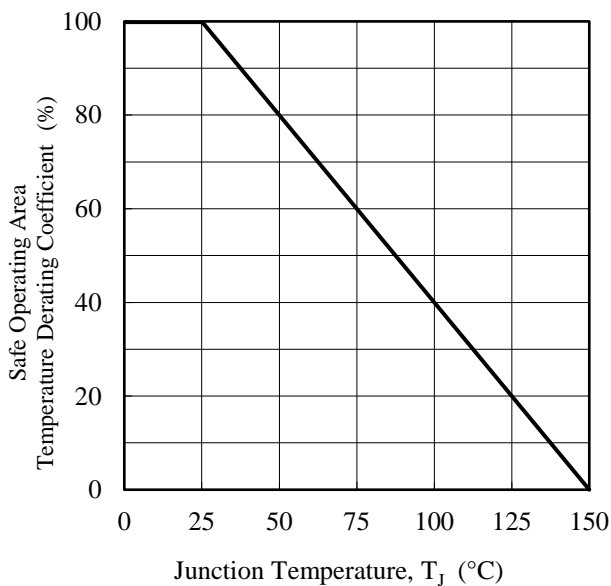
### 4.1  Derating Curves



Figure 4-1.  SOA Temperature Derating Coefficient Curve   Figure 4-2.   Avalanche Energy Derating Coefficient Curve

## 4.2 MOSFET Safe Operating Area Curve

When the IC is used, the safe operating area curve should be multiplied by the temperature derating coefficient derived from Figure 4-1. The broken line in the safe operating area curve is the drain current curve limited by on-resistance. Unless otherwise specified, $T_A = 25\ °C$, Single pulse.
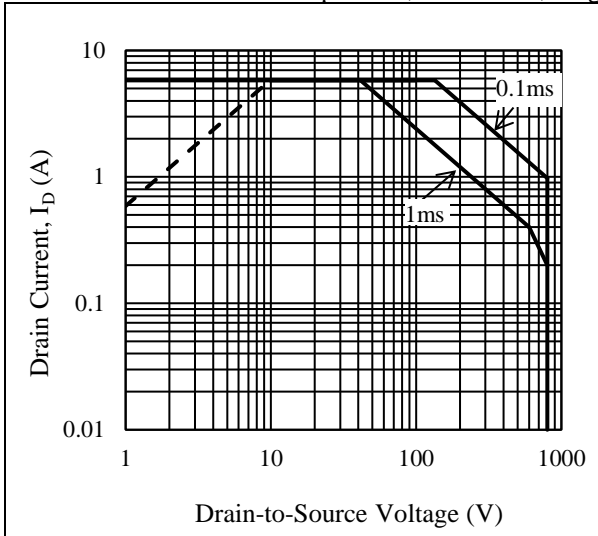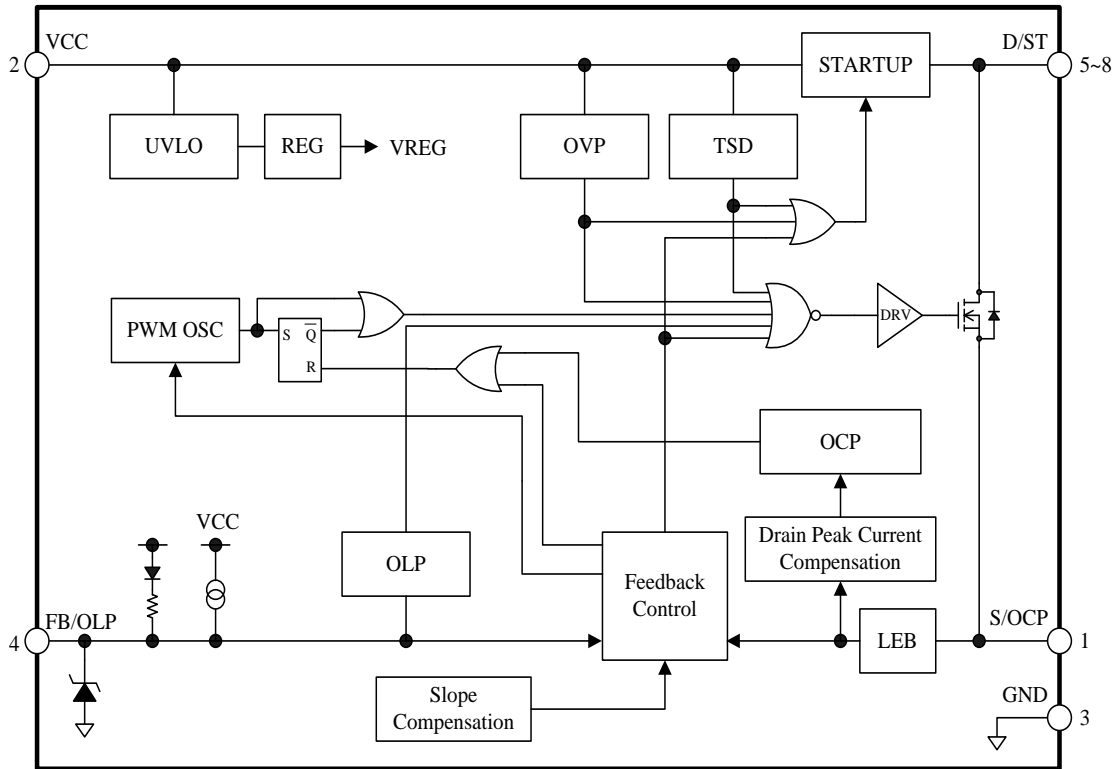


## 4.3 Ambient Temperature versus Power Dissipation Curve
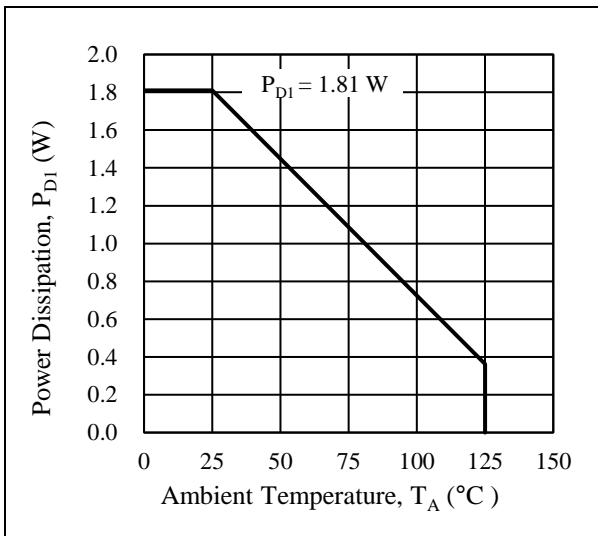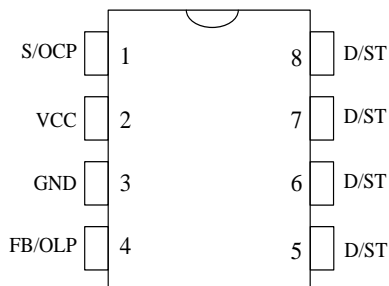


## 4.4 Transient Thermal Resistance Curve
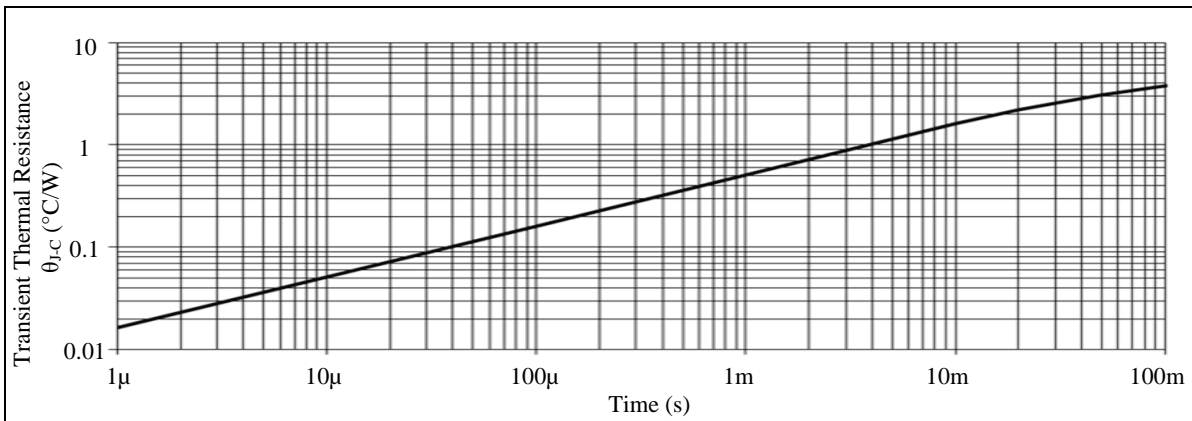
## 5. Block Diagram



BD_STR3A400_R1

## 6. Pin Configuration Definitions



| Pin | Name | Descriptions |
|---|---|---|
| 1 | S/OCP | Power MOSFET source and input of overcurrent protection (OCP) signal |
| 2 | VCC | Power supply voltage input for control part and input of overvoltage protection (OVP) signal |
| 3 | GND | Ground |
| 4 | FB/OLP | Input of constant voltage control signal and input of overload protection (OLP) signal |
| 5 | D/ST | Power MOSFET drain and input of startup current |
| 6 | | |
| 7 | | |
| 8 | | |

## 7. Typical Application

The PCB traces D/ST pins should be as wide as possible, in order to enhance thermal dissipation.

In applications having a power supply specified such that $V_{DS}$ has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.
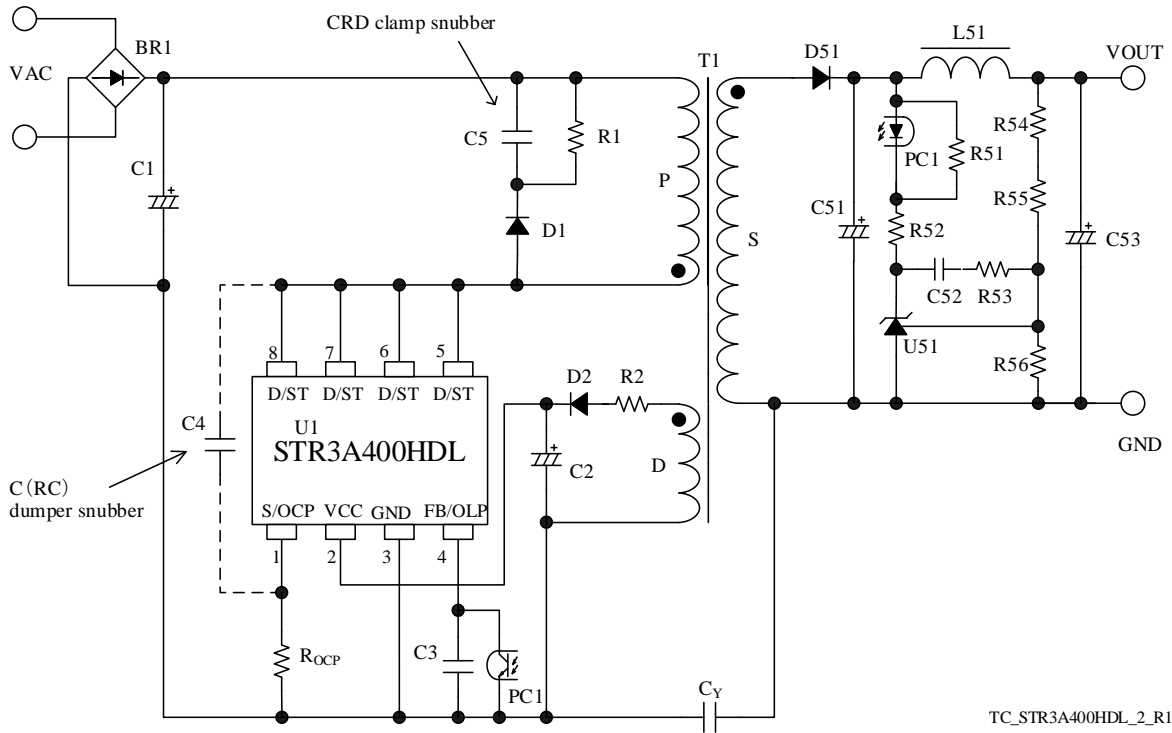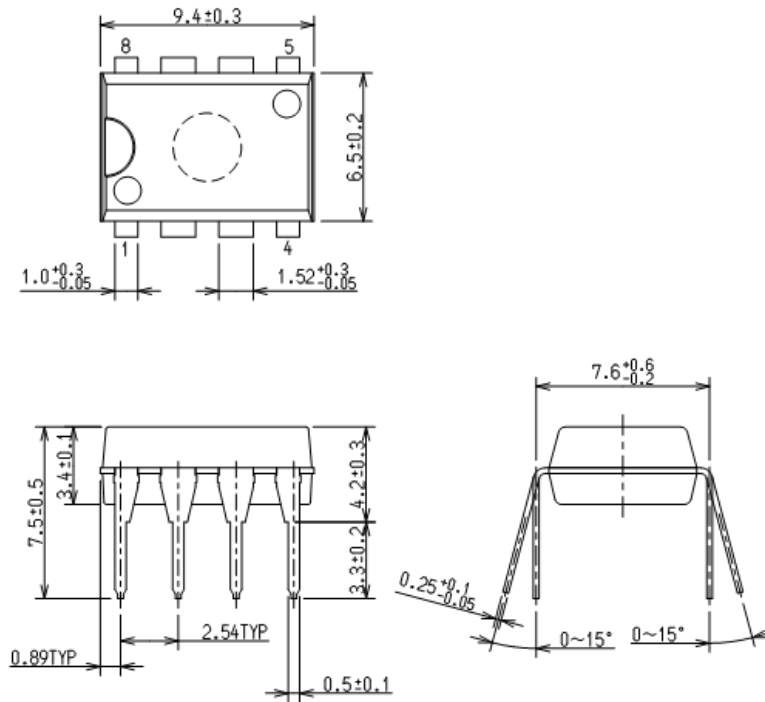


TC_STR3A400HDL_2_R1

Figure 7-1 Typical Application
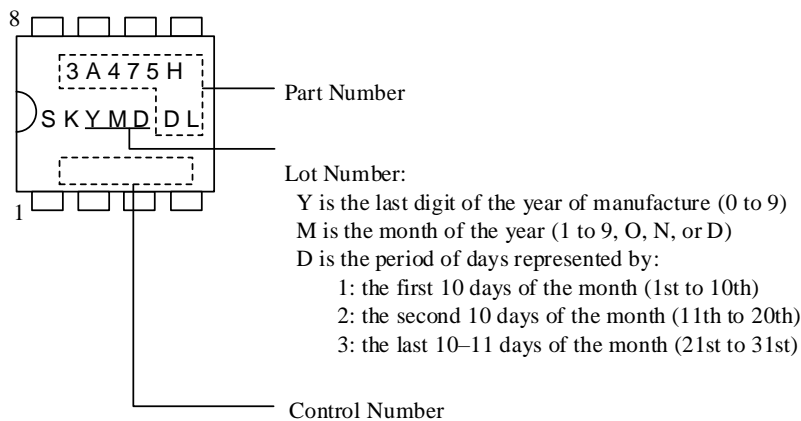
## 8. Physical Dimensions

● DIP8



**NOTES:**

● Dimensions in millimeters
● Bare lead frame: Pb-free (RoHS compliant)
● When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 °C / 10 s, 1 time
  Soldering Iron: 350 °C / 3.5 s, 1 time
  Soldering should be at a distance of at least 1.5 mm from the body of the product.

## 9. Marking Diagram



Part Number

Lot Number:
  Y is the last digit of the year of manufacture (0 to 9)
  M is the month of the year (1 to 9, O, N, or D)
  D is the period of days represented by:
    1: the first 10 days of the month (1st to 10th)
    2: the second 10 days of the month (11th to 20th)
    3: the last 10–11 days of the month (21st to 31st)

Control Number

## 10. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

### 10.1 Startup Operation
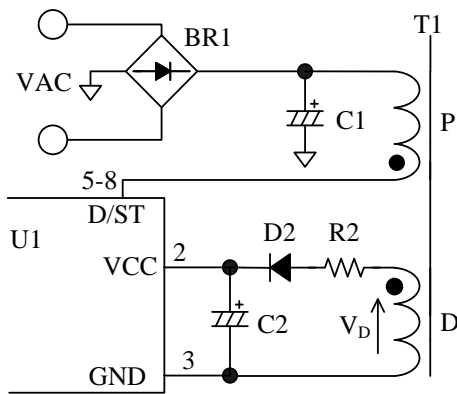
Figure 10-1 shows the circuit around the VCC pin.



Figure 10-1.    VCC Pin Peripheral Circuit

The IC incorporates the startup circuit. The circuit is connected to the D/ST pin. When D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{ST(ON)} = 47$ V, the startup circuit starts operation. During the startup process, the constant current, $I_{CC(ST)} = -2.5$ mA, charges C2 at the VCC pin. When VCC pin voltage increases to $V_{CC(ON)} = 15.0$ V, the control circuit starts switching operation. During the IC operation, the voltage rectified the auxiliary winding voltage, $V_D$, of Figure 10-1 becomes a power source to the VCC pin.

After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero. The approximate value of auxiliary winding voltage is about 18V, taking account of the winding turns of D winding so that the VCC pin voltage becomes Equation (1) within the specification of input and output voltage variation of power supply.

$$V_{CC(BIAS)}(\text{max.}) < V_{CC} < V_{CC(OVP)}(\text{min.})$$

$$\Rightarrow 10.5 \text{ (V)} < V_{CC} < 27.0 \text{ (V)} \tag{1}$$

The startup time of the IC is determined by C2 capacitor value. The approximate startup time $t_{START}$ is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left|I_{CC(ST)}\right|} \tag{2}$$

Where:
$t_{START}$ is the startup time of the IC (s), and
$V_{CC(INT)}$ is initial voltage on the VCC pin (V).

### 10.2 Undervoltage Lockout (UVLO)

Figure 10-2 shows the relationship of VCC pin voltage and circuit current $I_{CC}$. When the VCC pin voltage decreases to $V_{CC(OFF)} = 8.5$ V, the control circuit stops operation by UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.
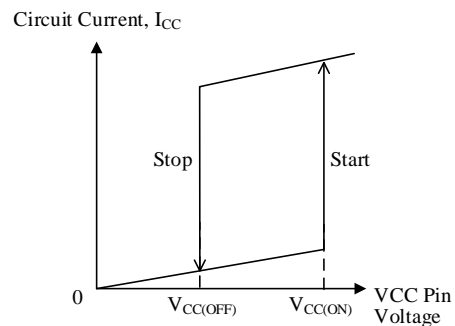


Figure 10-2.    Relationship between
VCC Pin Voltage and $I_{CC}$

### 10.3 Bias Assist Function

By the bias assist function, the startup failure is prevented. When FB pin voltage decreases to $V_{FB(OFF)} = 1.54$ V or less and VCC pin voltage decreases to the Startup Current Biasing Threshold Voltage, $V_{CC(BIAS)} = 9.6$ V, the bias assist function is activated. When the bias assist function is activated, the VCC pin voltage is kept almost constant voltage, $V_{CC(BIAS)}$ by providing the startup current, $I_{CC(ST)}$, from the startup circuit. Thus, the VCC pin voltage is kept more than $V_{CC(OFF)}$.

Since the startup failure is prevented by the bias assist function, the value of C2 connected to the VCC pin can be small. Thus, the startup time and the response time of the overvoltage protection (OVP) become shorter.

The operation of the bias assist function in startup is as follows. It is necessary to check and adjust the startup process based on actual operation in the application, so that poor starting conditions may be avoided.

Figure 10-3 shows the VCC pin voltage behavior during the startup period. After the VCC pin voltage increases to $V_{CC(ON)} = 15.0$ V at startup, the IC starts the operation. Then circuit current increases and the VCC pin voltage decreases. At the same time, the auxiliary

winding voltage, $V_D$, increases in proportion to output voltage. These are all balanced to produce the VCC pin voltage.

When the VCC pin voltage is decrease to $V_{CC(OFF)} = 8.5$ V in startup operation, the IC stops switching operation and a startup failure occurs. When the output load is light at startup, the output voltage may become more than the target voltage due to the delay of feedback circuit. In this case, the FB pin voltage is decreased by the feedback control. When the FB pin voltage decreases to $V_{FB(OFF)}$ or less, the IC stops switching operation and the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, the bias assist function is activated and the startup failure is prevented.
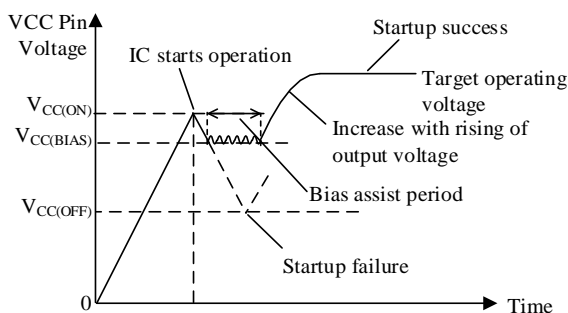


Figure 10-3. VCC Pin Voltage during Startup Period

## 10.4 Soft Start Function

Figure 10-4 shows the behavior of VCC pin voltage and drain current during the startup period.

The IC activates the soft start circuitry during the startup period. Soft start time is fixed to around 8.75 ms. during the soft start period, overcurrent threshold is increased step-wisely (7 steps). This function reduces the voltage and the current stress of a power MOSFET and the secondary side rectifier diode.

Since the leading edge blanking function (see Section 10.6) is deactivated during the soft start period, there is the case that an on time is less than the leading edge blanking time, $t_{BW} = 330$ ns.

After the soft start period, D/ST pin current, $I_D$, is limited by the overcurrent protection (OCP), until the output voltage increases to the target operating voltage. This period is given as $t_{LIM}$.

In case $t_{LIM}$ is longer than the OLP Delay Time, $t_{OLP}$, the output power is limited by the overload protection (OLP) operation.

Thus, it is necessary to adjust the value of output capacitor and the turn ratio of auxiliary winding D so that the $t_{LIM}$ is less than $t_{OLP} = 55$ ms (min.).
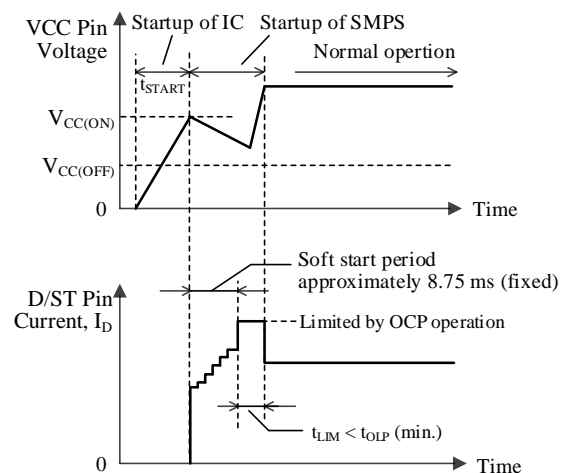


Figure 10-4. $V_{CC}$ and $I_D$ Behavior during Startup

## 10.5 Constant Output Voltage Control

The IC achieves the constant voltage control of the power supply output by using the current-mode control method, which enhances the response speed and provides the stable operation. The FB/OLP pin voltage is internally added the slope compensation at the feedback control (see Section 5. Block Diagram), and the target voltage, $V_{SC}$, is generated. The IC compares the voltage, $V_{ROCP}$, of a current detection resistor with the target voltage, $V_{SC}$, by the internal FB comparator, and controls the peak value of $V_{ROCP}$ so that it gets close to $V_{SC}$, as shown in Figure 10-5 and Figure 10-6.

● Light Load Conditions
When load conditions become lighter, the output voltage, $V_{OUT}$, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, $V_{SC}$ decreases, and the peak value of $V_{ROCP}$ is controlled to be low, and the peak drain current of $I_D$ decreases.
This control prevents the output voltage from increasing.

● Heavy Load Conditions
When load conditions become greater, the IC performs the inverse operation to that described above. Thus, $V_{SC}$ increases and the peak drain current of $I_D$ increases.
This control prevents the output voltage from decreasing.

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based

on the initial value of the drain current.

This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in Figure 10-7. This is called the subharmonics phenomenon.

In order to avoid this, the IC incorporates the Slope Compensation Function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the on-duty gets wider relative to the FB/OLP pin signal to compensate $V_{SC}$, the subharmonics phenomenon is suppressed.

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.
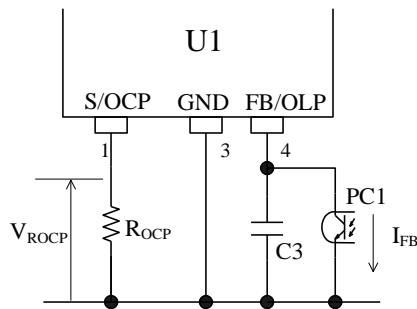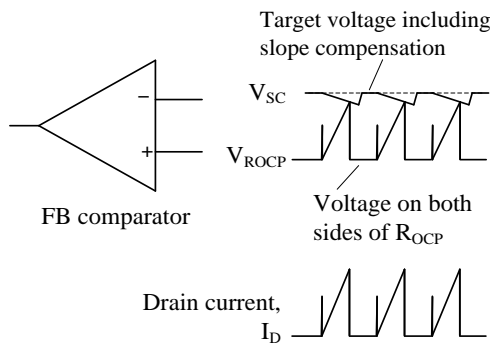


Figure 10-5.  FB/OLP Pin Peripheral Circuit



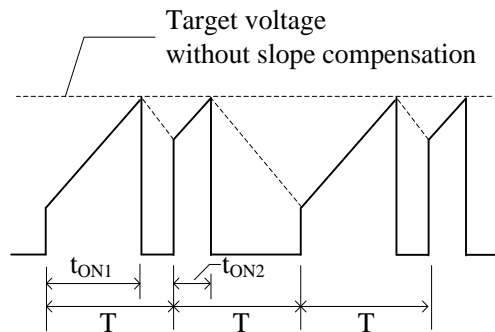Figure 10-6.  Drain Current, $I_D$, and FB Comparator Operation in Steady Operation



Figure 10-7.  Drain Current, $I_D$, Waveform in Subharmonic Oscillation

## 10.6  Leading Edge Blanking Function

The constant voltage control of output of the IC uses the peak-current-mode control method.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of a FB comparator or overcurrent protection (OCP) circuit to the steep surge current in turning on a power MOSFET. In order to prevent this response to the surge voltage in turning-on the power MOSFET, the Leading Edge Blanking, $t_{BW}$ = 330 ns is built-in. During $t_{BW}$, the OCP threshold voltage becomes $V_{OCP(LEB)}$ = 1.69 V in order not to respond to the turn-on drain current surge (see Section 10.10).

## 10.7  Random Switching Function

The IC modulates its switching frequency randomly by superposing the modulating frequency on $f_{OSC(AVG)}$ in normal operation. This function reduces the conduction noise compared to others without this function, and simplifies noise filtering of the input lines of power supply.

## 10.8  Automatic Standby Function

The IC has automatic standby function to achieve higher efficiency at light load. In order to reduce the switching loss, the automatic standby function automatically changes the oscillation mode to green mode or burst oscillation mode (see Figure 10-8).

When the output load becomes lower, FB/OLP pin voltage decreases. When the FB/OLP pin voltage decreases to $V_{FB(FDS)}$ = 3.60 V or less, the green mode is activated and the oscillation frequency starts decreasing. When the FB/OLP pin voltage becomes $V_{FB(FDE)}$ = 3.10 V, the oscillation frequency stops decreasing. At this point, the oscillation frequency becomes $f_{OSC(MIN)}$ = 30.0 kHz. When the FB/OLP pin voltage further decreases and becomes the standby operation point, the burst oscillation mode is activated. As shown in Figure 10-9, the burst oscillation mode consists of the switching period and the non-switching period. The oscillation frequency during the switching period is the Minimum Frequency, $f_{OSC(MIN)}$ = 30.0 kHz.
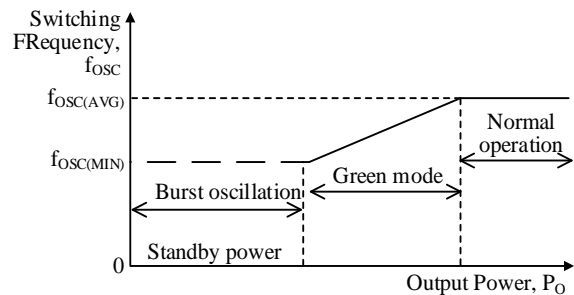


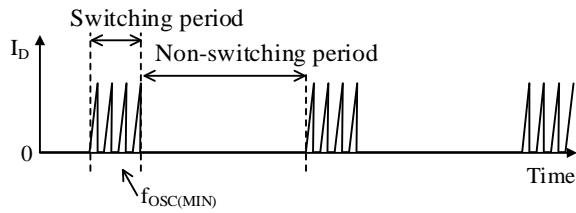Figure 10-8.  Relationship between $P_O$ and $f_{OSC}$

Figure 10-9.  Switching Waveform at Burst Oscillation

Generally, in order to improve efficiency under light load conditions, the frequency of the burst mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst mode, audible noises can be reduced.

The IC has some detection delay time. The higher the AC input voltage is, the steeper the slope of the drain current, $I_D$ is. Thus, the peak of $I_D$ at automatic standby mode becomes high at a high AC input voltage.

It is necessary to consider that the burst frequency becomes low at a high AC input.

If VCC pin voltage decreases to $V_{CC(BIAS)} = 9.6$ V during the transition to the burst mode, bias assist function is activated and stabilizes the standby mode, because the Startup Current, $I_{CC(ST)}$, is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$. However, if the bias assist function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and the secondary-side winding and/or reducing the value of R2 in Figure 11-2 (see Section 11.1).

## 10.9   Step Drive Control

Figure 10-10 shows a flyback control circuit. The both end of secondary rectification diode (D51) is generated surge voltage when a power MOSFET turns on. Thus, $V_{RM}$ of D51 should be set in consideration of the surge.

The IC optimally controls the gate drive of the internal power MOSFET (Step drive control) depending on the load condition. The step drive control reduces the surge voltage of D51 when the power MOSFET turns on (See Figure 10-11). Since $V_{RM}$ of D51 can be set to lower value than usual, the price reduction and the increasing circuit efficiency are achieved by using a diode of low $V_F$.
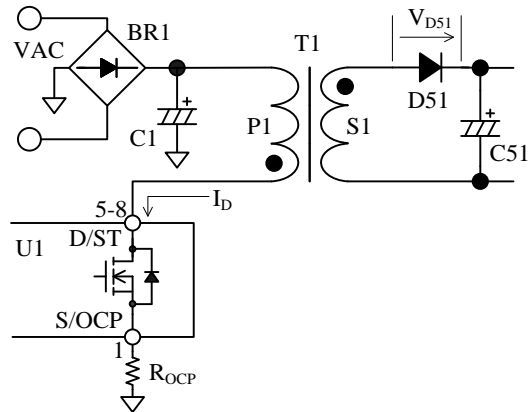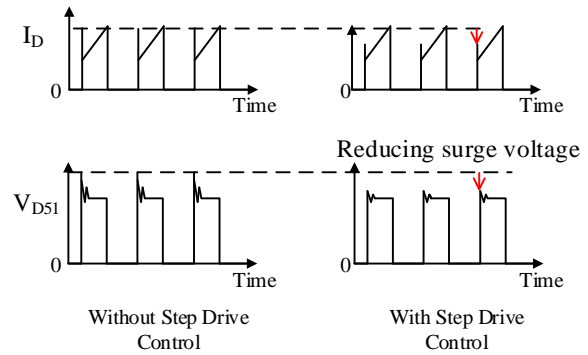


Figure 10-10.   Flyback Control Circuit



Figure 10-11.   $I_D$ and $V_{D51}$ Waveforms

## 10.10 Overcurrent Protection (OCP)

### 10.10.1 OCP Operation

The overcurrent protection (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to the OCP threshold voltage.

During the Leading Edge Blanking Time, the OCP threshold voltage becomes $V_{OCP(LEB)} = 1.69$ V which is higher than the normal OCP threshold voltage as shown in Figure 10-12. Changing to this threshold voltage prevents the IC from responding to the surge voltage in turning-on the power MOSFET. This function operates as protection at the condition such as output windings shorted or unusual withstand voltage of secondary-side rectifier diodes.

When the power MOSFET turns on, the surge voltage width of the S/OCP pin should be less than $t_{BW}$, as shown in Figure 10-12. In order to prevent surge voltage, pay extra attention to $R_{OCP}$ trace layout (see Section 11.2). In addition, if a C (RC) damper snubber of Figure 10-13 is used, reduce the capacitor value of damper snubber.
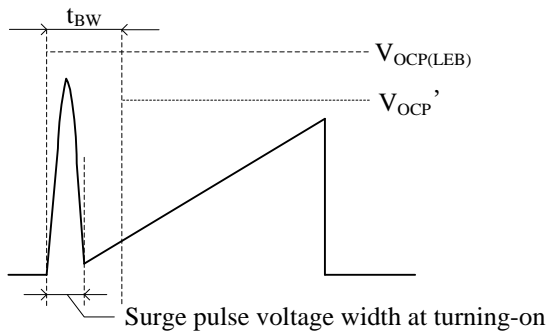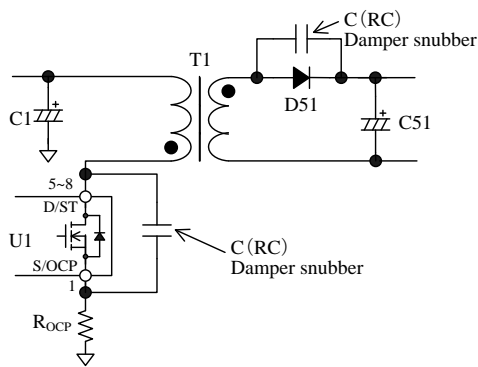
Figure 10-12.   S/OCP Pin Voltage



Figure 10-13.   Damper Snubber

## 10.10.2 OCP Input Compensation Function

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the detection voltage of actual drain peak current is, compared to $V_{OCP}$. Thus, the peak current has some variation depending on AC input voltage in the OCP state. In order to reduce the variation of peak current in the OCP state, the IC has Input Compensation Function.

This function corrects the OCP threshold voltage depending on the AC input voltage, as shown in Figure 10-14.

When the AC input voltage is low (the duty cycle is broad), the OCP threshold voltage is controlled to become high. The difference of peak drain current become small compared with the case where the AC input voltage is high (the duty cycle is narrow).

The compensation signal depends on the duty cycle . The relation between the duty cycle and the OCP threshold voltage after compensation $V_{OCP}'$ is expressed as Equation (3). When the duty cycle is broader than 36 %, the $V_{OCP}'$ becomes a constant value $V_{OCP(H)} = 0.888$ V.
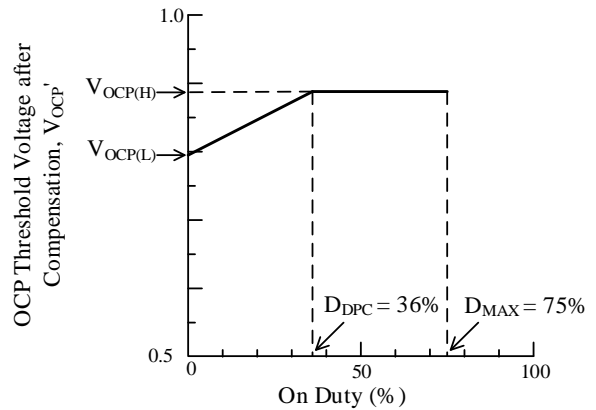


Figure 10-14.   Relationship between On Duty and Drain Current Limit after Compensation

$$V_{OCP}' = V_{OCP(L)} + DPC \times ONTime$$

$$= V_{OCP(L)} + DPC \times \frac{Duty}{f_{OSC(AVG)}} \qquad (3)$$

Where:
$V_{OCP(L)}$ is the OCP Threshold Voltage at Zero On Duty (V),
DPC is the OCP Compensation Coefficient (mV/μs),
ONTime is an on-time of power MOSFET (μs),
Duty is an duty cycle of power MOSFET (%), and
$f_{OSC(AVG)}$ is the Average PWM Switching Frequency (kHz).

## 10.10.3 Overload Protection (OLP)

Figure 10-15 shows the FB/OLP pin peripheral circuit, and Figure 10-16 shows each waveform for overload protection (OLP) operation.

When the peak drain current of $I_D$ is limited by overcurrent protection operation, the output voltage, $V_{OUT}$, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, $I_{FB}$, charges C3 connected to the FB/OLP pin and FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)} = 7.3$ V or more for the OLP delay time, $t_{OLP} = 75$ ms or more, the OLP is activated, the IC stops switching operation.

During OLP operation, the intermittent operation by VCC pin voltage repeats and reduces the stress of parts such as a power MOSFET and secondary side rectifier diodes.

When the OLP is activated, the IC stops switching operation, and the VCC pin voltage decreases.

During OLP operation, the bias assist function is disabled. When the VCC pin voltage decreases to $V_{CC(OFF)SKP}$ (about 9 V), the startup current flows, and

the VCC pin voltage increases. When the VCC pin voltage increases to $V_{CC(ON)}$, the IC starts operation, and the circuit current increases. After that, the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(OFF)} = 8.5$ V, the control circuit stops operation.

Skipping the UVLO operation of $V_{CC(OFF)}$ (see Section 10.2), the intermittent operation makes the non-switching interval longer and restricts the temperature rise of the power MOSFET.

When the abnormal condition is removed, the IC returns to normal operation automatically.
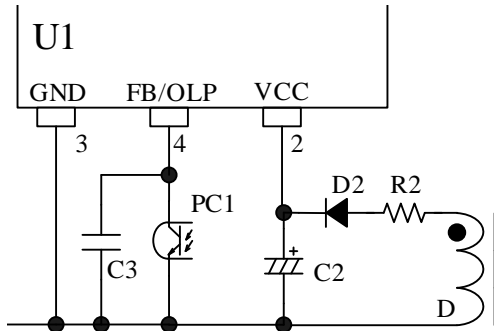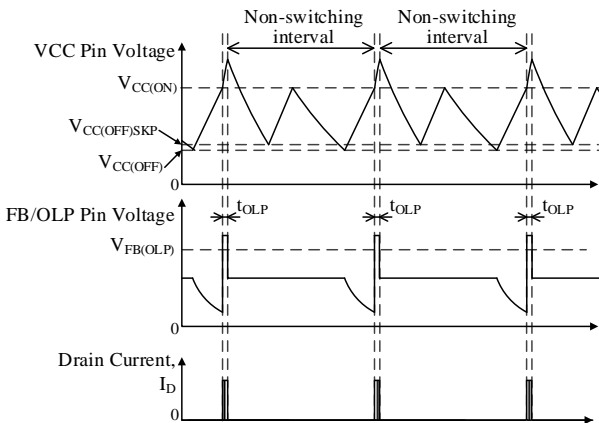


Figure 10-15.    FB/OLP Pin Peripheral Circuit



Figure 10-16.    OLP Operational Waveforms

## 10.10.4 Overvoltage Protection (OVP)

When a voltage between the VCC pin and the GND pin increases to $V_{CC(OVP)} = 29.1$ V or more, overvoltage protection (OVP) is activated, and the IC stops switching operation. During OVP operation, the bias assist function is disabled, the intermittent operation by the UVLO is repeated (see Section 10.10.3). When the fault condition is removed, the IC returns to normal operation automatically (see Figure 10-17).

When VCC pin voltage is provided by using auxiliary winding of transformer, the VCC pin voltage is proportional to output voltage. Thus, the VCC pin can detect the overvoltage conditions such as output voltage

detection circuit open. The approximate value of output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (4).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 29.1 \ (V) \tag{4}$$

Where:

$V_{OUT(NORMAL)}$ is the output voltage in normal operation, and

$V_{CC(NORMAL)}$ is the VCC pin voltage in normal operation.
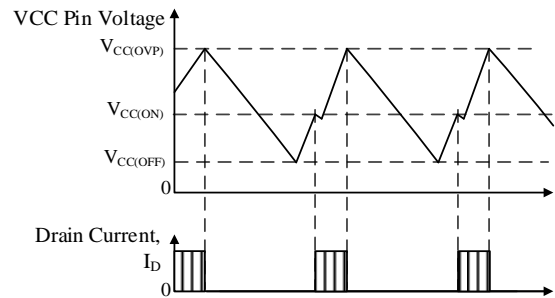


Figure 10-17.    OVP Operational Waveforms

## 10.10.5 Thermal Shutdown (TSD)

When the temperature of control circuit increases to $T_{J(TSD)} = 145$ °C or more, thermal shutdown (TSD) is activated.

Figure 10-18 shows the TSD operational waveforms. TSD has the thermal hysteresis.
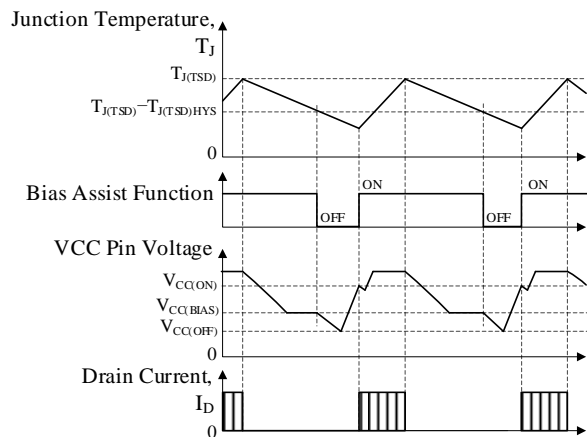


Figure 10-18.    TSD Operational Waveforms

When TSD is activated, and the IC stops switching operation. After that, VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, the bias assist function is activated and the VCC pin voltage is

kept to over the $V_{CC(OFF)}$.

When the temperature reduces to less than $T_{J(TSD)}-T_{J(TSD)HYS}$, the bias assist function is disabled and the VCC pin voltage decreases to $V_{CC(OFF)}$. At that time, the IC stops operation and reverts to the state before startup. After that, the startup circuit is activated, the VCC pin voltage increases to $V_{CC(ON)}$, and the IC starts switching operation again.

In this way, the intermittent operation by the TSD and the UVLO is repeated while there is an excess thermal condition.

When the fault condition is removed, the IC returns to normal operation automatically.

## 11.  Design Notes

### 11.1  External Components

Take care to use properly rated, including derating as necessary and proper type of components.
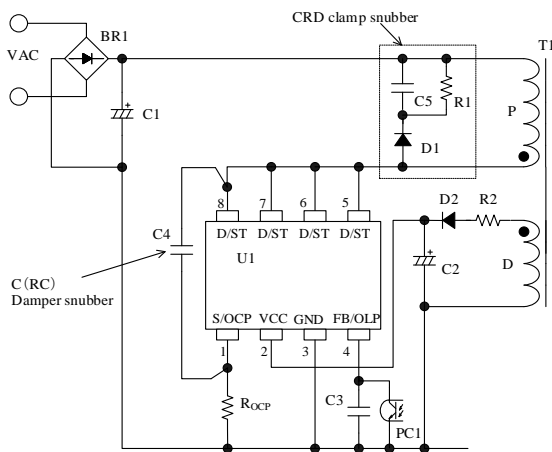
Figure 11-1.   The IC Peripheral Circuit

### 11.1.1  Input and Output Electrolytic Capacitor

Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

### 11.1.2  S/OCP Pin Peripheral Circuit

In Figure 11-1, $R_{OCP}$ is the resistor for the current detection. Since high frequency switching current flows to $R_{OCP}$, choose the resistor of low inductance and high power dissipation capability.

### 11.1.3  VCC Pin Peripheral Circuit

The value of C2 in Figure 11-1 is generally recommended to be 10 µF to 47 µF (see Section 10.1 Startup Operation, because the startup time is determined by the value of C2)

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, $I_{OUT}$ (see Figure 11-2), and the overvoltage protection (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off. For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 11-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.
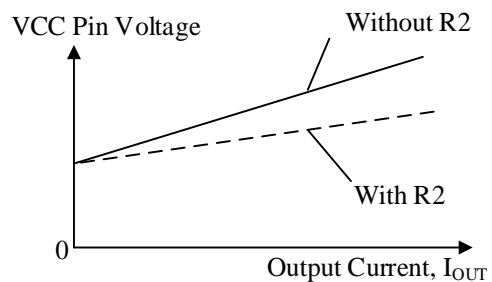
Figure 11-2.   Variation of VCC Pin Voltage and Power

### 11.1.4  FB/OLP Pin Peripheral Circuit

C3 (see Figure 11-1) is for high frequency noise rejection and phase compensation, and should be connected close to the FB/OLP pin and the GND pin. The value of C3 is recommended to be about 2200 pF to 0.01 µF, and should be selected based on actual operation in the application.

### 11.1.5  Snubber Circuit

In case the serge voltage of $V_{DS}$ is large, the circuit should be added as follows (see Figure 11-1);

● A clamp snubber circuit of a capacitor-resistor- diode (CRD) combination should be added on the primary winding P.
● A damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.

In case the damper snubber circuit is added, this components should be connected near D/ST pin and S/OCP pin.

### 11.1.6 Peripheral Circuit of Secondary-side Shunt Regulator

Figure 11-3 shows the secondary-side detection circuit with the standard shunt regulator IC (U51).

C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047 μF to 0.47 μF and 4.7 kΩ to 470 kΩ, respectively. They should be selected based on actual operation in the application.
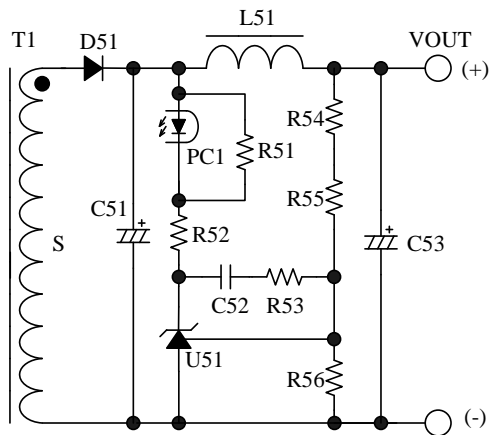


Figure 11-3.   Peripheral Circuit of Secondary-side Shunt Regulator (U51)

### 11.1.7 Transformer

Apply proper design margin to core temperature rise by core loss and copper loss.
Because the switching currents contain high frequency currents, the skin effect may become a consideration.
Choose a suitable wire gauge in consideration of the RMS current and a current density of 4 to 6 A/mm$^2$.
If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

● Increase the number of wires in parallel.
● Use litz wires.
● Thicken the wire gauge.

In the following cases, the surge of VCC pin voltage becomes high.

● The surge voltage of primary main winding, P, is high (low output voltage and high output current power supply designs)
● The winding structure of auxiliary winding, D, is susceptible to the noise of winding P.

When the surge voltage of winding D is high, the VCC pin voltage increases and the overvoltage protection (OVP) may be activated. In transformer design, the following should be considered;

● The coupling of the winding P and the secondary output winding S should be maximized to reduce the leakage inductance.
● The coupling of the winding D and the winding S should be maximized.
● The coupling of the winding D and the winding P should be minimized.

In the case of multi-output power supply, the coupling of the secondary-side stabilized output winding, S1, and the others (S2, S3···) should be maximized to improve the line-regulation of those outputs
Figure 11-4 shows the winding structural examples of two outputs.

● Winding structural example (a):
S1 is sandwiched between P1 and P2 to maximize the coupling of them for surge reduction of P1 and P2. D is placed far from P1 and P2 to minimize the coupling to the primary for the surge reduction of D.

● Winding structural example (b)
P1 and P2 are placed close to S1 to maximize the coupling of S1 for surge reduction of P1 and P2.。
D and S2 are sandwiched by S1 to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces the surge of D, and improves the line-regulation of outputs.
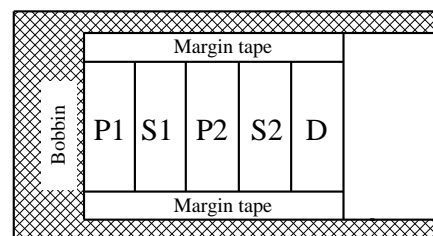


Winding structural example (a)
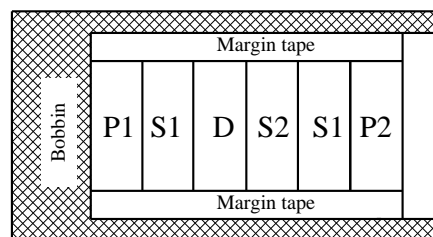


Winding structural example (b)

Figure 11-4.   Winding Structural Examples

## 11.2 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace. In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 11-5 shows the circuit design example.

(1) Main Circuit Trace Layout

This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground Trace Layout

Since the operation of the IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 11-5 as close to the $R_{OCP}$ pin as possible.

(3) VCC Trace Layout:

This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C2 and the IC are distant from each other, placing a capacitor such as film capacitor $C_f$ (about 0.1 μF to 1.0 μF) close to the VCC pin and the GND pin is recommended.

(4) $R_{OCP}$ Trace Layout

$R_{OCP}$ should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 11-5) which is close to the base of $R_{OCP}$.

(5) FB/OLP Trace Layout

The components connected to FB/OLP pin should be as close to FB/OLP pin as possible. The trace between the components and FB/OLP pin should be as short as possible.

(6) Secondary Rectifier Smoothing Circuit Trace Layout:

This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(7) Thermal Considerations

Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.

Since the copper area under the IC and the D/ST pin trace act as a heatsink, its traces should be as wide as possible.
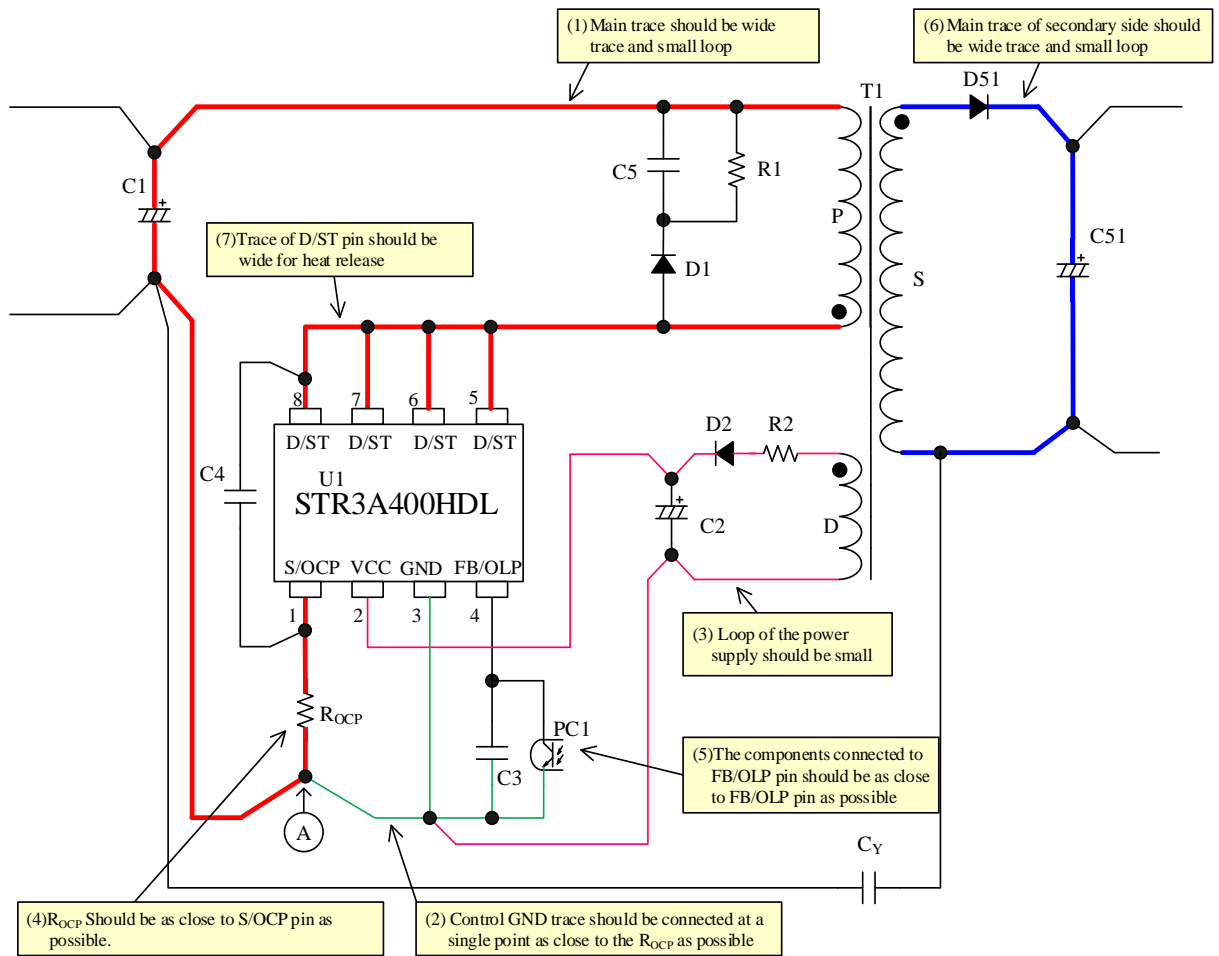
Figure 11-5.   Peripheral Circuit Example Around the IC

## 12. Pattern Layout Example

The following show the two outputs PCB pattern layout example and the schematic of circuit using STR3A475HDL series. The PCB pattern layout example is made usable to other ICs in common. The parts in Figure 12-2 are only used.
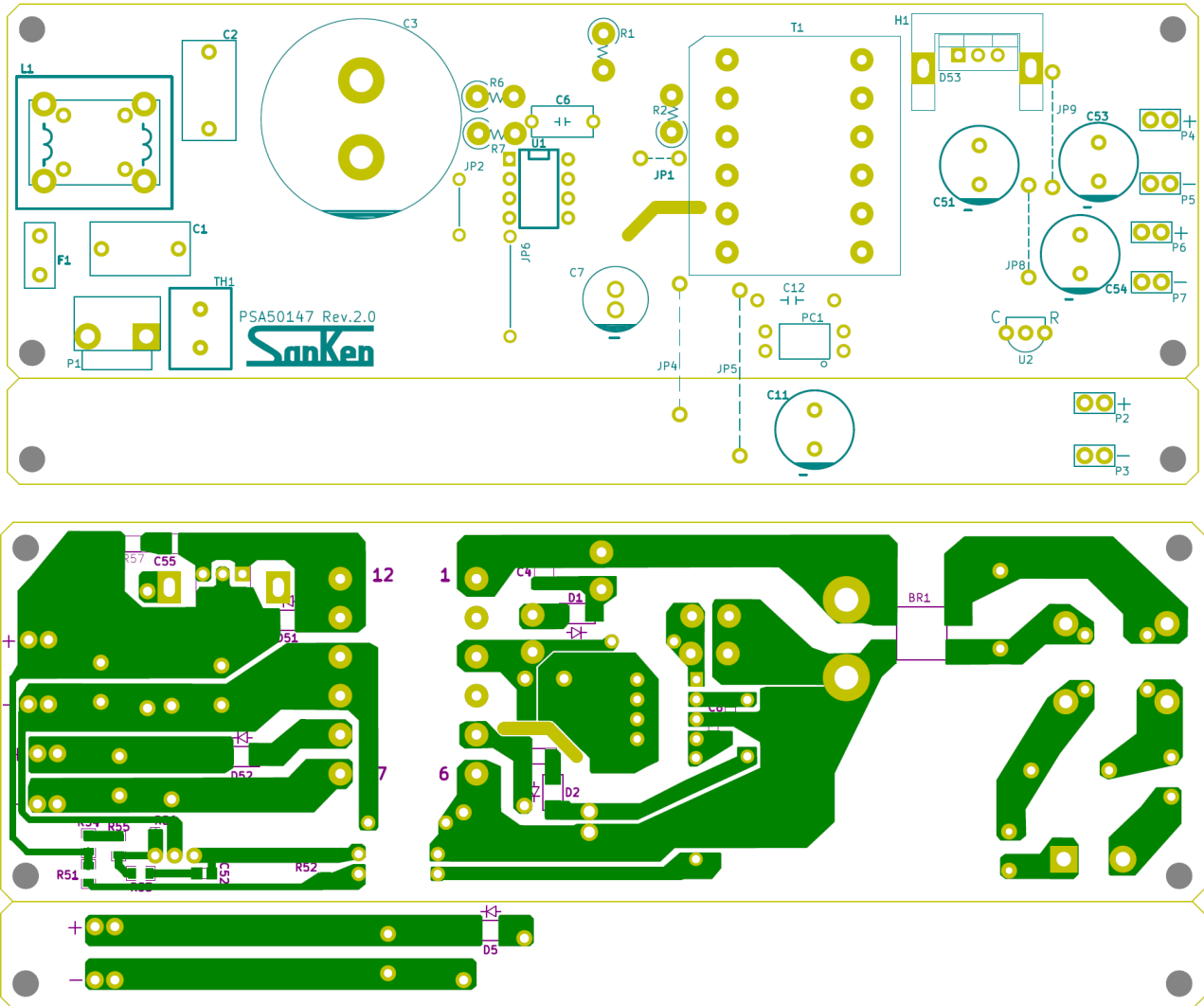


Figure 12-1.    PCB Circuit Trace Layout Example
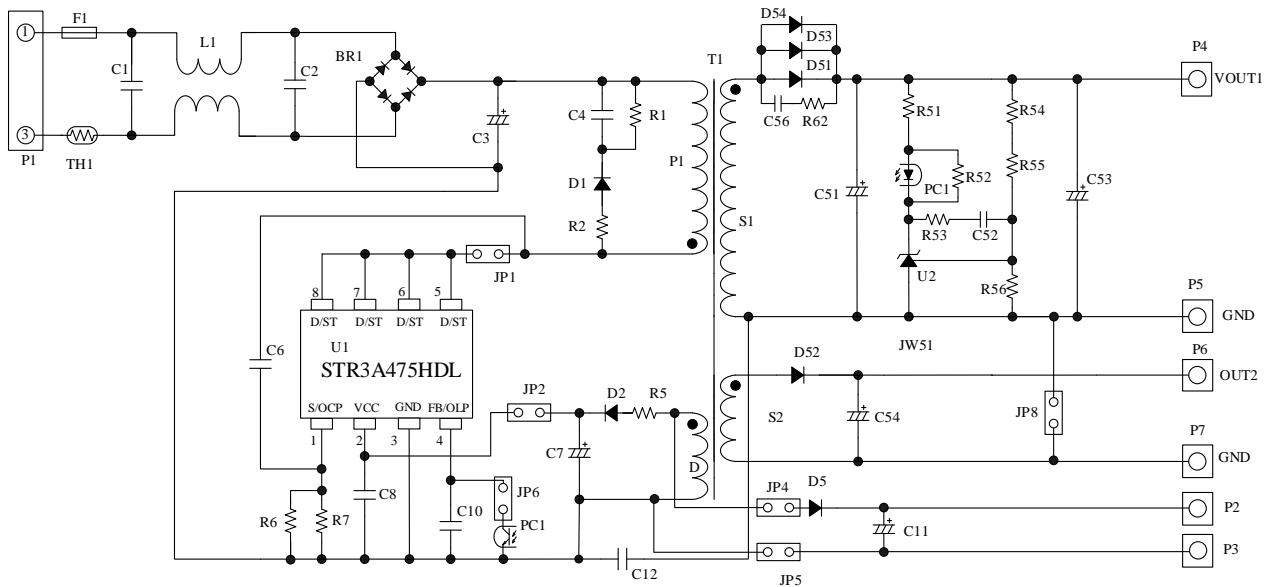
Figure 12-2.    Circuit Schematic for PCB Circuit Trace Layout

## 13.   Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

● Power Supply Specification

| IC | STR3A475HDL |
|---|---|
| Input voltage | 85VAC to 265VAC |
| Maximum output power | 34.8 W (40.4 W peak) |
| Output 1 | 14 V / 2.2 A (2.6 A peak) |
| Output 2 | 8 V / 0.5 A |

● Circuit Schematic
See Figure 12-2

● Bill of Materials

| Symbol | Part type | Ratings[1] | Recommended Sanken Parts | Symbol | Part type | Ratings[1] | Recommended Sanken Parts |
|---|---|---|---|---|---|---|---|
| F1 | Fuse | AC 250 V, 3 A | | BR1 | General | 1000 V, 1.5 A | |
| L1[2] | CM inductor | 10 mH | | L51 | Inductor | Short | |
| TH1[2] | NTC thermistor | Short | | D51 | | Open | |
| D1 | General | 800 V, 1.2 A | SARS05 | D52 | Schottky | 60 V, 1.5 A | SJPB-H6 |
| D2 | Fast recovery | 200 V, 1 A | SJPL-D2 | D53 | Schottky | 100V, 10A | FMEN-210A |
| D5 | Fast recovery | Open | | D54 | | Open | |
| C1[2] | Film, X2 | 0.1 μF, 275 V | | C51[2] | Electrolytic | 680 μF, 25 V | |
| C2[2] | Electrolytic | Open | | C52[2] | Ceramic | 0.1 μF, 50 V | |
| C3 | Electrolytic | 100 μF, 450 V | | C53[2] | Electrolytic | 680 μF, 25 V | |
| C4 | Ceramic | 1000 pF, 2 kV | | C54 | Electrolytic | 470 μF, 16 V | |
| C6[2] | Ceramic | 15 pF, 2 kV | | C56[2] | Ceramic | Open | |
| C7 | Electrolytic | 22 μF, 50 V | | R51 | General | 1.8kΩ | |
| C8[2] | Ceramic | Open | | R52 | General | 1.5 kΩ | |
| C10[2] | Ceramic | 2200 pF | | R53[2] | General | 10 kΩ | |
| C11 | Electrolytic | Open | | R54[2] | General | 6.8 kΩ | |
| C12 | Ceramic, Y1 | 2200 pF, 250 V | | R55 | General, 1% | 39 kΩ | |
| R1[3] | Metal oxide | 330 kΩ, 1 W | | R56 | General, 1% | 10 kΩ | |
| R2[2] | General | 47 Ω, 1 W | | JP1 | | Short | |
| R5[2] | General | 10 Ω | | JP2 | | Short | |
| R6[2] | General | 0.47 Ω, 1 W | | JP4 | | Open | |
| R7[2] | General | Open | | JP5 | | Open | |
| PC1 | Photo-coupler | PC123 or equiv | | JP6 | | Short | |
| U1 | IC | — | STR3A475HDL | JP8 | | Short | |
| T1 | Transformer | See the specification | | U2 | Shunt regulator | $V_{REF} = 2.5$ V TL431 or equiv | |

[1] Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.

[2] It is necessary to be adjusted based on actual operation in the application.

[3] Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series to reduce applied voltage to each of them, according to the requirement of the application.

● Transformer Specification
Primary inductance, $L_P$: 460 μH
Core size: EER-28S
Al-value: 373 nH/N$^2$ (Center gap of about 0.25 mm)
Winding specification

| Winding | Symbol | Number of turns (T) | Wire diameter (mm) | Construction |
|---|---|---|---|---|
| Primary winding | P1 | 18 | φ 0.30 | Single-layer, solenoid winding |
| Primary winding | P2 | 18 | φ 0.30 | Single-layer, solenoid winding |
| Auxiliary winding | D | 6 | φ 0.20 | Space winding |
| Output 1 winding | S1-1 | 2 | φ 0.4 × 2 | Solenoid winding |
| Output 1 winding | S1-2 | 2 | φ 0.4 × 2 | Solenoid winding |
| Output 2 winding | S2-1 | 3 | φ 0.4 × 2 | Solenoid winding |
| Output 2 winding | S2-2 | 3 | φ 0.4 × 2 | Solenoid winding |
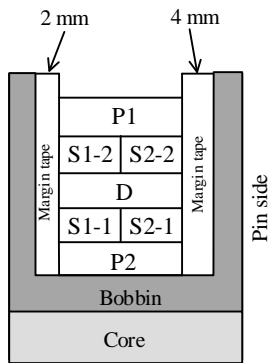
Cross-section view
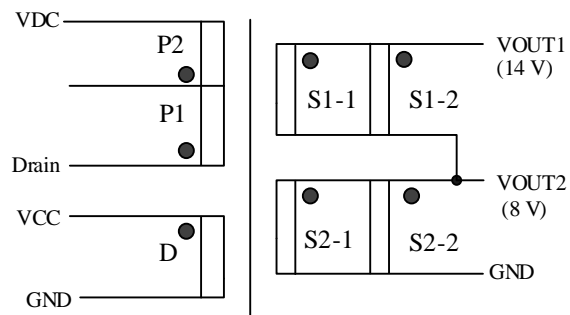
●: Start at this pin

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