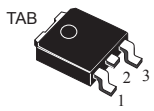
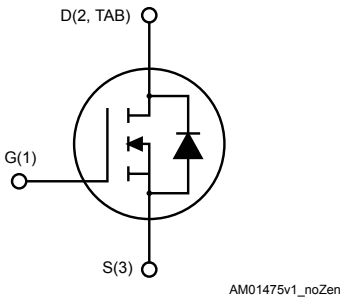
Automotive-grade N-channel 75 V, 18 mΩ, 40 A, STripFET™ II Power MOSFET in a DPAK package



DPAK



Features

Type	V_{DS}	$R_{DS(on)}$ max.	I_D
STD45NF75T4	75 V	24 mΩ	40 A

- AEC-Q101 qualified
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET series has been developed using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status link
STD45NF75T4

Product summary	
Order code	STD45NF75T4
Marking	D45NF75
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	75	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	40(1)	A
	Drain current (continuous) at T_C = 100 °C	30	A
I_{DM}(2)	Drain current (pulsed)	160	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	W
E_{AS}(3)	Single-pulse avalanche energy	500	mJ
dv/dt(4)	Peak diode recovery voltage slope	20	V/ns
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Operating junction temperature range		

1. *This value is limited by package.*
2. *Pulse width is limited by safe operating area.*
3. *Starting T_J = 25 °C, I_D = 20 A, V_{DD} = 40 V*
4. *I_{SD} ≤ 40 A, di/dt ≤ 800 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ T_{JMAX}*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.2	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb(1)	50	°C/W

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board.*

2 Electrical characteristics

T_{CASE} = 25 °C unless otherwise specified

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	75			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 75 V			1	µA
		V_{GS} = 0 V, V_{DS} = 75 V, T_C = 125 °C(1)			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DD} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 20 A		18	24	mΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1760	-	pF
C_{oss}	Output capacitance		-	360	-	pF
C_{rss}	Reverse transfer capacitance		-	140	-	pF
Q_g	Total gate charge	V_{DD} = 60 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	60	80	nC
Q_{gs}	Gate-source charge		-	13	-	nC
Q_{gd}	Gate-drain charge		-	23	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 37 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	15	-	ns
t_r	Rise time		-	40	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
t_f	Fall time		-	10	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		40	A
I_{SDM}(1)	Source-drain current (pulsed)		-		160	A
V_{SD}(2)	Forward on voltage	I_{SD} = 40 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 40 A, di/dt = 100 A/µs, V_{DD} = 30 V, T_J = 150 °C (see Figure 17. Switching time waveform)	-	120		ns
Q_{rr}	Reverse recovery charge		-	410		nC
I_{RRM}	Reverse recovery current		-	7.5		A

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

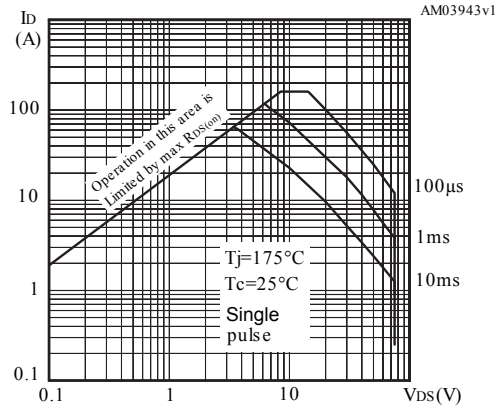


Figure 2. Thermal impedance

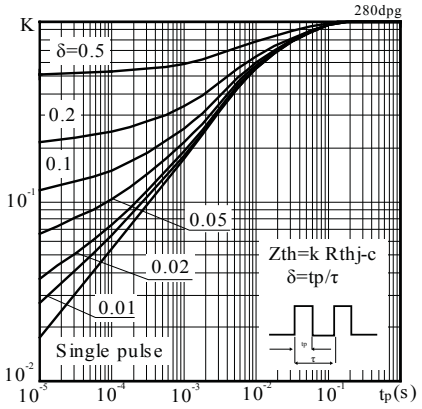


Figure 3. Output characteristics

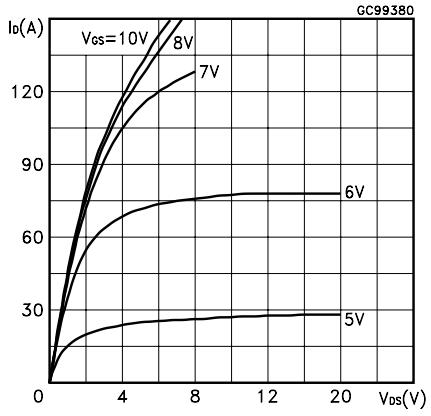


Figure 4. Transfer characteristics

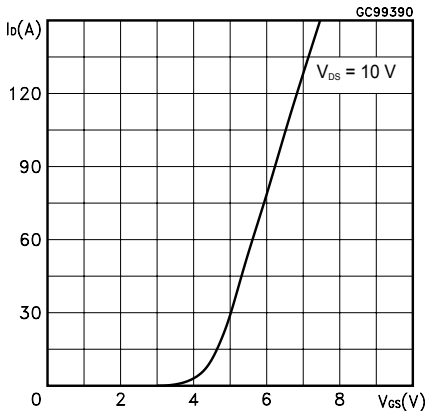


Figure 5. Static drain-source on-resistance

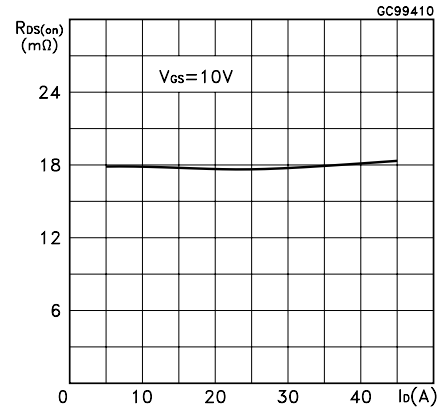


Figure 6. Gate charge vs gate-source voltage

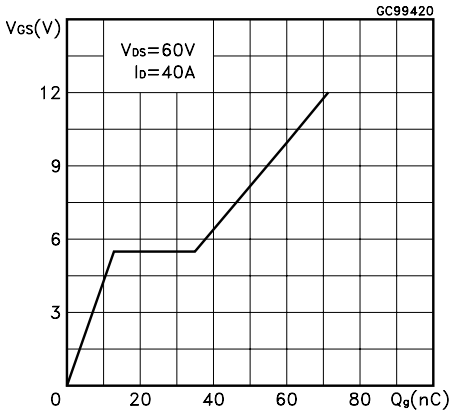


Figure 7. Capacitance variations

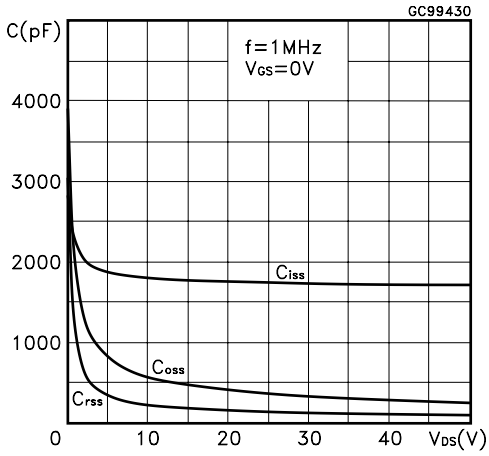


Figure 8. Normalized gate threshold voltage vs temperature

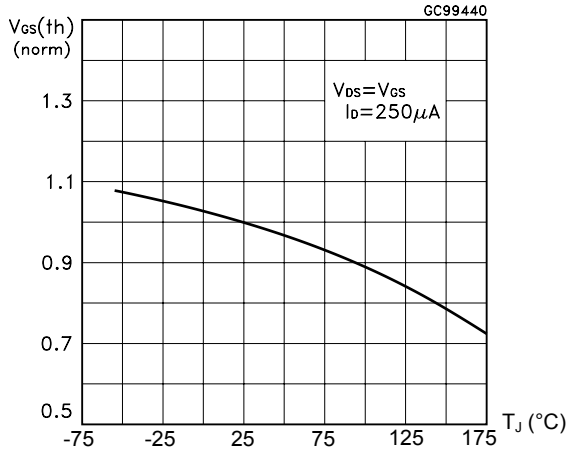


Figure 9. Normalized on-resistance vs temperature

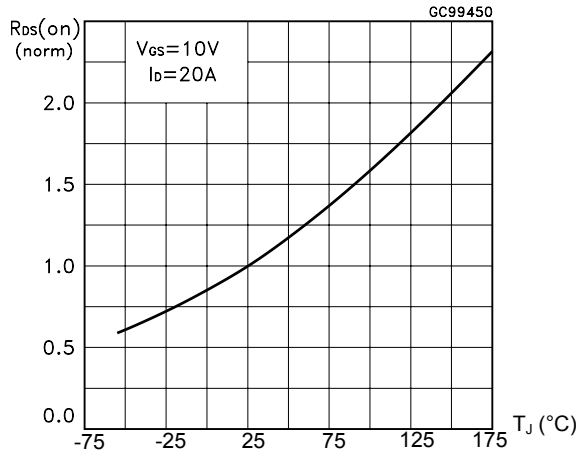


Figure 10. Source-drain diode forward characteristics

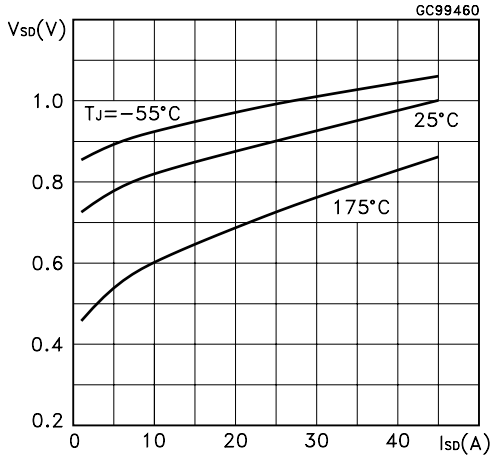
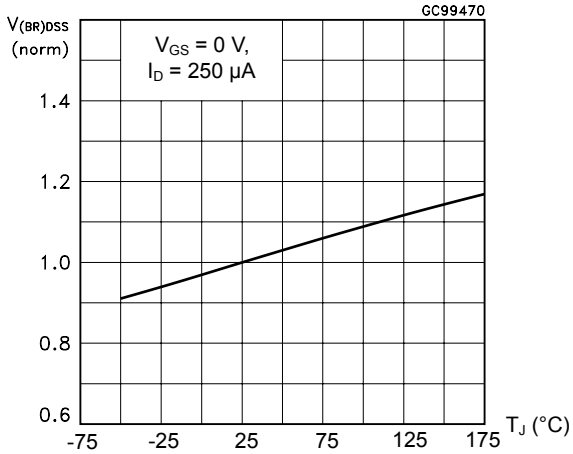


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 12. Test circuit for resistive load switching times

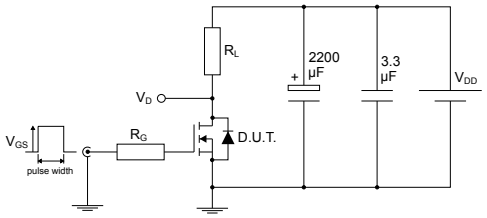


Figure 13. Test circuit for gate charge behavior

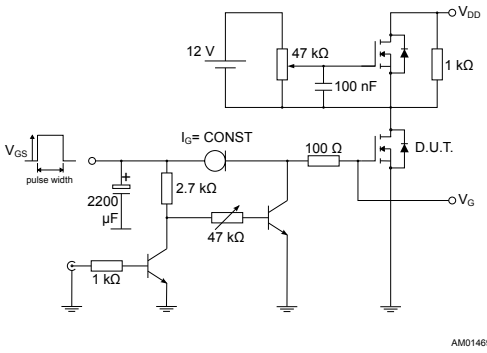


Figure 14. Test circuit for inductive load switching and diode recovery times

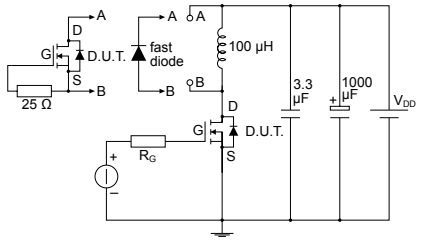


Figure 15. Unclamped inductive load test circuit

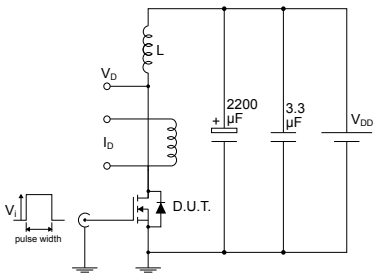


Figure 16. Unclamped inductive waveform

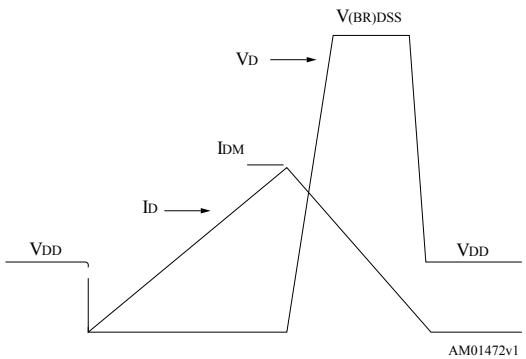
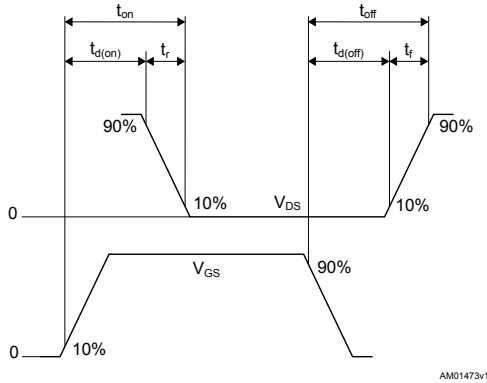


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 18. **DPAK (TO-252) type A2 package outline**

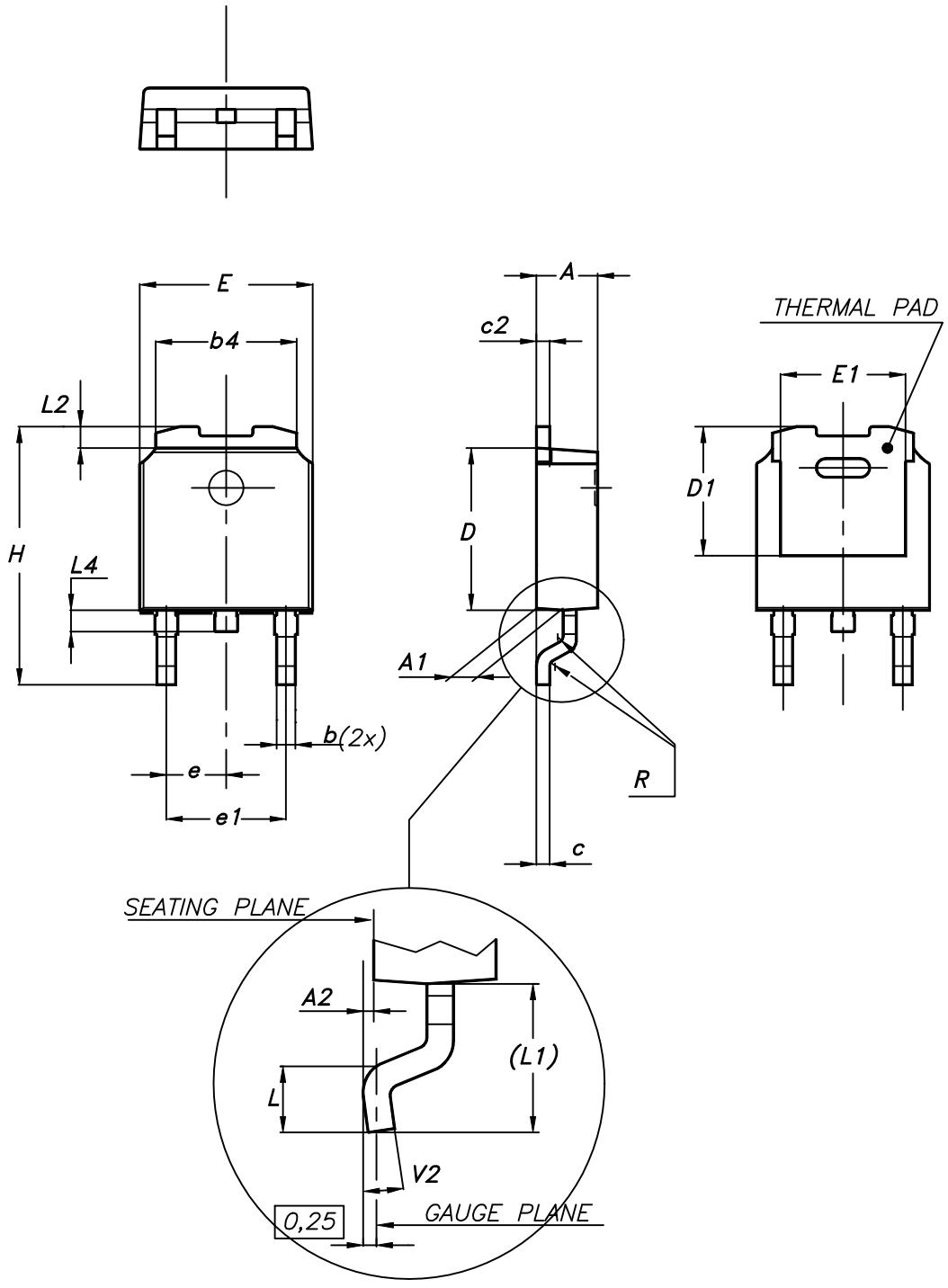
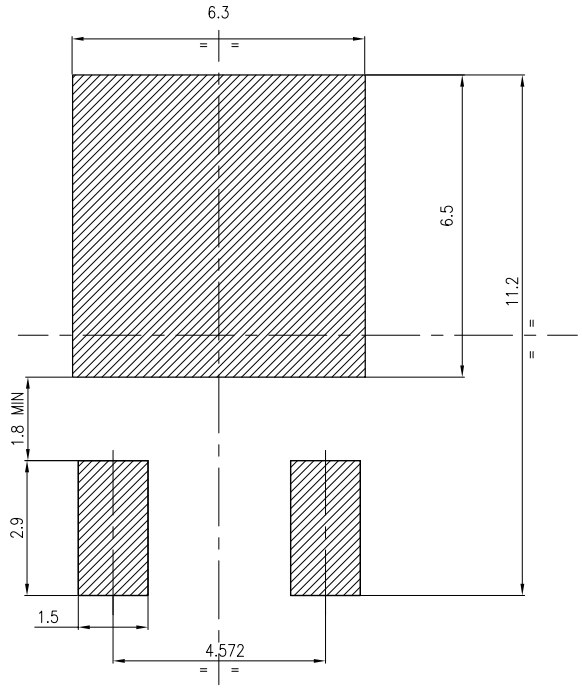


Table 7. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 19. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



4.2 DPAK (TO-252) packing information

Figure 20. **DPAK (TO-252) tape outline**

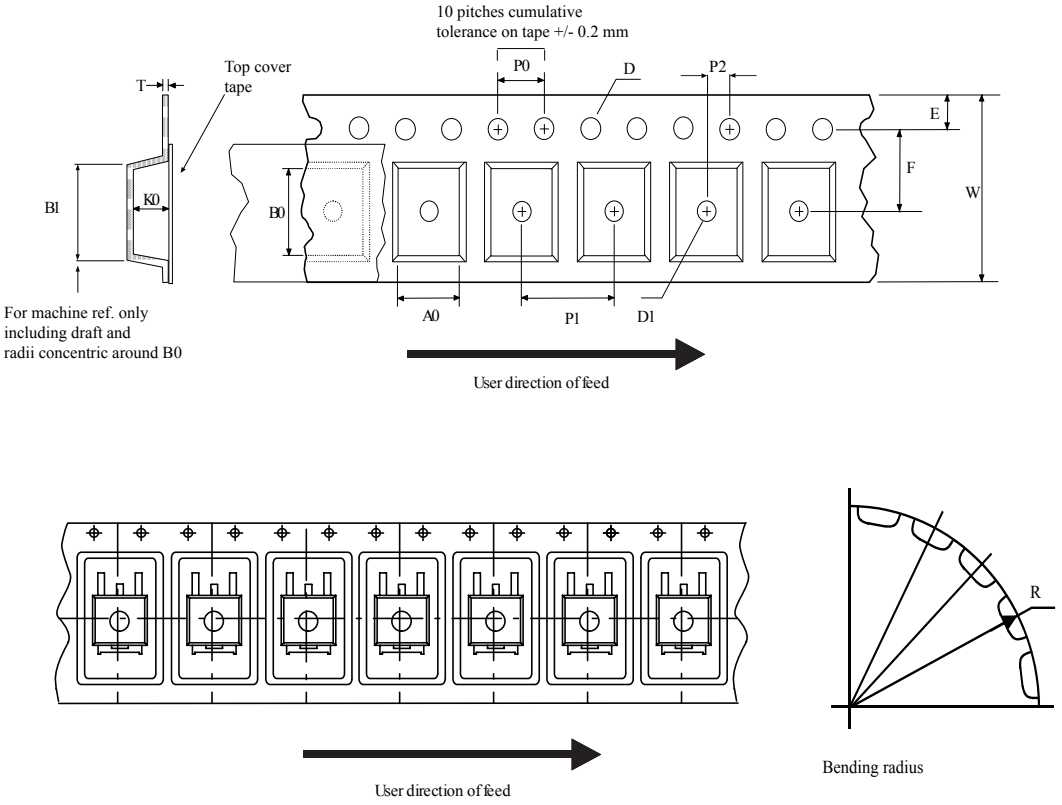


Figure 21. **DPAK (TO-252) reel outline**

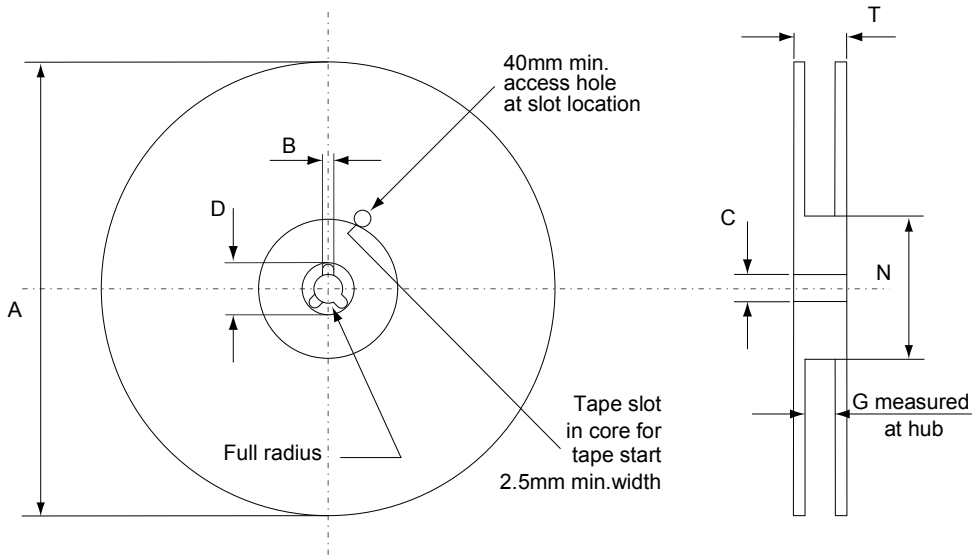


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Table 8. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 9. **Document revision history**

Date	Version	Changes
22-Jun-2004	1	Preliminary version
09-Sep-2004	2	Complete version
11-Jul-2006	3	New template, no content change
20-Feb-2007	4	Typo mistake on page 1
20-May-2009	5	*Figure 2* and *Figure 3* have been updated
03-Oct-2018	6	Updated information on cover page. Updated Section 4 Package information. Minor text changes

Contents