

N-Channel Power MOSFET

900V, 7A, 1.9Ω

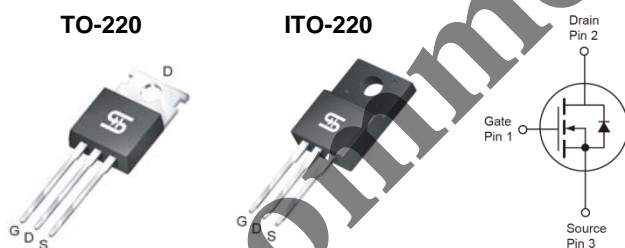
FEATURES

- Low RDS(on) 1.9Ω (Max.)
- Low gate charge typical @49nC (Typ.)
- Improve dV/dt capability
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V _{DS}	900	V
R _{DS(on)} (max)	1.9	Ω
Q _g	49	nC

APPLICATION

- Power Supply
- Lighting



ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)				
PARAMETER	SYMBOL	TO-220	ITO-220	UNIT
Drain-Source Voltage	V _{DS}	900		V
Gate-Source Voltage	V _{GS}	±30		V
Continuous Drain Current (Note 1)	I _D	T _C = 25°C		A
		T _C = 100°C		A
Pulsed Drain Current (Note 2)	I _{DM}	28		A
Total Power Dissipation @ T _C = 25°C	P _{DTOT}	250	40.3	W
Single Pulsed Avalanche Energy (Note 3)	E _{AS}	106		mJ
Single Pulsed Avalanche Current (Note 3)	I _{AS}	7		A
Operating Junction and Storage Temperature Range	T _J , T _{STG}	- 55 to +150		°C

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	TO-220	ITO-220	UNIT
Junction to Case Thermal Resistance	R _{θJC}	0.5	3.1	°C/W
Junction to Ambient Thermal Resistance	R _{θJA}	62.5		°C/W

Notes: R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. R_{θJA} is guaranteed by design while R_{θCA} is determined by the user's board design. R_{θJA} shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	900	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2	--	4	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 900V, V_{GS} = 0V$	I_{DSS}	--	--	10	μA
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 3.5A$	$R_{DS(on)}$	--	1.52	1.9	Ω
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 720V, I_D = 7A,$ $V_{GS} = 10V$	Q_g	--	49	--	nC
Gate-Source Charge		Q_{gs}	--	7	--	
Gate-Drain Charge		Q_{gd}	--	20	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	1969	--	pF
Output Capacitance		C_{oss}	--	133	--	
Reverse Transfer Capacitance		C_{rss}	--	11	--	
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 380V,$ $R_{GEN} = 25\Omega,$ $I_D = 10A, V_{GS} = 10V,$	$t_{d(on)}$	--	39	--	ns
Turn-On Rise Time		t_r	--	38	--	
Turn-Off Delay Time		$t_{d(off)}$	--	155	--	
Turn-Off Fall Time		t_f	--	45	--	
Source-Drain Diode (Note 4)						
Forward On Voltage	$I_S = 10A, V_{GS} = 0V$	V_{SD}	--	--	1.4	V
Reverse Recovery Time	$I_S = 7A,$ $di_f/dt = 100A/\mu s$	t_{rr}	--	464	--	ns
Reverse Recovery Charge		Q_{rr}	--	4.7	--	μC

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. $L = 4.1mH, I_{AS} = 7A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
100% Eas Test Condition: $L = 1mH, I_{AS} = 3.5A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

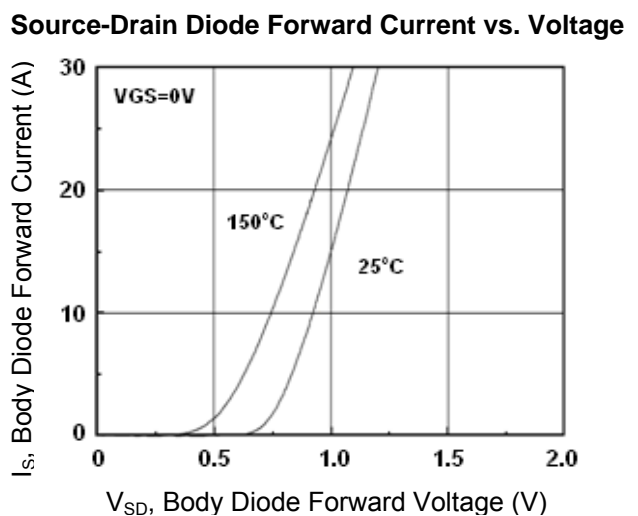
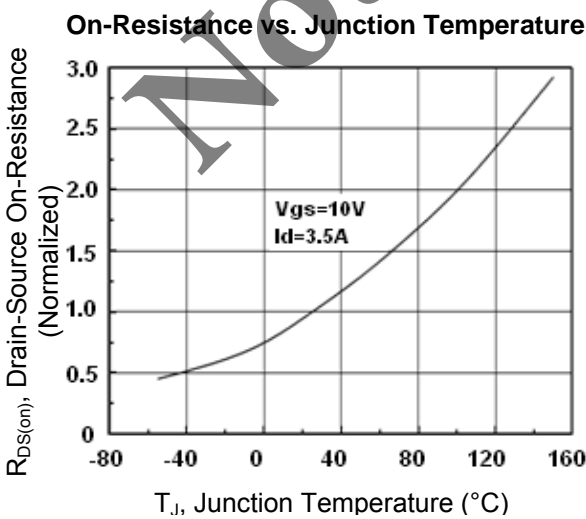
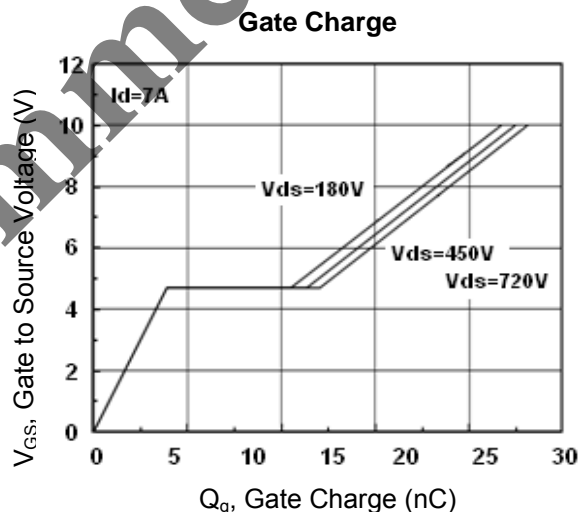
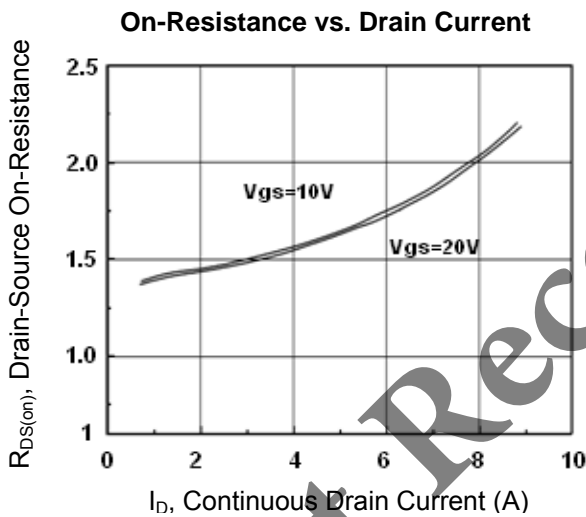
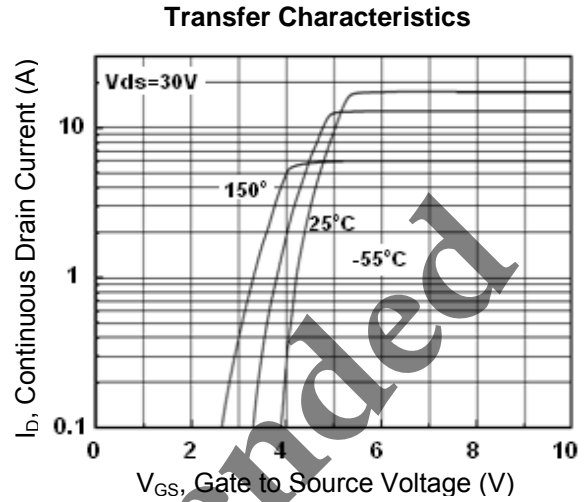
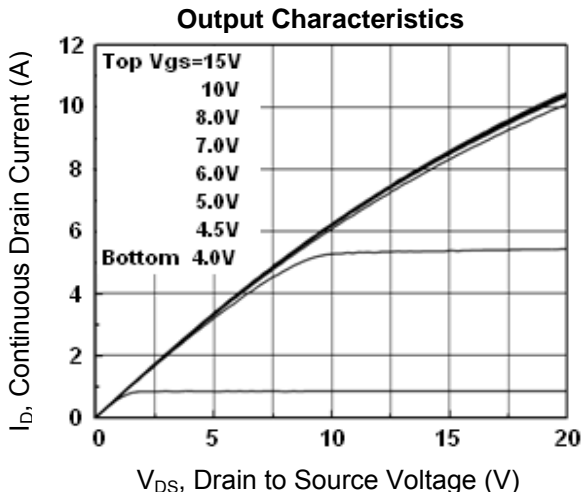
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM7N90CZ C0G	TO-220	50pcs/Tube
TSM7N90CI C0G	ITO-220	50pcs/Tube

Not Recommended

CHARACTERISTICS CURVES

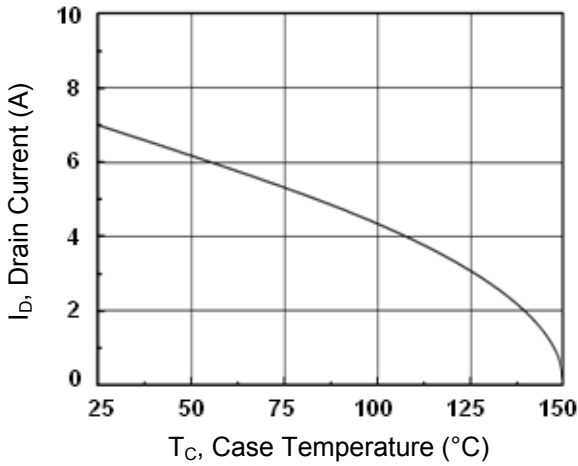
($T_c = 25^\circ\text{C}$ unless otherwise noted)



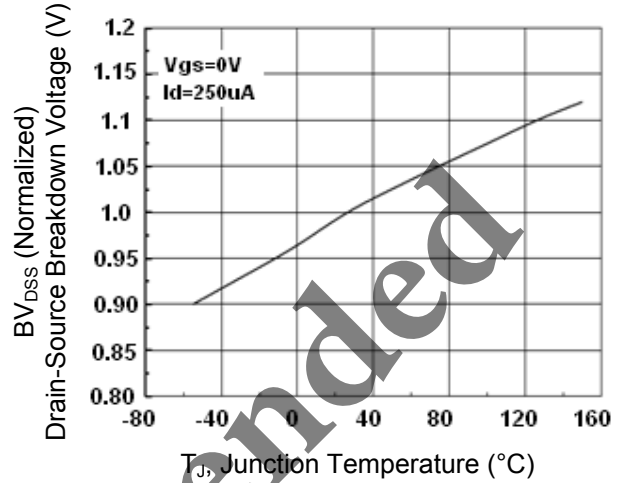
CHARACTERISTICS CURVES

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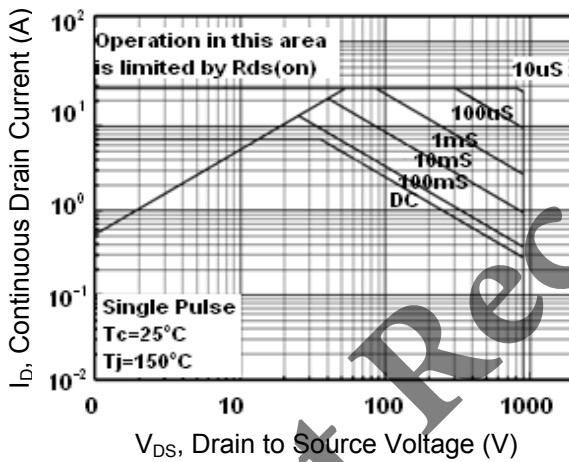
Drain Current vs. Case Temperature



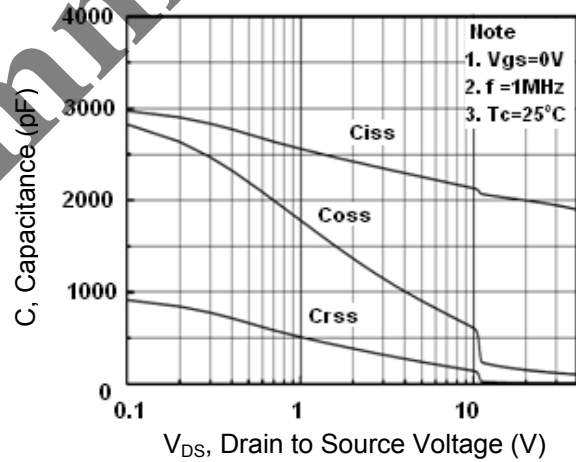
BV_{DSS} vs. Junction Temperature



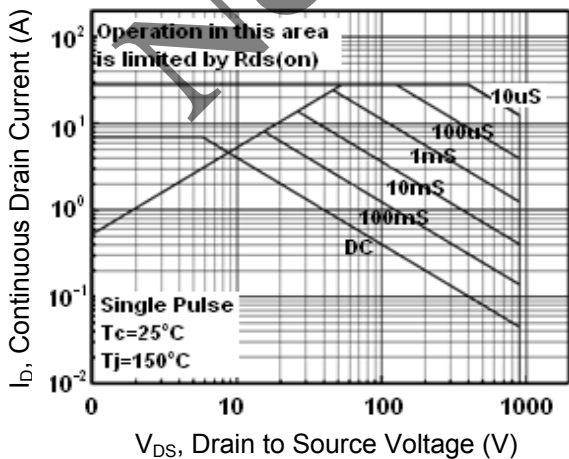
Maximum Safe Operating Area (TO-220)



Capacitance vs. Drain-Source Voltage



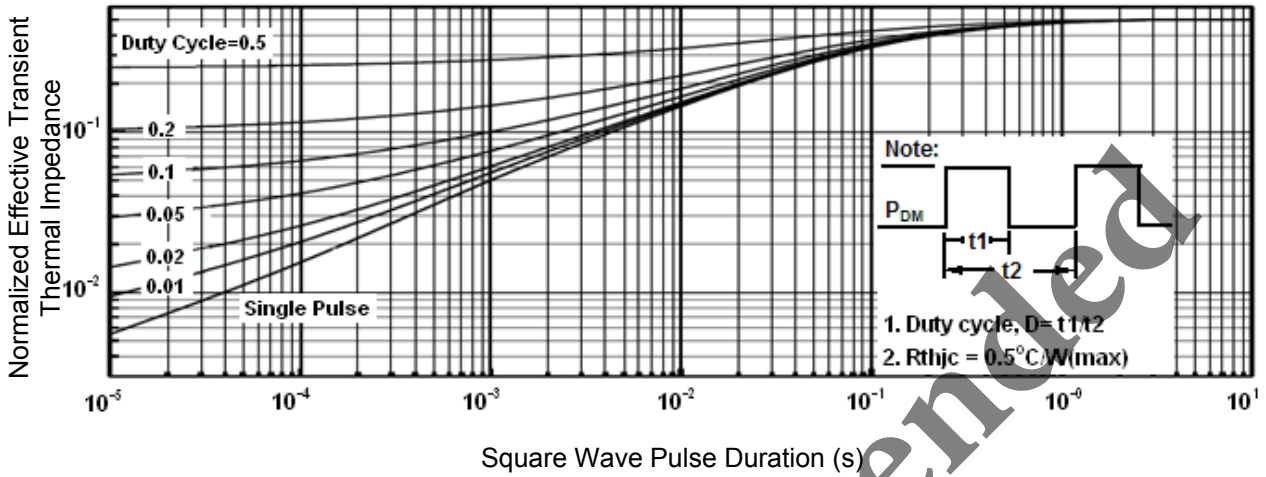
Maximum Safe Operating Area (ITO-220)



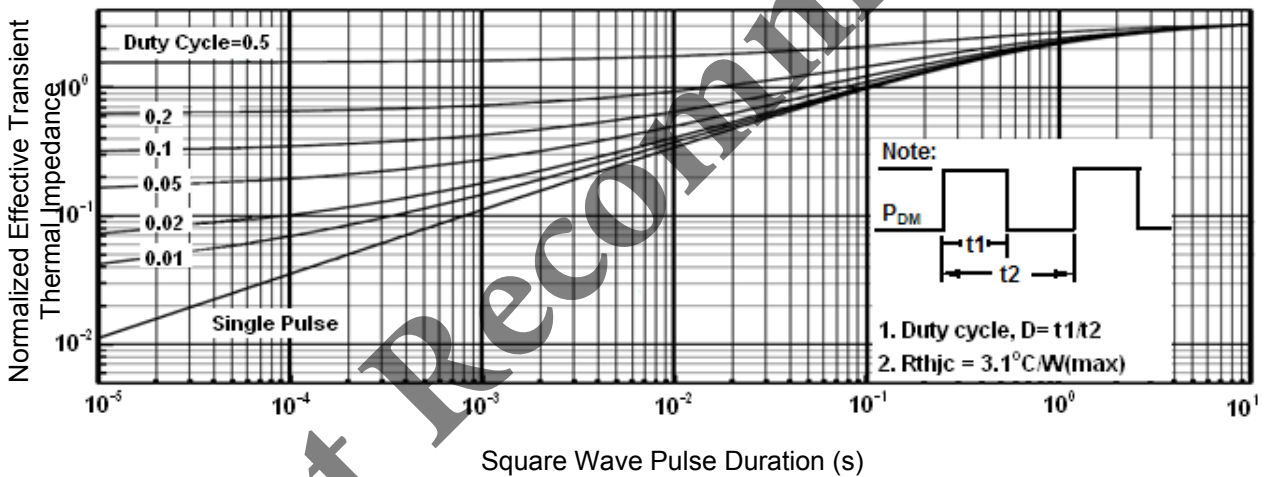
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Case (TO-220)

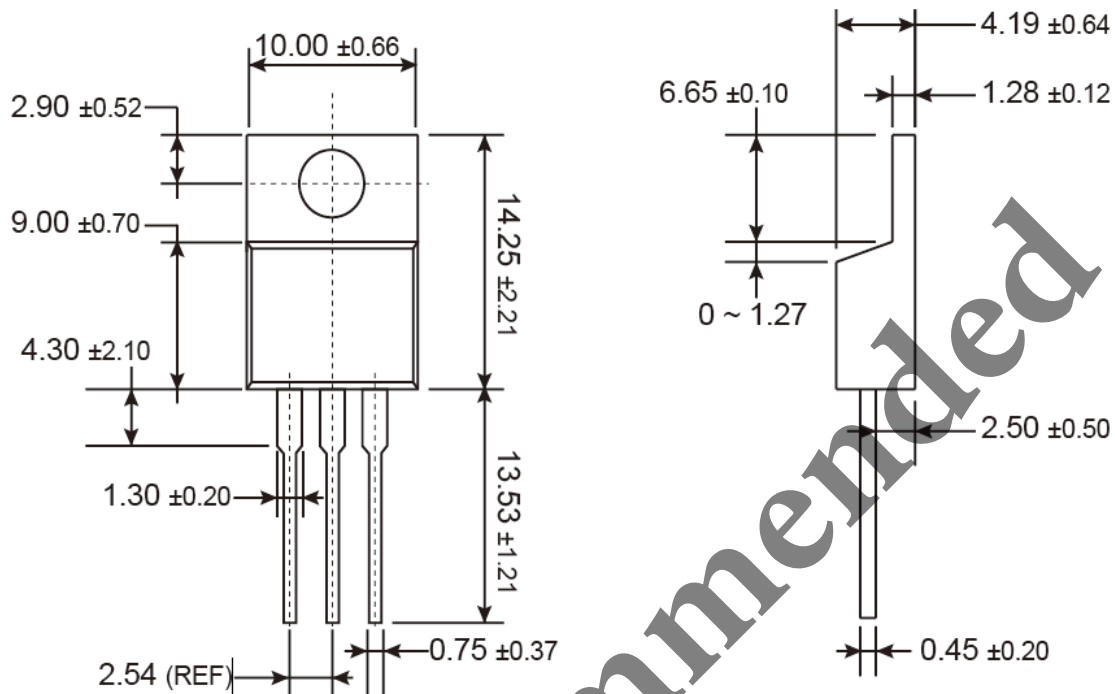


Normalized Thermal Transient Impedance, Junction-to-Case (ITO-220)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-220

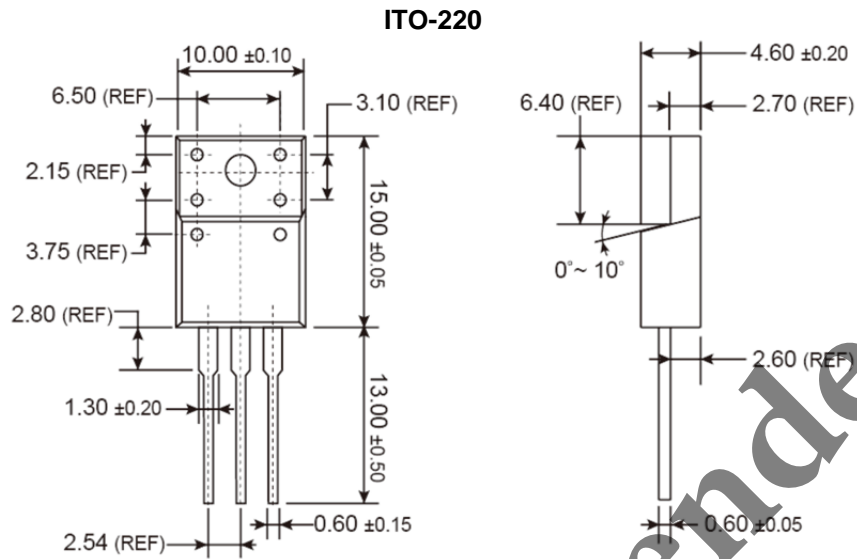


MARKING DIAGRAM



- Y** = Year Code
- M** = Month Code for Halogen Free Product
 - O** =Jan **P** =Feb **Q** =Mar **R** =Apr
 - S** =May **T** =Jun **U** =Jul **V** =Aug
 - W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

Not Recommended

Not Recommended

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