SM72240 SolarMagic 5-Pin Microprocessor Reset Circuit

Check for Samples: SM72240

FEATURES

- **Renewable Energy Grade**
- **Precise monitoring of 5V supply voltages**
- **Fully specified over temperature**
  - **−40°C to +125°C**
- **100 ms minimum Power-On Reset pulse width, 190 ms typical:**
  - **Active-Low $\overline{\text{RESET}}$ Open Drain Output**
- **$\overline{\text{RESET}}$ Output valid for V_{CC} ≥ 1V**
- **Low Supply Current, 6µA typical**
- **Power supply transient immunity**
- **Compatible with MAX811/812 applications**

APPLICATIONS

- **Microprocessor Systems**
- **Computers**
- **Controllers**
- **Intelligent Instruments**
- **Portable/Battery-Powered Equipment**

DESCRIPTION

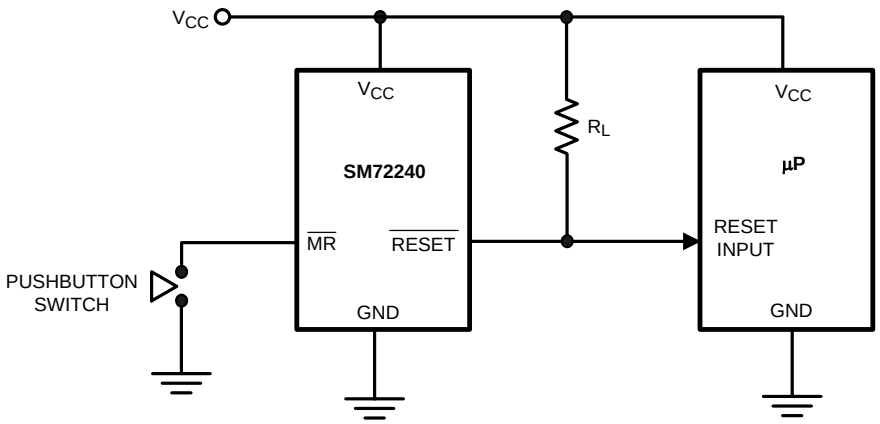
The SM72240 microprocessor supervisory circuit monitors the power supplies in microprocessor and digital systems. It provides a reset to the microprocessor during power-up, power-down, brown-out conditions, and manual reset.

The SM72240 asserts a reset signal whenever the supply decreases below the factory-programmed reset threshold. Reset will be asserted for at least 100ms even after V_{CC} rises above the reset threshold.

The SM72240 has an active-low open-drain $\overline{\text{RESET}}$ output.

The SM72240 is suitable for monitoring 5V. With a low supply current of only 6µA, the SM72240 is ideal for use in portable equipment. The SM72240 is available in the 5-pin SOT-23 package.

Typical Application Circuit



Connection Diagram

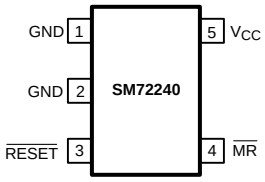


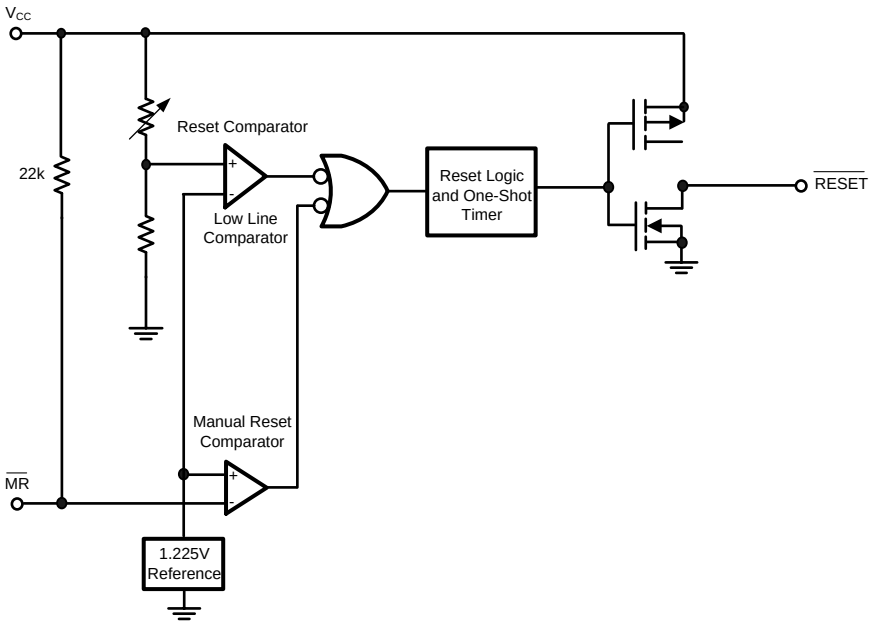
Figure 1. 5-Pin SOT-23 Package
See Package Number DBV

PIN DESCRIPTIONS

Pin	Name	Function
1	GND	Ground reference
2	GND	Ground reference, device substrate, connect to ground.
3	$\overline{\text{RESET}}$	Active-low output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold voltage, and for 190 ms after V_{CC} rises above the reset threshold voltage.
4	$\overline{\text{MR}}$	Active-low input. Reset is asserted whenever this pin is pulled low and remains asserted for 190 ms after the $\overline{\text{MR}}$ pin goes high. May be left open.
5	V_{CC}	Supply Voltage (+5V, nominal)

Block Diagram

Figure 2. SM72240 Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

V_{CC}, $\overline{MR}$		−0.3V to 6.0V
RESET, $\overline{RESET}$		−0.3V to (V_{CC}+ 0.3V)
Input Current, V_{CC} Pin		20mA
Output Current, RESET, $\overline{RESET}$ Pin		20mA
ESD Rating[3]		2kV
Continuous Power Dissipation (T_A = +70°C)	SOT-23[4]	320mW
Operating Temperature Range		−40°C to +125°C
Maximum Junction Temperature		125°C
Storage Temperature Range		−65°C to +160°C
Lead Temperature (soldering, 10sec)		+300°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which the device operates correctly. Operating ratings do not imply specified performance limits. For performance limits and associated test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(4) At elevated temperatures, devices must be derated based on package thermal resistance. The device must be derated at 4.5mW/°C at ambient temperatures above 70°C. The device has internal thermal protection.

Electrical Characteristics

Typical values are at T_A = +25°C. Limits with standard typeface are for T_A = +25°C, and limits in boldface type apply for the operating temperature range −40°C to +125°C , unless otherwise noted.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{CC}	V_{CC} Range			**1.0**		**5.5**	V
I_{CC}	Supply Current (I_{LOAD} = 0A)	SM72240-4.63	V_{CC} = 5.5V		8	**15**	µA
		SM72240-3.08	V_{CC} = 3.6V		7	**10**	
V_{TH}	Reset Threshold	SM72240-4.63		4.54 **4.50**	4.63	4.72 **4.75**	V
		SM72240-3.08		3.03 **3.00**	3.08	3.14 **3.15**	
V_{TH} Tempco	Reset Threshold Temperature Coefficient				30		ppm/°C
t_{RD}	V_{CC} to Reset Delay[2]	V_{CC} = V_{TH} to (V_{TH} − 100mV)			20		µs
t_{RP}	Reset Active Timeout Period			**100**	190	**560**	ms
t_{MR}	$\overline{MR}$ Minimum Pulse Width			**10**			µs
t_{MD}	$\overline{MR}$ to Reset Propagation Delay				2		µs
	$\overline{MR}$ Glitch Immunity[3]				100		ns
V_{IH}	$\overline{MR}$ Input Threshold	V_{CC} > $V_{TH(MAX)}$		**2.3**			V
V_{IL}						**0.8**	
	$\overline{MR}$ Pull-Up Resistance				22		kΩ
V_{OL}	$\overline{RESET}$Output Voltage Low	V_{CC} = V_{TH} min, I_{SINK} = 3.2 mA				**0.4**	V
		V_{CC} > 1V, I_{SINK} = 50µA				**0.3**	
I_{IN}	$\overline{RESET}$ Output Leakage Current (SM72240)	V_{CC} > V_{TH}, $\overline{RESET}$ = 5.5V				**0.5**	µA

(1) Production testing done at T_A = +25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
(2) $\overline{RESET}$ output.
(3) Glitches of 100 ns or less typically will not generate a reset pulse.

Typical Performance Characteristics

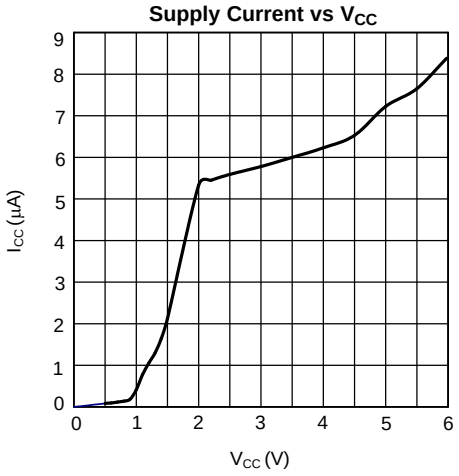


Figure 3.

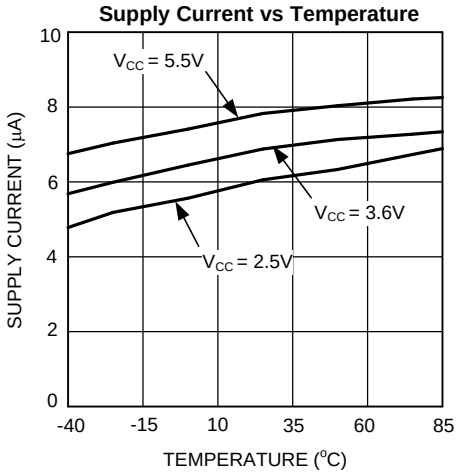


Figure 4.

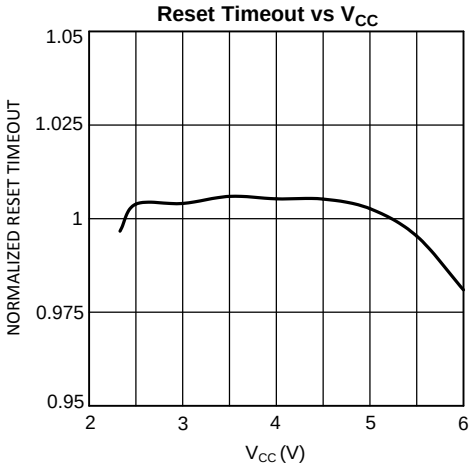


Figure 5.

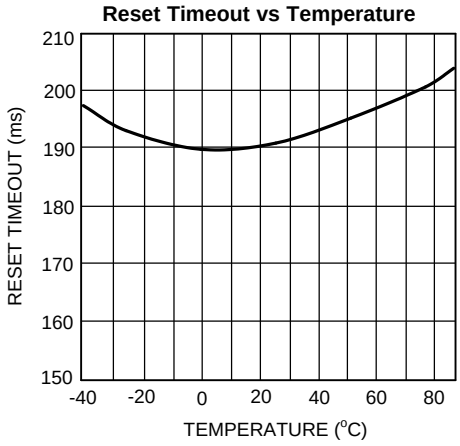


Figure 6.

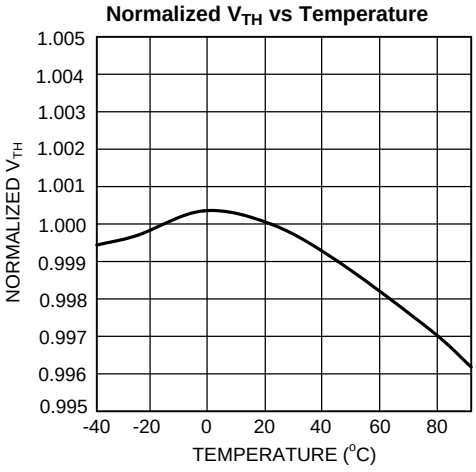


Figure 7.

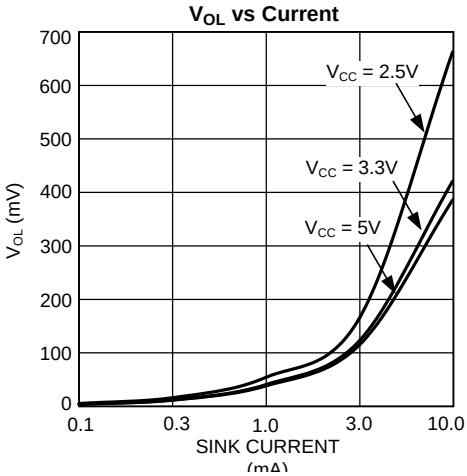


Figure 8.

Typical Performance Characteristics (continued)

Low V_{CC} Characteristics

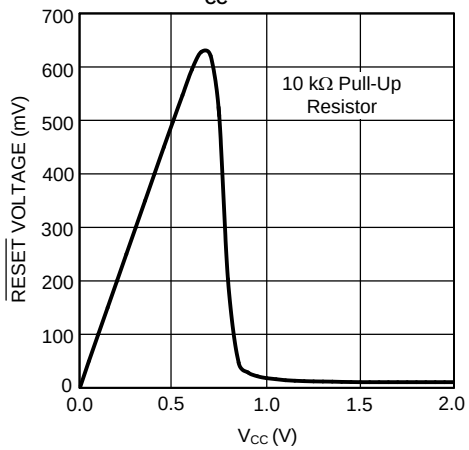


Figure 9.

Timing Diagram

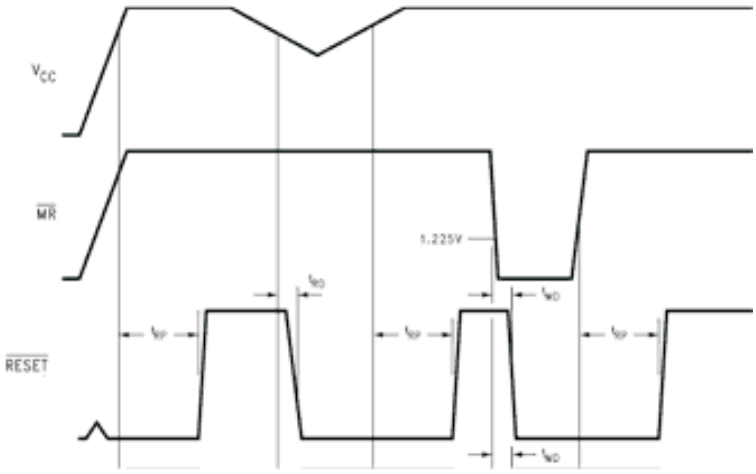


Figure 10.

CIRCUIT INFORMATION

RESET OUTPUT

The reset input of a µP initializes the device into a known state. The SM72240 microprocessor voltage monitoring circuit asserts a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{\text{RESET}}$ is valid for $V_{CC} \geq 1V$. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high and the microprocessor initializes itself into a known state. $\overline{\text{RESET}}$ is active low.

As V_{CC} drops below the reset threshold (such as during a brownout), the reset activates (see the NEGATIVE-GOING V_{CC} TRANSIENTS section). When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

Additionally, the Manual Reset input ($\overline{\text{MR}}$) will initiate a forced reset. See the MANUAL RESET INPUT ($\overline{\text{MR}}$) section.

The SM72240 reset output ignores short duration glitches on V_{CC} and $\overline{MR}$. See the Applications Information section for details.

RESET THRESHOLD

The SM72240 is available with a reset voltage of 4.63V or 3.08V which are suitable for monitoring 5.0V or 3.3V supplies respectively.

MANUAL RESET INPUT ($\overline{MR}$)

Many µP-based products require a manual reset capability, allowing the operator to initiate a reset. The $\overline{MR}$ input is fully debounced and provides an internal 22 kΩ pull-up. When the $\overline{MR}$ input is pulled below V_{IL} ($0.25V_{CC}$) for more than 100 ns, reset is asserted after a typical delay of 2 µs. Reset remains active as long as $\overline{MR}$ is held low, and releases after $\overline{MR}$ rises above V_{IH} and the reset timeout period expires. Use $\overline{MR}$ with digital logic to assert reset or to daisy chain supervisory circuits.

Applications Information

BENEFITS OF PRECISION RESET THRESHOLDS

A microprocessor supply supervisor must provide a reset output within a predictable range of the supply voltage. A common threshold range is between 5% and 10% below the nominal supply voltage. The SM72240 uses highly accurate circuitry to ensure that the reset threshold occurs only within this range (for 5.0V and 3.3V supplies). Table 1 shows how the standard reset threshold applies to 5.0V and 3.3V nominal supply voltages.

Table 1. Monitored Tolerance Table

Reset Threshold	Supply Voltage	
	3.3V	5.0V
4.63 ± %		90.8-94.4%
3.08 ± %	91.8–95.2%	

ENSURING A VALID RESET OUTPUT DOWN TO V_{CC} = 0V

When V_{CC} falls below 1V, the SM72240 $\overline{RESET}$ output is unable to sink the rated current. A high-impedance CMOS logic input connected to $\overline{RESET}$ can therefore drift to undetermined voltages. To prevent this situation, a 100kΩ resistor should be connected from the $\overline{RESET}$ output to ground, as shown in Figure 11.

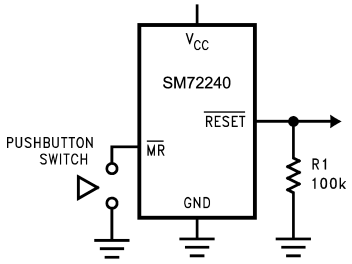


Figure 11. Circuit for $\overline{RESET}$ Valid from V_{CC} = 0V

OPEN DRAIN OUTPUT

An open drain output allows easy paralleling of multiple microprocessor reset circuits without requiring additional logic gates. Open drain outputs also allow interfacing devices of differing logic levels or families, since the output pull-up resistor may be connected to any supply voltage up to 5.5V, regardless of V_{CC}.

The pull up resistor is calculated so that maximum current flow into $\overline{RESET}$ is less than 10 mA when activated. The resistor must be small enough so that the leakage current of all connected devices does not create an excessive voltage drop when the output is not activated. A resistor value of 100 kΩ will generally suffice.

NEGATIVE-GOING V_{CC} TRANSIENTS

The SM72240 is relatively immune to short negative-going transients or glitches on V_{CC}. Figure 12 shows the maximum pulse width a negative-going V_{CC} transient can have without causing a reset pulse. In general, as the magnitude of the transient increases, going further below the threshold, the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 125 mV below the reset threshold and lasts 40 µs or less will not cause a reset pulse. A 0.1 µF bypass capacitor mounted as close as possible to the V_{CC} pin will provide additional transient rejection.

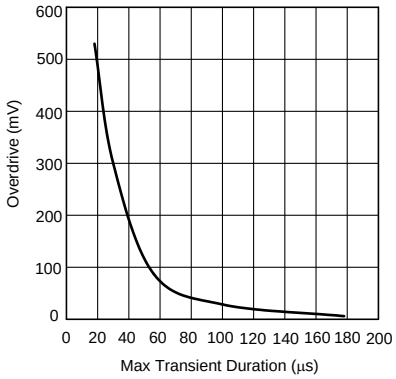


Figure 12. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SM72240MF-3.08/NOPB	NRND	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	R133	
SM72240MF-4.63/NOPB	NRND	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2240	
SM72240MFE-3.08/NOPB	NRND	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	R133	
SM72240MFE-4.63/NOPB	NRND	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2240	
SM72240MFX-3.08/NOPB	NRND	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	R133	
SM72240MFX-4.63/NOPB	NRND	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2240	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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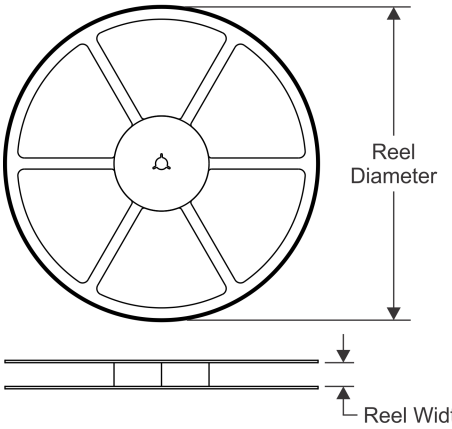
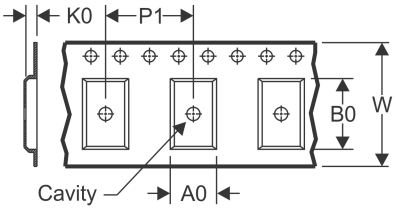
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

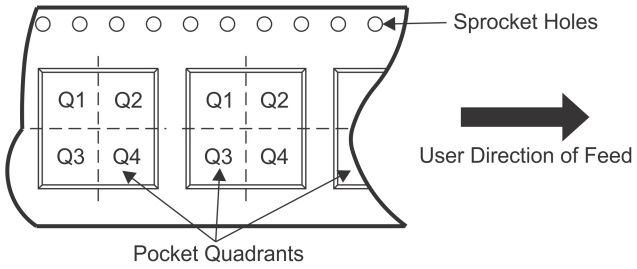


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

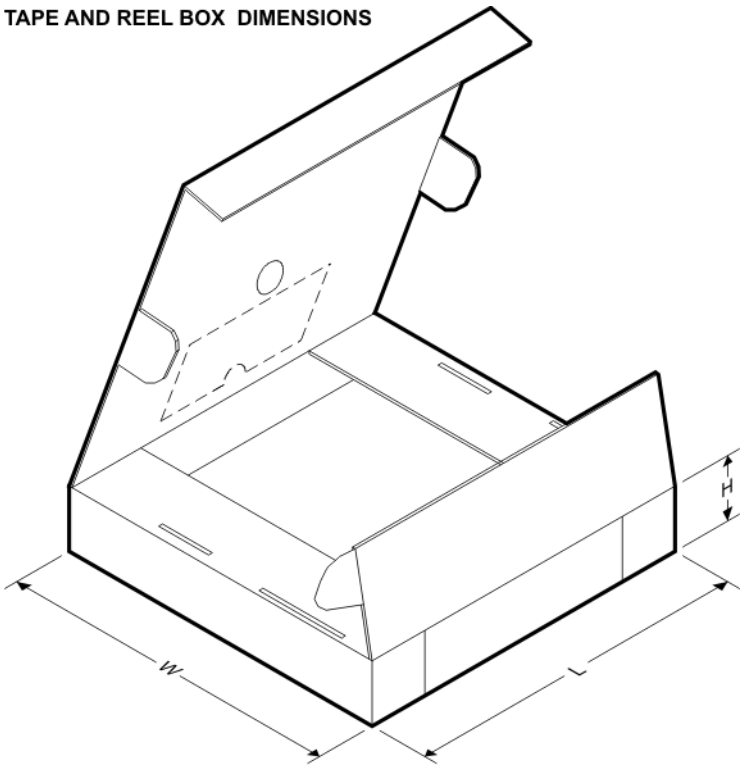
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM72240MF-3.08/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SM72240MF-4.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SM72240MFE-3.08/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SM72240MFE-4.63/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SM72240MFX-3.08/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SM72240MFX-4.63/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

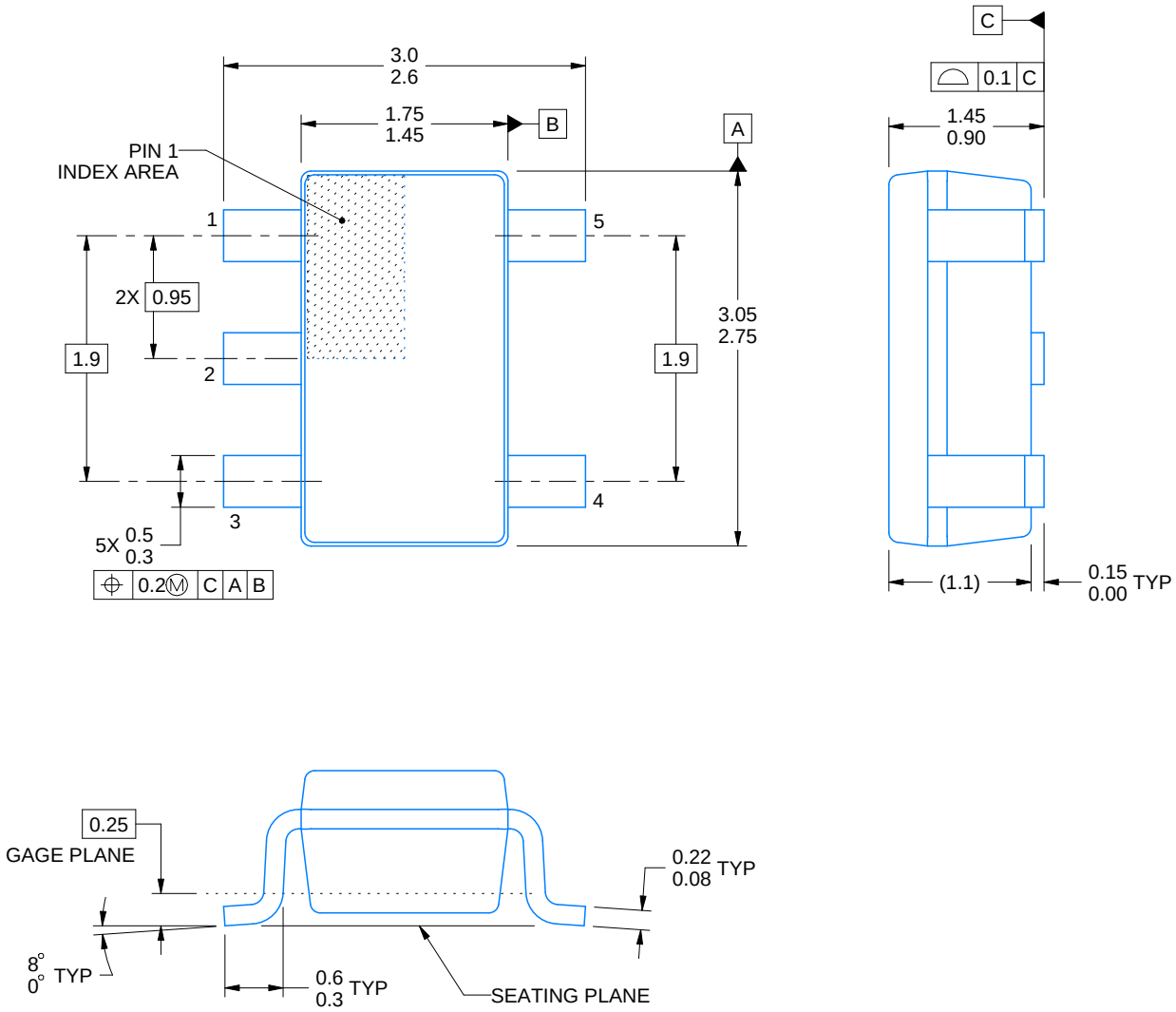
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM72240MF-3.08/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
SM72240MF-4.63/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
SM72240MFE-3.08/NOPB	SOT-23	DBV	5	250	208.0	191.0	35.0
SM72240MFE-4.63/NOPB	SOT-23	DBV	5	250	208.0	191.0	35.0
SM72240MFX-3.08/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
SM72240MFX-4.63/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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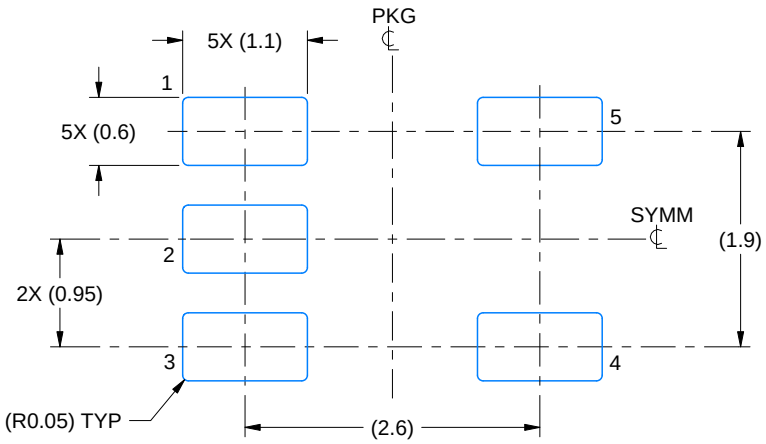
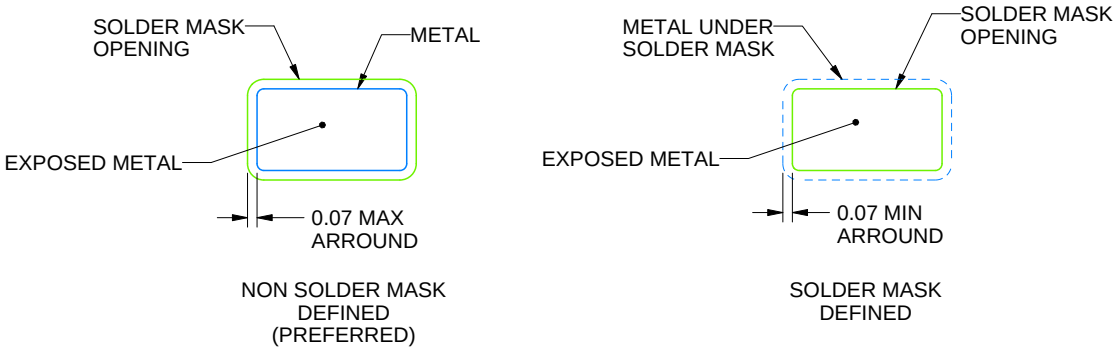
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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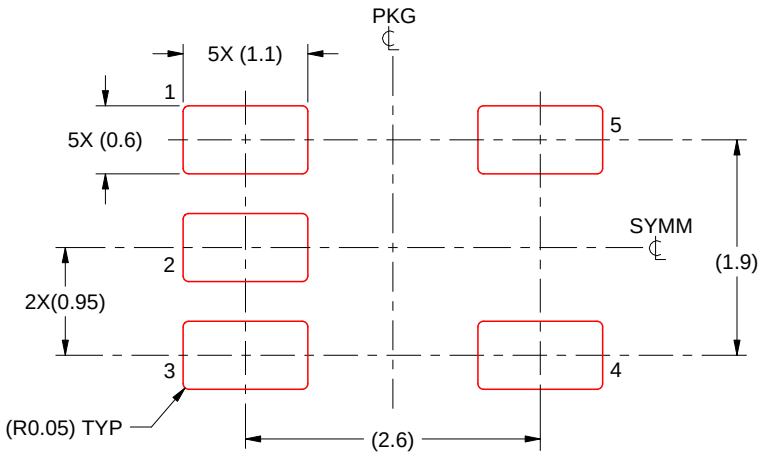
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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