PET800-12-074xD

DC-DC Front-End Power Supply

The PET800-12-074xD is an 800 Watt DC to DC power supply that converts -40 to -72 VDC voltage into an insulated main output of +12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches. The PET800-12-074xD utilizes digital control architecture for greater efficiency, control and functionality.
This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Key Features & Benefits

- High Efficiency to 94% at 50% load
- Wide input voltage range: -40 to -72 VDC
- Always-On 24 W standby output (12 V/2 A)
- Hot-plug capable
- Parallel operation with active current sharing
- Digital controls for improved performance
- High density design: 25 W/in^3
- Small Form Factor 73.5 x 39.0 x 185 mm
- Power Management Bus Communications Protocol for control, programming and monitoring
- Over temperature, output over voltage and over current protection
- One DC OK Signaling Status LED

Applications

- Networking Switches
- High Performance Servers
- Routers

1. ORDERING INFORMATION

PET	800	-	12	-	074	x	D
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
PET Front-Ends	800 W		12 V		73.5 mm	N: Normal R: Reverse	D: DC

2. OVERVIEW

The PET800-12-074xD DC/DC power supply is a DSP controlled, high efficiency front-end power supply. It incorporates state-of-the art technology and uses a forward converter topology with active clamp and synchronous rectification to reduce component stresses, thus providing increased system reliability and high efficiency.

With a wide input DC voltage range the PET800-12-074xD maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.

An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I²C bus. The I²C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I²C bus.

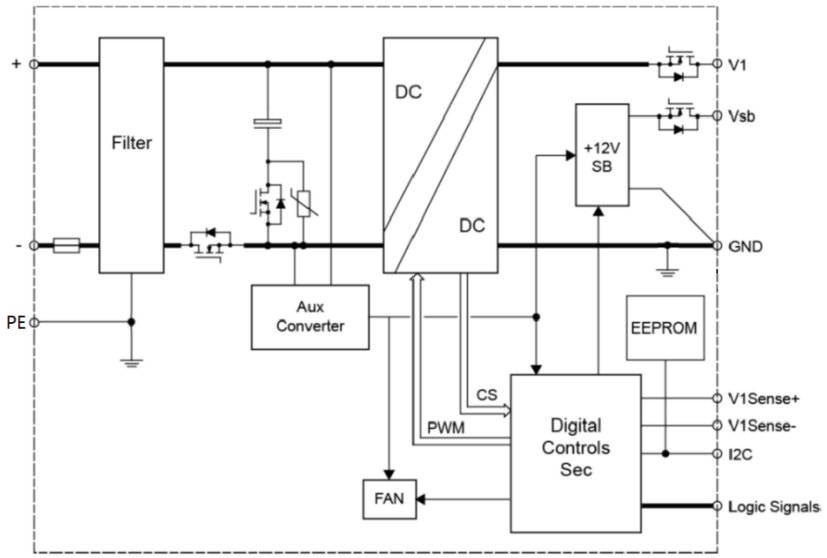


Figure 1. Block Diagram

3. ABSOLUTE MAXIMUM RATING

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi *maxc*	Maximum Input Voltage	Continuous			-75	VDC

4. INPUT

General Condition: T_A = 0… 50 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi start	Minimum operating input voltage	Stand-by output available, DSP running	-30			VDC
Vi nom	Nominal input voltage		-48		-60	VDC
Vi	Input voltage	Normal operation (from Vi min to Vi max)	-40		-72	VDC
Ii	Input current	Vi > Vi min			25	A
Ii pk	Inrush current limitation	From Vi min to Vi max, T_A = 25°C, turn on			50	A
Vi on	Turn-on standby input voltage	Ramping up	-30			VDC
Vi on	Turn-on input voltage	Ramping up	-39		-43	VDC
Vi off	Turn-off input voltage	Ramping down	-37		-41	VDC
η	Efficiency	Vi = -48 VDC; 20% load		90		%
		Vi = -48 VDC; 50% load		94		%
		Vi = -48 VDC; 100% load		91		%
Thold_V1	Hold-up time V1	65 A on V1, 2 A on Vsb with 11000 µF Load capacitance, Vi= -48 VDC	1			ms
Thold_sb	Hold-up time Vsb	65 A on V1, 2A on Vsb with 350 µF Load capacitance, Vi= -48 VDC	2			ms

4.1 INPUT FUSE

A fast-acting 30 A input fuse in the negative voltage path inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

Internal bulk capacitors will be charged through resistors connected from bulk cap minus pin to the DC rail minus, thus limiting the inrush current. After the inrush phase, NTC resistors are then shorted with MOSFETs connected in parallel. The Inrush control is managed by the digital controller (DSP).

4.3 INPUT UNDER-VOLTAGE

If the value of input DC voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 EFFICIENCY

The power supply module efficiency curve is measured at -48 VDC and with external fan power as below.

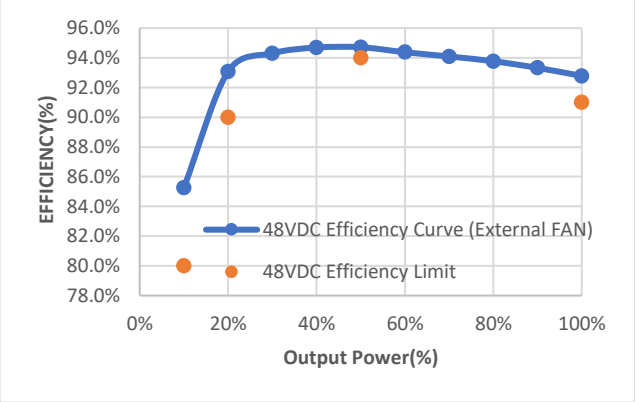


Figure 2. Efficiency Curve

5. OUTPUT

General Condition: T_A = 0…50 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_A = 25°C		12.0		VDC
$V_{1\ set}$	Output Set Point Accuracy		-0.5		+0.5	%$V_{1\ nom}$
$dV_{1\ tot}$	Total Static Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, T_A = 0 to 40°C	-5		+5	%$V_{1\ nom}$
$P_{1\ nom}$	Nominal output power	$V_{i\ min}$ to $V_{i\ max}$, T_A = 0 to 50°C		780		W
$I_{1\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$,, T_A = 0 to 50°C		65		ADC
$V_{1\ pp}$	Output Ripple Voltage[1]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, 20 Mhz Bandwidth			150	mVpp
$dV_{1\ temp}$	Thermal Drift	$V_{i\ nom\ HL}$, 0.5 · $I_{1\ nom}$			0.05	%/°C
$dI_{1\ share}$	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 10%	-6.5		+6.5	ADC
V_{ISHARE}	Current Share Bus Voltage	$I_{1\ peak}$		6		VDC
$dV_{1\ lt}$	Load Transient Response	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 10 … 100% $I_{1\ nom}$, C_{ext} = 0 mF, dI_1/dt = 1 A/µs, recovery within 1% of $V_{1\ nom}$	-5		5	% $V_{1\ nom}$
t_{rec}	Recovery Time				2	ms
$t_{V1\ on\ delay}$	Delay time from DC applied	V1 in regulation Vi = 0V to $V_{i\ min}$, $V_{i\ nom}$, $V_{i\ max}$			2.5	sec
$t_{V1\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{1\ nom}$			10	%$V_{1\ nom}$
$dV_{1\ sense}$	Remote Sense	Compensation for cable drop, 0 to 100% $I_{1\ nom}$			0.25	V
$C_{V1\ load}$	Capacitive Loading				11000	µF
Standby Output V_{SB}						
$V_{SB\ nom}$	Nominal Output Voltage	I_{SB} =1A (50% of I_{SBnom}), T_A = 25°C		12		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-1		+1	%V_{SBnom}
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$	-5		+5	%V_{SBnom}
$P_{SB\ nom}$	Nominal output power	$V_{i\ min}$ to $V_{i\ max}$, T_A = 0 to 50°C		24		W
$I_{SB\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$, T_A = 0 to 50°C			2	ADC
$V_{SB\ pp}$	Output Ripple Voltage	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, C_{ext} = 0Mf, 20 Mhz bandwidth			120	mVpp
$t_{VSB\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{SB\ nom}$			10	%Vsb
dVSB	Load Transient Response	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 10… 100% $I_{SB\ nom}$, dI_{SB}/dt = 0.5A/µs, recovery within regulation of $V_{SB\ nom}$	-5		+5	%Vsb
trec	Recovery Time				250	µs
$C_{VSB\ load}$	Capacitive Loading				350	µF

[1] The output noise and ripple measurement was made with 20 MHz bandwidth using a 6 inch twisted pair, terminated with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor. The output ripple voltage on V_{SB} is influenced by the main output V_1. Evaluating V_{SB} output ripple must be done when maximum load is applied to V_1

5.1 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 3*. Alternatively, separated ground signals can be used as shown in *Figure 4*. In this case the two ground planes should be connected together at the power supplies ground pins.
The output ground of the pins of the power supply provides the output power return path. The ground output at the PCB card edge shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.
The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC-current.

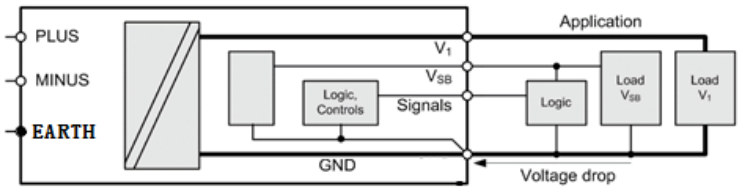


Figure 3. Common low impedance ground plane

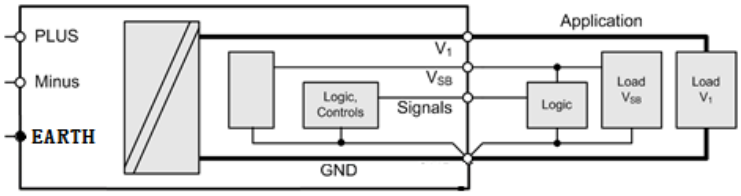


Figure 4. Separated power and signal ground

6. PROTECTION

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input fuse (L)	Not use accessible, fast acting		30		A
$V_{1\ OV}$	OV Threshold V_1	Over Voltage V_1 Protection, Latch-off Type, unlatch unit by disconnecting AC or by togging PS_ON signal	13.3		14.5	VDC
$V_{VSB\ OV}$	OV Threshold V_{SB}	Over Voltage Vsb Protection, unlatch unit by disconnecting AC or by togging PS_ON signal	13.3		14.5	VDC
$V_{1\ UV}$	UV Threshold V_1	Unlatch unit by disconnecting DC or by toggling the PS ON signal		10.5		VDC
$I_{V1\ OC\ Slow}$	OC Limit V_1	Over Current Limitation, $V_{i\ min}$ to $V_{i\ max}$	71.5		80	ADC
$I_{VSB\ OC}$	OC Limit V_{SB}	Over Current Limit., Hiccup mode	2.2		4.5	A
T_{SD}	Over Temperature on Inlet	Automatic recovery with Hysteresis		65		°C
	Over Temperature Oring	Automatic recovery with Hysteresis		105		°C

6.1 OVERVOLTAGE PROTECTION

The PET800-12-074xD front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output or V_{SB}, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the DC supply or by toggling the PS_ON input.

6.2 UNDERVOLTAGE DETECTION

The main output will latch off when V1 drop to below the UV threshold. The latch can be unlatch by disconnecting the supply from the DC mains or by toggling the PS_ON input. The main output will shut down if the V_{SB} voltage drop below 8 V and recover when V_{SB} voltage higher than 10 V.

6.3 CURRENT LIMITATION

MAIN OUTPUT

The main output exhibits a substantially rectangular output characteristic controlled by a software feedback loop. If it runs in current limitation and its voltage drops below ~10.8 VDC for more than 10 ms, the output will latch off (standby remains on).

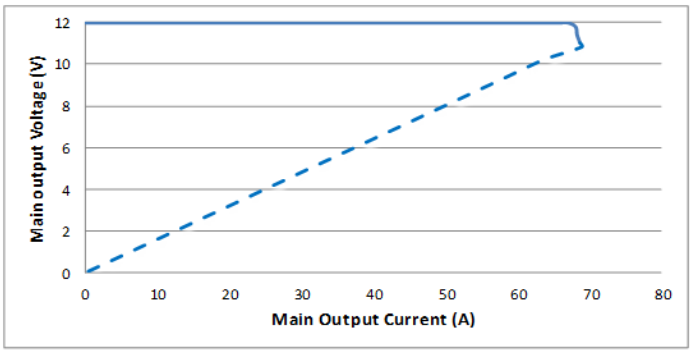


Figure 5. Current Limitation on V_1 (Vi = -54 VDC)

A second current limitation circuit on V_1 will immediately switch off the main output if the output current increases beyond the peak current trip point. The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PS_ON input.

STANDBY OUTPUT

The standby output exhibits a substantially rectangular output characteristic down to 0 V (hiccup mode). If it runs in current Limitation and its output voltage drops below the UV threshold, then the main output will be inhibited.

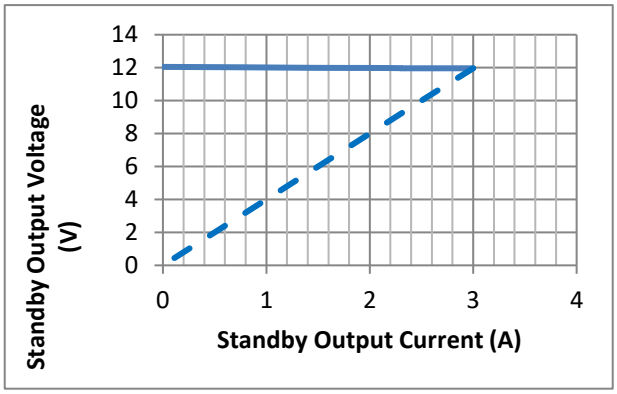


Figure 6. Current limitation on V_{SB}

7. SIGNAL TIMING

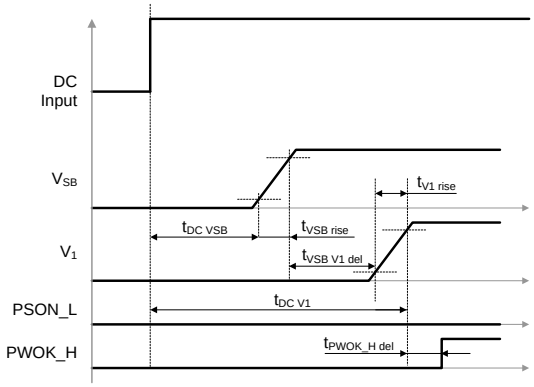


Figure 7. DC turn-on timing

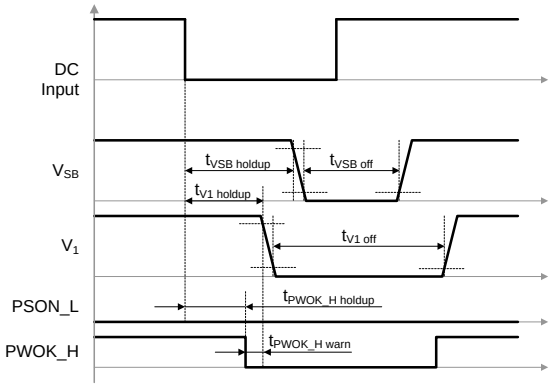


Figure 8. DC long dips

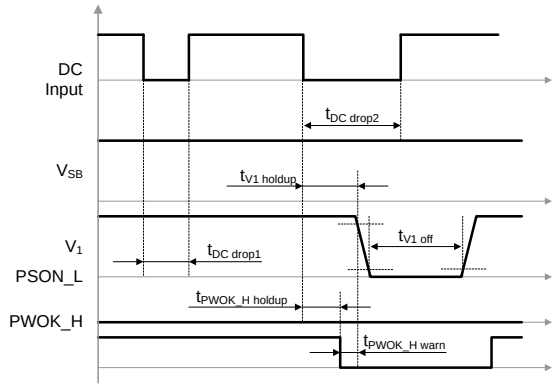


Figure 9. DC short dips

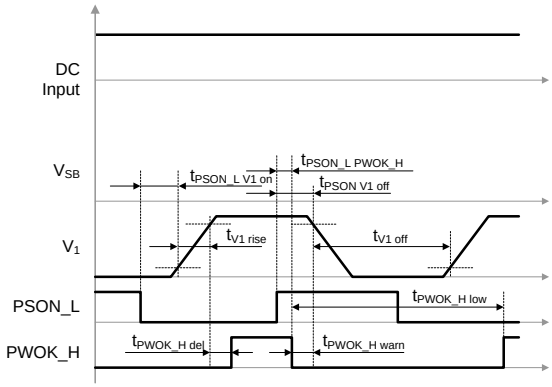


Figure 10. PS_ON turn-on/off timing

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$T_{DC\ VSB}$	DC Line to 90% V_{SB}				1500	ms
$T_{DC\ V1}$	DC Line to 90% V_1	PS_ON = Low			2500	ms
$t_{VSB\ V1\ del}$	V_{SB} to V_1 delay	PS_ON = Low	50		1000	ms
$t_{V1\ rise}$	V_1 rise time		1		200	ms
$t_{VSB\ rise}$	V_{SB} rise time		1		200	ms
$T_{DC\ drop1}$	DC drop without V_1 leaving regulation	$I_{1\ nom}$, $I_{SB\ nom}$			1	ms
$T_{DC\ drop2}$	DC drop without V_{SB} leaving regulation	$I_{1\ nom}$, $I_{SB\ nom}$			2	ms
$t_{V1\ holdup}$	Loss of DC to V_1 leaving regulation	See chapter 4 INPUT	1			ms
$t_{VSB\ holdup}$	Loss of DC to Vsb leaving regulation	See chapter 4 INPUT	2			ms
$t_{PWOK\_H\ del}$	Outputs in regulation to PWOK_H asserted		5		400	ms
$t_{PWOK\_H\ warn}$	Warning time from de-assertion of PWOK_H to V_1 leaving regulation		0.2			ms
$t_{PWOK\_H\ holdup}$	Loss of DC to PWOK_H de-asserted		0.2			ms
$t_{PWOK\_H\ low}$	Time PWOK_H is kept low after being de-asserted		100			ms
$t_{PS\_ON\ V1\ on}$	Delay PS_ON active to V_1 in regulation		5		400	ms
$t_{PS\_ON\ V1\ off}$	Delay PS_ON de-asserted to V_1 disabled				1	ms
$t_{PS\_ON\ PWOK\_H}$	Delay PS_ON de-asserted to PWOK_H de-asserted				4	ms
$t_{V1\ off}$	Time V_1 is kept off after leaving regulation			1		s
$t_{VSB\ off}$	Time V_{SB} is kept off after leaving regulation			1		s

8. MONITORING

The power supply operating parameters can be accessed through I2C interface. For more details refer to chapter 10. I²C / Power Management Bus Communication and document URP.xxxxx (PET800-12-074xD Power Management Bus Communication Manual).

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,mon}$	Input Voltage	$V_{i\,min\,LL} \le V_i \le V_{i\,max}$	-5		+5	%
$I_{i\,mon}$	Input Current	I_i >7 A	-10		+10	%
$P_{i\,mon}$	True Input Power	P_i > 350 W	-10		+10	%
$V_{1\,mon}$	V_1 Voltage		-2		+2	%
$I_{1\,mon}$	V_1 Current	I_1 > 10 A	-2		+2	%
		$I_1 \le$ 10 A	-5		+5	ADC
$P_{1\,nom}$	V_1 Output Power	P_1 > 200 W	-5		+5	%
		$P_1 \le$ 200 W	-24		+24	W
$V_{SB\,mon}$	V_{SB} Voltage		-2		+2	%
$I_{SB\,mon}$	V_{SB} Current		-0.5		+0.5	ADC

9. SIGNALING AND CONTROL

9.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
PS ON# Signal Characteristics					
Signal type (Active Low)	Accepts an open collector/drain input from the system. Pul-up to Vsb located in the power supply.				
PSON = Low	ON				
PSON= Open or High	OFF				
PSON = Low	OFF				
Logic level low	power supply ON	0		1.0	V
Logic level high	power supply OFF	2.0		5.25	V
Source current	Vpson = low			4	mA
Power up delay	T pson on delay	5		400	ms
PWOK delay	T pson pwok			50	ms
PWOK Signal Characteristics					
Signal type	Open collector/drain output from power supply. Pull-up to Vsb located in power supply.				
PWOK = High	Power Good				
PWOK = Low	Power Not Good				
Logic level low voltage	Isink = 4 mA	0		0.4	V
Logical level high voltage	Isource = 200 µA	2.4		5.25	V
Sink current	PWOK = low			4	mA
Source current,	PWOK = high			2	mA
PWOK delay	Tpwok on	100		500	ms
PWOK rise and fall time				100	µs
Power down delay	Tpwok off	1		200	ms
SMB Alert Signal Characteristics					
Signal Type	Open collector/drain output from power supply. Pull-up to Vsb located in power supply.				
Alert = High	Power OK				
Alert = Low	Power Alert to system				
Logic level low voltage	Isink = 4 mA	0		0.4	V
Logic level high voltage	Isink = 50 µA	2.4		3.46	V
Sink current	Alert = low	-		4	mA
Sink current	Alert = high			50	µA

NOTE: Signals that can be defined as low true use the following convention: Signal = low true.

9.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding ±0.5 V. Therefore, all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off.
If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in *Figure 7* (except for SMB_ALERT, PW_OK pins). This will ensure the pin voltage is not affected by an unpowered power supply.

9.3 LED Indicator

Status information is indicated by front-panel LED, LED is bi-colored: green and yellow. See *Table 1* for different LED status.

POWER SUPPLY CONDITION	LED
No DC power to all PSU	OFF
DC present/only standby output on	1 Hz Flashing Green
Power supply DC output ON and OK	Green
Power supply failure	Yellow
Power supply warning	0.5 Hz Flashing Yellow*/Green*

NOTE: * Flashing frequency: 1 Hz (0.5 sec Yellow/ 0.5 sec Green)

Table 1 - LED Status

9.4 PS_ON INPUT

The PS_ON is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition. The PS_ON can be either controlled by an open collector device or by a voltage source.

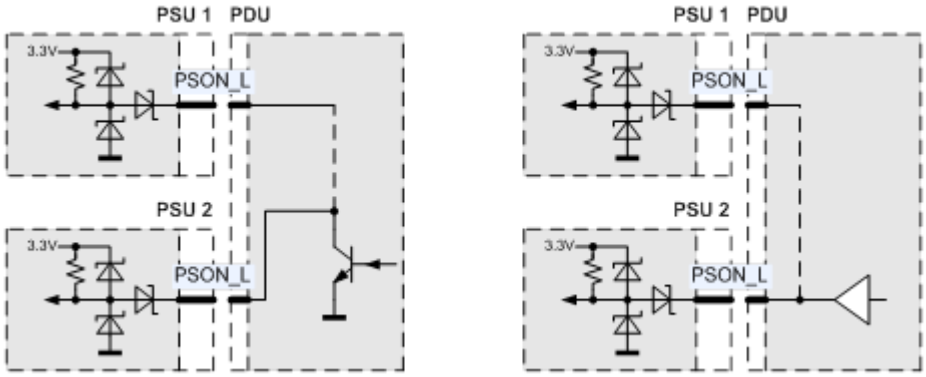


Figure 11. PS_ON Connection

9.5 PWOK OUTPUT

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, an internal failure or when AC power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

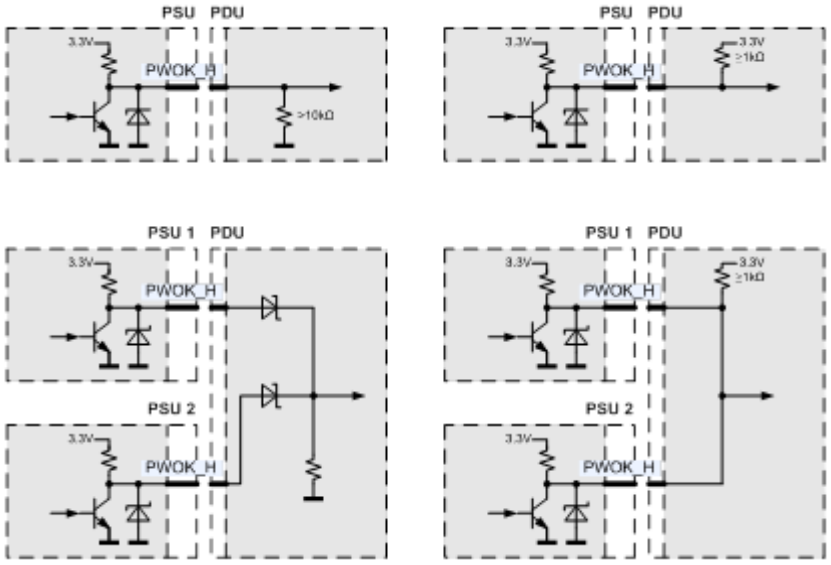


Figure 12. PWOK Connection

9.6 SMB ALERT OUTPUT

The SMB_ALERT is an output signal and it is pulled to 3.3 V by a 4.7 K resistor in power supply. This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

9.6.1 THERMAL CLST

SMB Alert shall also be utilized for warning of critical thermal component temperatures. The Thermal CLST shall assert when the component temperature, which shall be reported by a dedicated thermal probe, is reaching below specified _T to critical shut down. The power supply shall report the temperature in addition to Thermal CLST through.

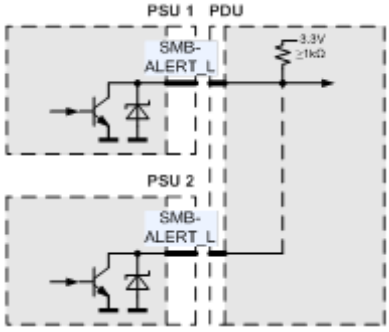


Figure 13. SMBALERT_L connection

9.7 PDB_ALERT

The PDB_ALERT is received signal from system, if signal is pulled low, the unit internal fan will be forced to run at max. speed.

9.8 PDB_FAULT

The PDB_FAULT receive a signal from system or PSU backplane. Power shall be shut down if this signal is high.

9.9 CURRENT SHARE

All outputs shall be capable of operating in a redundant current share mode. Eight power supplies may be operated in parallel. All outputs shall incorporate an isolation diode for fault isolation. Filter capacitors that are located after the isolation diode shall be of high reliability and shall be de-rated sufficiently to minimize failures. The +12 V current sharing shall be a single wire type. Connecting the ISHARE pins of each power supply together shall enable the current share feature. With the current share pins tied together, the output load current shall be balanced as defined below. The load share (ISHARE) shall be a single wire type. Connecting ISHARE pins of each PCM together shall enable the current share feature. With the current share pins tied together, the output load current shall be balanced to within 10% of full load (current difference should be less than 6.5 A). Shorting or opening of a current share pin shall not cause the output voltage to go out of steady state regulation. For 65 A the ISHARE voltage shall be 6 V for a single power supply.
The standby output uses a passive current share method (droop output voltage characteristic).

9.10 REMOTE SENSE

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 200 mV on the GND rail.
With open sense inputs the main output voltage will rise by 270 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

9.11 PRESENT_L

The PRESENT_L pin is wired through a 100 Ohms resistor to internal GND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 5mA to guarantee a low level voltage if power supply is seated.

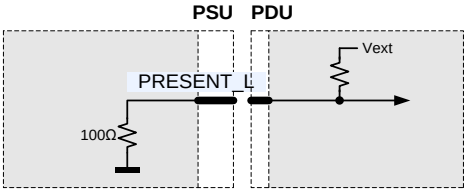


Figure 14. PRESENT_L Connection

10. I²C / POWER MANAGEMENT BUS COMMUNICATION

The interface driver in the PET supply is referenced to the V1 Return. The PET supply is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and further characterized referenced in the *Figure 14*.

The SMB_ALERT signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events.

Communication to the DSP or the EEPROM will be possible as long as the input DC voltage is provided. If no DC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit).

- There are 10K internal pull-up resistors
- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery
- within 10 ms

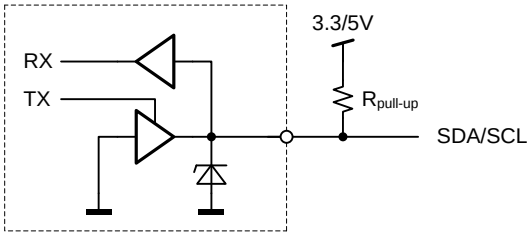


Figure 15. Physical layer of communication interface

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
SCL / SDA					
V_{IL}	Input low voltage		-0.5	1.0	V
V_{IH}	Input high voltage		2.3	3.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		20+0.1C_b[1]	1000	ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF	20+0.1C_b[1]	300	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
$R_{pull-up}$	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[3]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		ms

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

Table 2. I2C / SMBus Specification

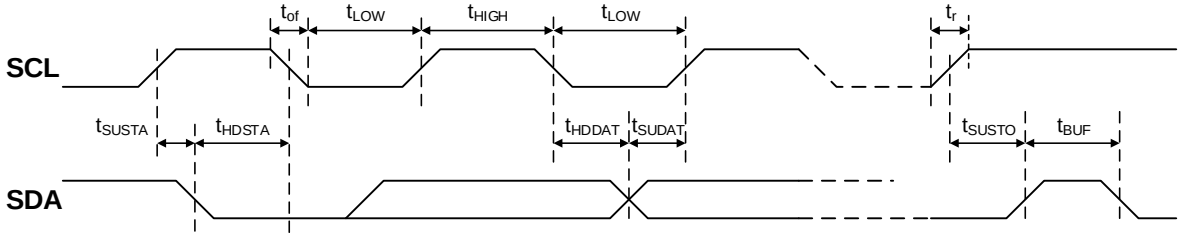


Figure 16. I²C / SMBus Timing

10.1 ADDRESS SELECTION

The address for I2C communication can be configured by pulling address input pins A1 and A0 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A1 / A0 pin to be in High Level if left open. A fixed addressing offset exists between the Controller and the EEPROM.

A2[3]	A1	A0	I2C Address[4]	
			Controller	EEPROM
0	0	0	0xB0	0xA0
0	0	1	0xB2	0xA2
0	1	0	0xB4	0xA4
0	1	1	0xB6	0xA6
1	0	0	0xB8	0xA8
1	0	1	0xBA	0xAA
1	1	0	0xBC	0xAC
1	1	1	0xBE	0xAE

[3] A2 will be implemented in future
[4] The LSB of the address byte is the R/W bit.

Table 3. Address and protocol encoding

10.2 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see *Figure*) and can be accessed under different addresses, see ADDRESS SELECTION. The SDA/SCL lines are connected directly to the controller and EEPROM which are supplied by internal 3.3 V.
The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

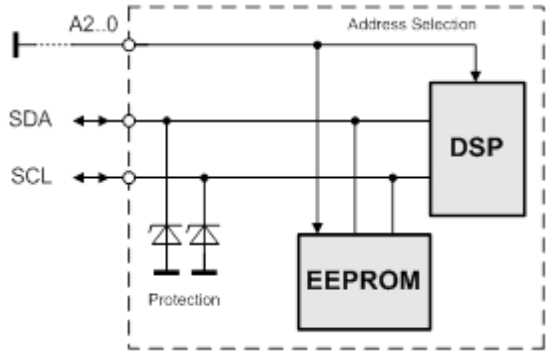


Figure 17. I2C Bus to DSP and EEPROM

10.3 EEPROM PROTOCOL

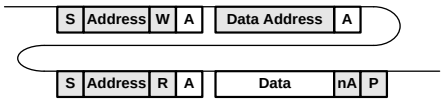
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE
The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

S	Address	W	A	Data Address	A	Data	A	P

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



10.4 POWER MANAGEMENT BUS PROTOCOL

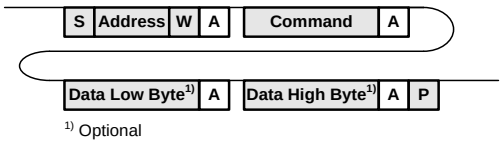
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The PET800-12-074xD supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

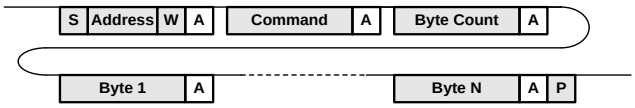
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



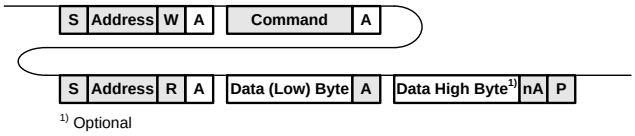
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See PET800-12-074xD Power Management Bus Communication Manual for further information.



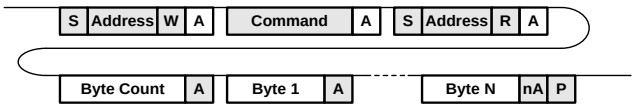
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes.
See PET800-12-074xD Power Management Bus Communication Manual for further information.



10.5 GRAPHICAL USER INTERFACE

The Bel Power Solutions provides with its “I²C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PET800-12-074xD Front-End. The utility can be downloaded on: belfuse.com/power-solutions and supports both the PSMI and Power Management Bus protocols.
The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.
If the GUI is used in conjunction with the VRA.00334.0 Evaluation Board, it is also possible to control the PS_ON pin(s) of the power supply.
Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

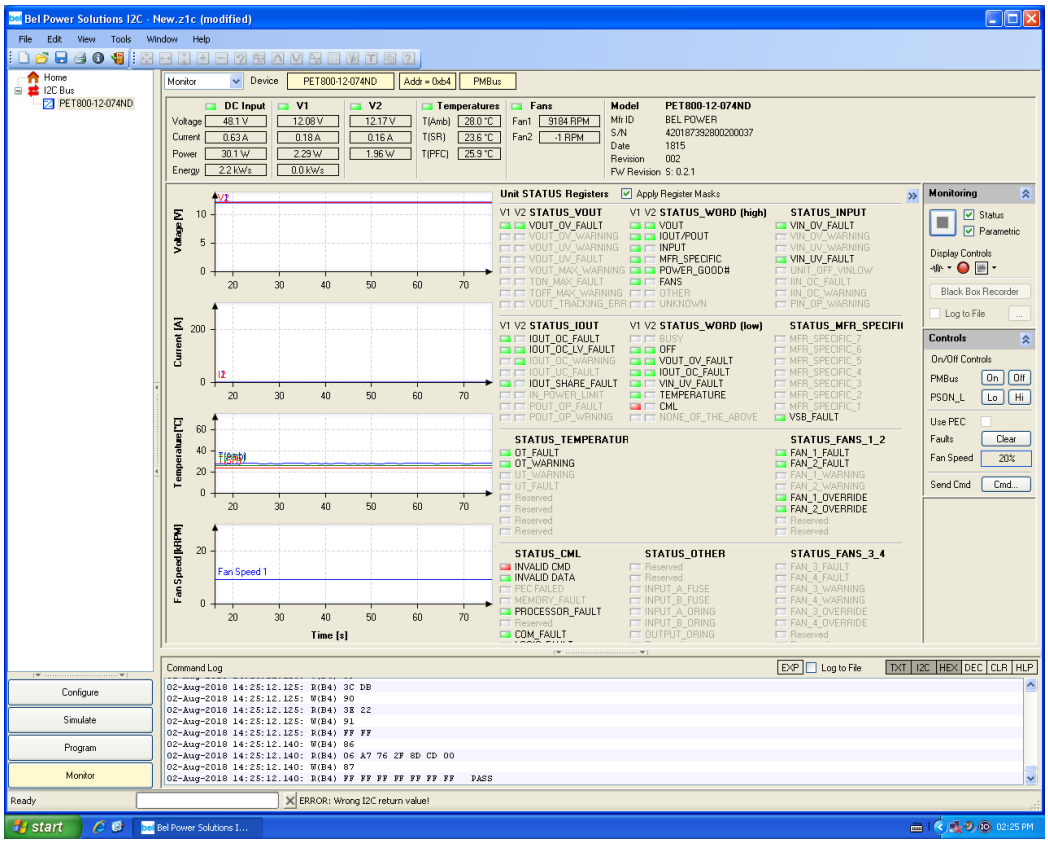


Figure18. Monitoring dialog of the I2C Utility

11. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PET800-12-074xD is provided with a rear to front airflow, which means the air enters through the DC-output of the supply and leaves at the DC-inlet.
The PET800-12-074xD power supply has been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

The PET800-12-074xD provides access via I²C to the measured temperatures of in total 6 sensors within the power supply, see *Table 4*. The microprocessor is monitoring these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V_1 (or V_{SB} if auxiliary converter is affected) will be disabled. At the same time the warning or fault condition is signalized accordingly through LED, PWOK and SMB_ALERT.

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	POWER MANAGEMENT BUS REGISTER	WARNING THRESHOLD	SHUT DOWN THRESHOLD
Inlet air temperature	Sensor located on control board close to DC end of power supply	0x8E	ND:67°C RD: 77°C	ND:70°C RD:80 °C
Synchronous rectifier	Sensor located on secondary side of DC/DC stage	0XD2	ND:92°C RD:102 °C	ND:95°C RD:105 °C
Primary heat sink	Sensor located next to the heat sink		-	105°C
outlet air temperature	Sensor located on control board close to DC input connector	0x8F	ND:62°C RD:72 °C	ND:65°C RD:75 °C
Oring mosfet	Sensor located on the gold finger	0x8D	ND:82°C RD:112 °C	ND:85°C RD: 115°C

Table 4. Temperature sensor location and thresholds

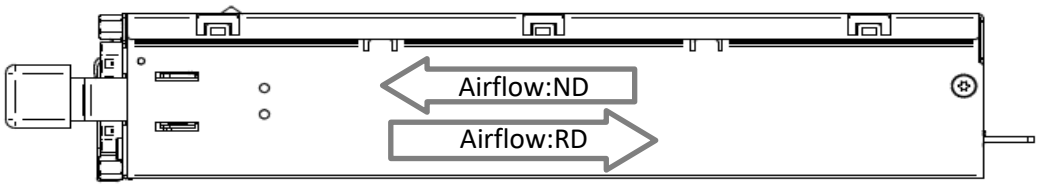


*Figure**19**. Airflow direction*

12. ELECTROMAGNETIC COMPATIBILITY

12.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LED, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetics Filed	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1µs Pulse Modulation, 10 kHz ... 2 GHz	A
Burst	IEC / EN 61000-4-4, Level 3 DC input port ±1 kV, 1 minute	A
Surge	IEC / EN 61000-4-5 Common mode: ±1 kV Differential mode ±1 kV	A
RF Conducted Immunity	IEC / EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 … 80 MHz	A

12.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single power supply	Class A
Radiated Emission	EN 55022 / CISPR 22: 30 MHz … 1 GHz, QP, single power supply	Class A

13. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 62368-1, and UL 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	Approved to the latest version of the following safety standards: UL/CSA 62368-1, EN 62368-1 and IEC 62368-1.	Approved
Isolation Strength	Input plus to chassis; 1414 V for 1 minute	Basic
	Input minus to chassis; 1414 V for 1 minute	Basic
	Output to chassis	Function
Creepage / Clearance	Primary to chassis (PE) Primary to secondary	>2 mm

14. ENVIRONMENTAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
TA	Ambient Temperature	Up to 1’000 m ASL	0		+50	°C
		Linear derating from 1’000 to 3’048 m ASL			+40	°C
TAext	Extended Temp. Range				65	°C
TS	Storage Temperature	Non-operational	-20		+70	°C
	Altitude	Operational, above Sea Level	-		3’048	m
		Non-operational, above Sea Level	-		10’600	m
	Shock, operational	Half sine, 11ms, 10 shocks per direction, 6 directions			1	g peak
	Shock, non-operational				30	g peak
	Vibration, sinusoidal, operational	IEC/EN 60068-2-6, sweep 5 to 500 to 5 Hz, 1 octave/min, 5 sweeps per axis			1	g peak
	Vibration, sinusoidal, non-operational				4	g peak
	Vibration, random, non-operational	IEC/EN 60068-2-64, 5 to 500 Hz, 1 hour per axis			0.025	g^2/Hz
	Acoustical Noise	Distance 1 meter, 25°C, 50% Load			46	dBA

15. RELIABILITY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
MTBF	Mean time to failure	According Telcordia SR-332; Ground Benign T_A = 25°C, Vi = -48 VDC, 0.5 · I1 nom, I_{SB} nom	300			kh
	Expected life time	T_A = 25°C, V_i = -48 VDC, 0.7 · $I_{1\ nom}$, $I_{SB\ nom}$	5			years

16. MECHANICAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width		73.5		mm
		Heigth		39		mm
		Depth		185		mm
m	Weight			735		g

Top and side views with the connector added

Dimensions in mm, tolerance unless otherwise stated: 0.5-30: ±0.3; 30-120: ±0.4; 120-400: ±0.5

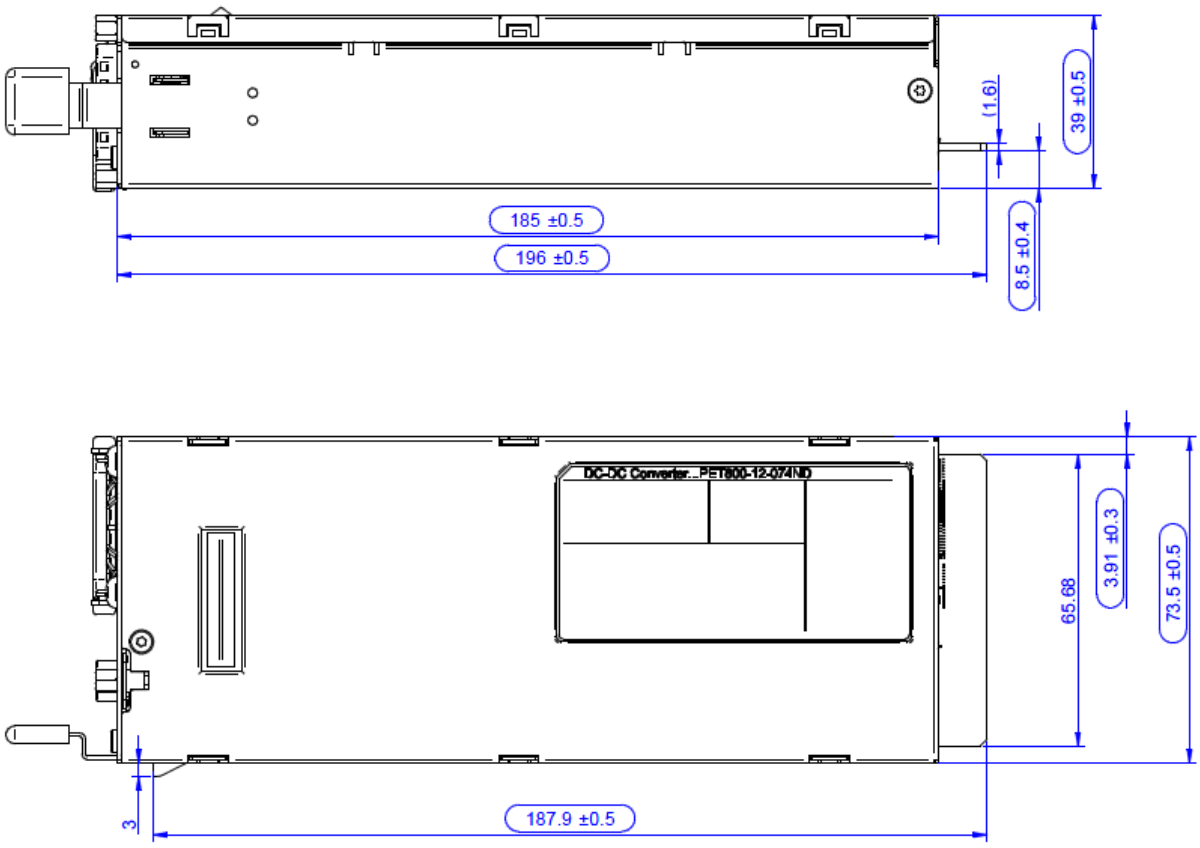


Figure 20. Top and side view with the connector added (TBD)

Figure21. Front View

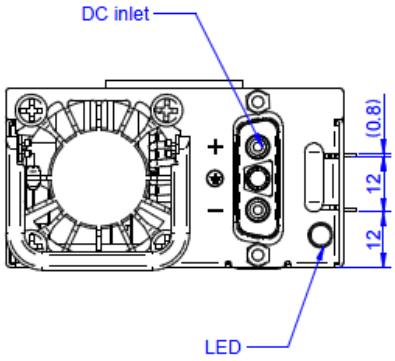


Figure22. Rear View

17. CONNECTIONS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
DC input connector	D-SUB connector				
Mating input connector	POSITRONIC CBD3WK3F0000X/AA(female terminal FC4008D/AA x2pcs, male terminal MC4008D/AA x1pcs, optional plastic cover D15000Z00/AA), wire size10AWG or above ; Amphenol FCE17-A3M3SM-2N2, wire size 10AWG or above ; Other equivalent part are acceptable.				
DC output connector	Golden finger 16 power contacts, 24 signal contacts				
DC output mating connector	FCI 10035388-102LF or equivalent BEL P/N : ZES.00530				

For the pin assignment of DC connector, please refer to Figure 23 and Table 4.

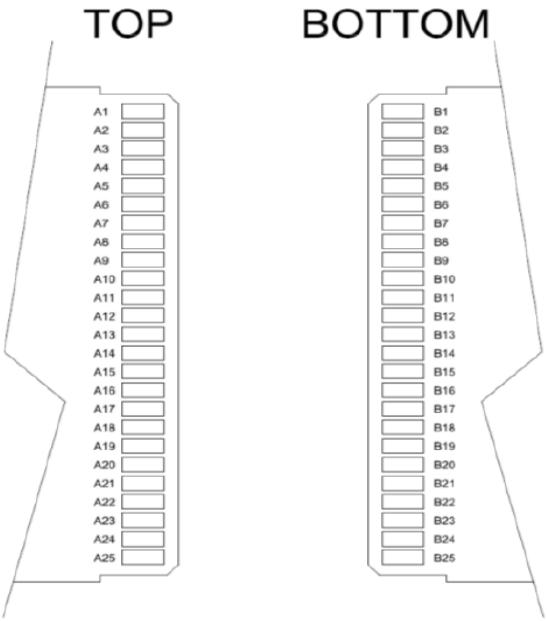
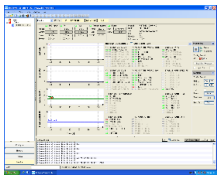


Figure 23. Pin Assignment of DC Output Connector (PCB card edge)

PIN	SIGNAL NAME	DESCRIPTION
A1 ~ A9	VS_R	+12 V return
B1 ~ B9	VS_R	+12 V return
A10 ~ A18	VS	+12 V power output
B10 ~ B18	VS	+12V power output
A19	SDA	I²C Data signal
A20	SCL	I²C Clock signal
A21	PS_ON	Module PS_ON Remote control power On/Off (Pulled LOW=POWER ON)
A22	SMB_ALERT	SMB Alert signal output: active-low
A23	VS_SENSE_R	+12 V Remote sense return
A24	VS_SENSE	+12 V Remote sense
A25	PWOK	Power Good Output. Signal is pulled HIGH to indicate all outputs ok.
B19	A0	I²C address bit 0
B20	A1	I²C address bit 1
B21	12 VSB	+12 V Standby Output
B22	PDB_FAULT	To receive a FAULT signal from system or PSU backplane. PSU shall shutdown if this pin is pulled HIGH.
B23	ISHARE	+12 V Main output Current share bus
B24	PDB_ALERT	To receive ALERT signal from system or PSU backplane, If signal is pulled LOW, the PSU internal fan shall be forced to run at maximum speed to improve thermal performance.
B25	Present_L	Power supply seated, active-low

Table 5. Output Pin Assignment

18. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**BPS I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor PET Front-Ends (and other I²C units)	Download	belfuse.com/power-solutions
 Loading Board  	**Dual Connector Board** Connector board to operate 2 PET units in parallel. Includes an on-board USB to I²C converter (use I²C Utility as desktop software).	VRA.00334.0	belfuse.com/power-solutions

19. REVISION HISTORY

DATE	REVISION	ISSUE	PREPARED BY	APPROVED BY	ECO/MCO REFERENCE NO
2018/03/21	001	Initial release	Zhiqun Wan	Mike Chen	
2018/08/02	002	Initial release	Zhiqun Wan	Mike Chen	
2018/10/18	003	Initial release	JG YU	Andrew Li	C95037
2020/08/24	A	Adding Present_L signal on B25 Adding 9.11, description of Present_L Update to A version	Zhiqun Wan	Zhiqun Wan	CO106600

For more information on these products consult: tech.support@psbel.com

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