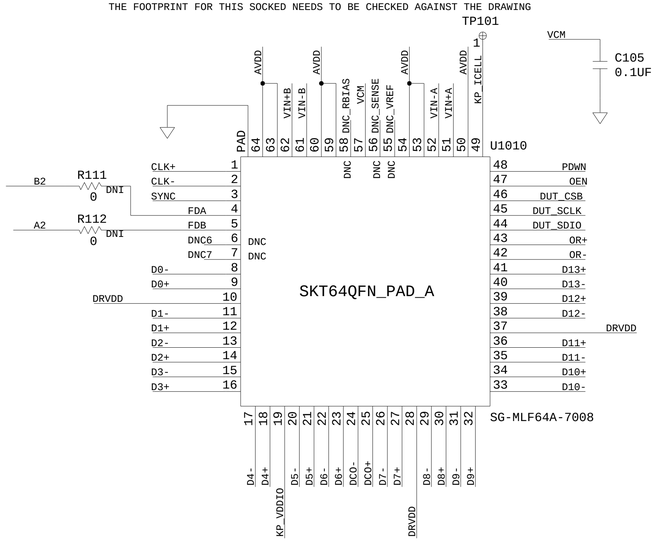
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

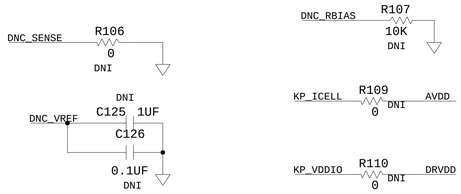
AD9643/AD6649 ENG (SOCKET)

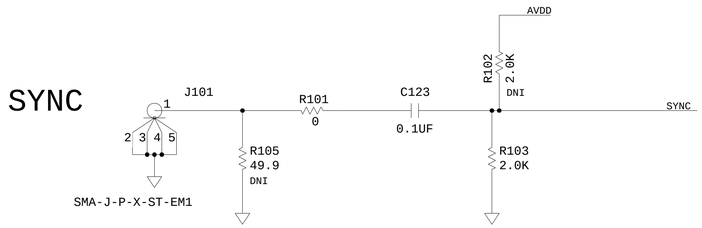
DUT

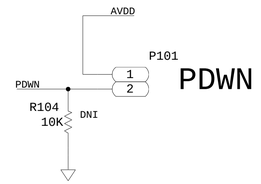
THE FOOTPRINT FOR THIS SOCKED NEEDS TO BE CHECKED AGAINST THE DRAWING

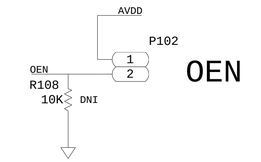


EXTRA CIRCUITRY FOR AD9258 COMPATIBILITY
NOT NEEDED FOR AD9643/AD6649

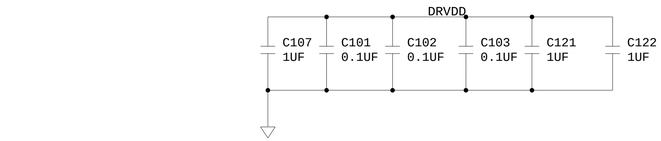


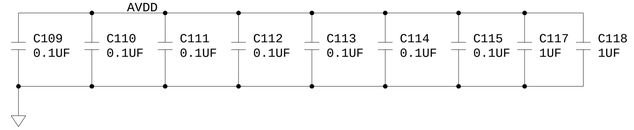






LAYOUT: DECOUPLING QUANTITY MAY VARY LAYOUT DEPENDING





ANALOG DEVICES

SCHEMATIC

9643 & 6649 ENGINEERING EVAL. PCB
AD9643
Engineering Board

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	9643EE01	B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE NONE	SHEET 1 OF 6

POWER

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

P201 PJ-202A
F201 1.1A
FL201 BNX016-01
CR202 SK33A-TP
CR203 LN1514G8TRA (GREEN)
C201 10UF
CR201
R201 261
VIN

U201 ADP1708ARDZ-R7
R202 10K
R203 1.91K
C202 4.7UF
C203 4.7UF
E201 100MHZ
P103
5V_SUPPORT

CR204 S2A-TP
U202 ADP150AUJZ-3.3-R7
C204 4.7UF
C205 DNI
0.01UF
C206 4.7UF
E202 100MHZ
P104
3P3V_ANALOG
DNI E203 100MHZ

U203 ADP150AUJZ-3.3-R7
C207 4.7UF
C208 DNI
0.01UF
C209 4.7UF
E204 100MHZ
P105
3P3V_DIGITAL

U207 ADP150AUJZ-1.8-R7
C241 4.7UF
C242 DNI
0.01UF
C243 4.7UF
E217 100MHZ
P110
1P8V_CLOCK

P106
E208 100MHZ

U204 ADP1706ARDZ-1.8-R7
C225 4.7UF
C226
0.01UF
C227 4.7UF
E205 100MHZ
P107
AVDD

DNI E206 100MHZ
TO EVALUATE SHARING OF AVDD AND DVDD

U205 ADP1706ARDZ-1.8-R7
C228 4.7UF
C229
0.01UF
C230 4.7UF
E207 100MHZ
P108
DRVDD

P109
E209 100MHZ

P202
Z5.531.3625.0
E212 100MHZ
C231 0.1UF
C232 10UF
3P3V_DIGITAL
E213 100MHZ
C233 0.1UF
C234 10UF
DRVDD
E214 100MHZ
C235 0.1UF
C236 10UF
AVDD

P203
Z5.531.3425.0
E215 100MHZ
C237 0.1UF
C238 10UF
5V_SUPPORT
E216 100MHZ
C239 0.1UF
C240 10UF
3P3V_ANALOG

CR205 S2A-TP
CR206 S2A-TP
JP201 0
JP203 0

OPTIONAL SWITCHING SUPPLY

U206 ADP2114_PRELIM
VDD SCFG FREQ SYNC_CLKOUT OPCFG EN1 V1SET FB1 SS1 EN2 V2SET FB2 SS2 GND
VIN1 VIN2 VIN3 VIN4 VIN5 VIN6
PGOOD1 COMP1 SW1 SW2 PGOOD2 COMP2 SW3 SW4 PGND1 PGND2 PGND3 PGND4 PAD
SW_FREQ
C210 22UF
C211 22UF
R206 10
C212 1UF
R204 0 DNI
R205 1.00K
R207 100K
R208 100K
C213 2200PF
R214 10.5K
C214 100PF
R209 27K
R210 4.64K
R211 15K
C217 0.01UF
R212 15K
C218 0.01UF
R213 13K
C215 1500PF
C216 100PF
R221 0 DNI
R222 1.00K
VOUTA
VOUTB
R216 0 DNI
E210 100MHZ
L201 2.2UH DNI
C220 22UF
C221 22UF
R217 0
R215 TBD0603 DNI
C219 TBD0603 DNI
R218 0 DNI
E211 100MHZ
L202 2.2UH DNI
C223 22UF
C224 22UF
R219 0
R220 TBD0603 DNI
C222 TBD0603 DNI

ANALOG DEVCES

SCHEMATIC

9643 & 6649 ENGINEERING EVAL. PCB
AD9643
Engineering Board

DESIGN VIEW <DESIGN_VIEW>
DRAWING NO. 9643EE01
REV B
PTD ENGINEER <PTD_ENGINEER>
SIZE D
SCALE NONE
SHEET 2 OF 6

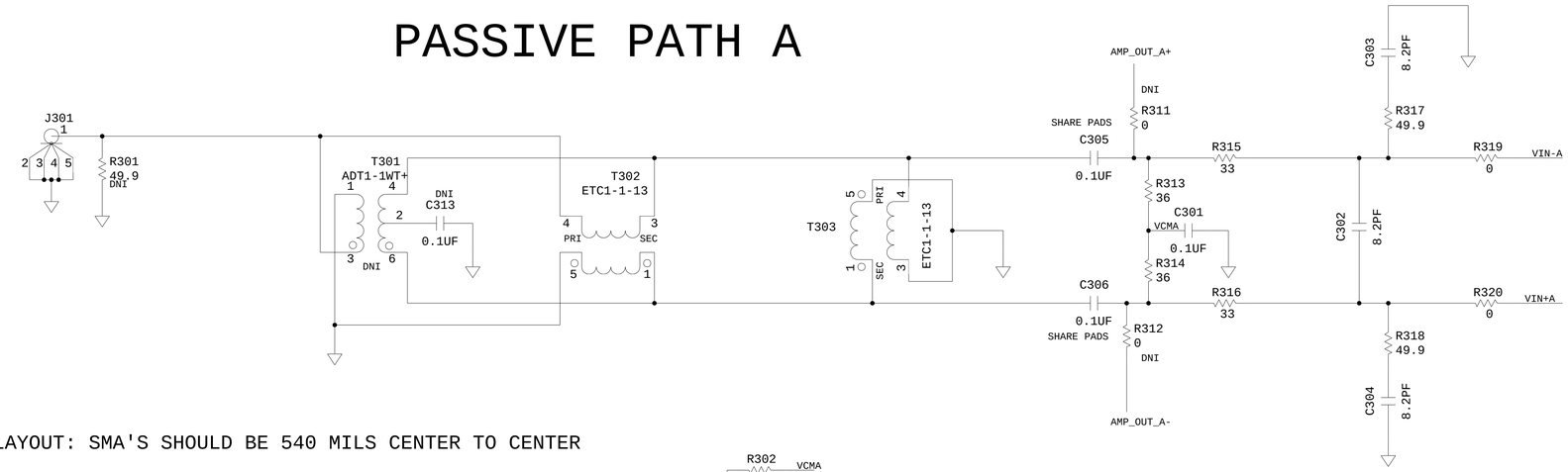
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANALOG INPUT

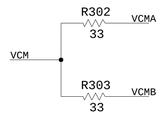
THIS SECTION WILL CHANGE BASED ON 9644 EXPERIMENTS

PASSIVE PATH A

AIN_A



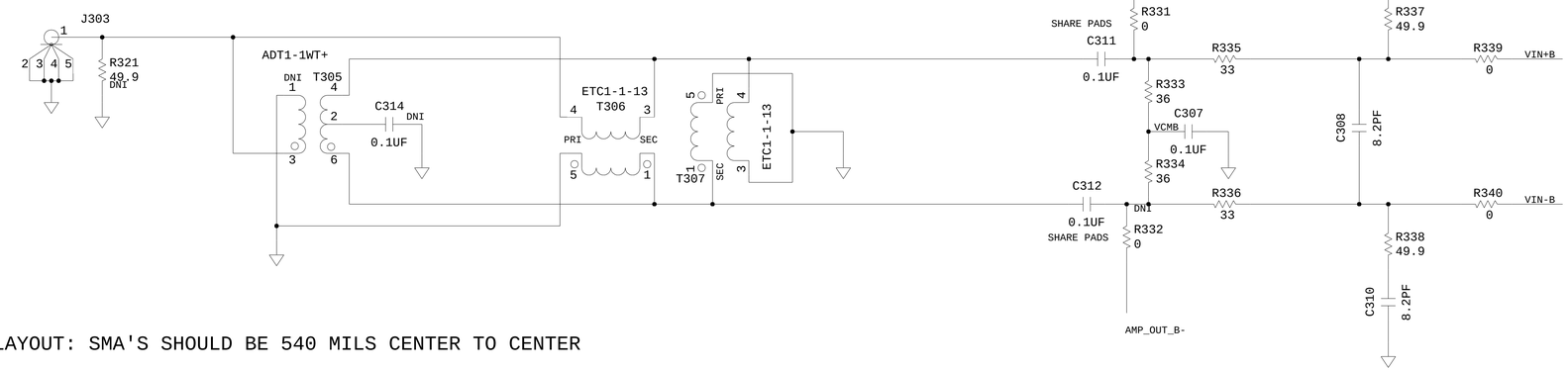
LAYOUT: SMA'S SHOULD BE 540 MILS CENTER TO CENTER



NOTE: CUTS REQ'D FOR 2ND TRANSF USE

PASSIVE PATH B

AIN_B



LAYOUT: SMA'S SHOULD BE 540 MILS CENTER TO CENTER

ANALOG DEVICES	SCHEMATIC		
	9643 & 6649 ENGINEERING EVAL. PCB AD9643 Engineering Board		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 9643EE01	REV B
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE NONE
		SHEET 3 OF 6	

ACTIVE PATH - CHANNEL A AND B

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

3P3V_ANALOG
C413 0.1UF
C414 0.1UF
C419 0.1UF

5V_SUPPORT
C410 10UF
C412 10UF
C407 0.1UF
C408 0.1UF
C409 0.1UF
C411 0.1UF

3P3V_ANALOG
R432 1K
P400
1
2
3
SAMTECTSW10608GS3PIN
R429 1K

3P3V_ANALOG
R427 1K
5V_SUPPORT
34
23
24
25
26
27
28
PWUPA
VPOS
VPOS_IDB
VPOS_IGB
VPOS_IGA
VPOS_IDA
VPOS

3P3V_ANALOG
DNI
R445 1K
R446 1K

U401
VOUTA_NEG 30
VOUTA_POS 29
NC4 32
NC3 31
NC1 19
NC2 20
VOUTB_NEG 21
VOUTB_POS 22
A0_UPDN_CLK_A 38
DATA 39
A2_FA_A 40
CSA_N_A3 1
A4 2
A5 3
UPDN_CLK_B_B0 13
DATA 12
GS0_FA_B_B2 11
GS1_CSB_N_B3 10
SCLK_B4 9
SDIO_B5 8
PWUPB 17
GND_ZAP 7
GND 18
GND 33
PAD PAD
ADL5202_PRELIM
DNI

36 VINA_NEG
35 VINA_POS
15 VINB_NEG
16 VINB_POS
37 LATCHA
14 LATCHB
6 PM
5 MODE0
4 MODE1

A0 A1 A2 A3 A4 A5 B0 B1 B2 B3 B4 B5

R401 0
R403 0 DNI
C402 0.1UF
T401
6
1
2
4
3
C401 0.1UF
TC3-1T+
DNI R405 130
J404 DNI
1
2 3 4 5
AMP_IN_B+
R437 49.9 DNI
R404 0 DNI
C403 0.1UF

R406 0 DNI
C405 0.1UF
DNI
J403
1
2 3 4 5
AMP_IN_A+
R438 49.9 DNI
TC3-1T+
T402
4
3
2
6
1
C404 0.1UF
DNI R408 130
R402 0
R407 0 DNI
C406 0.1UF

R430 1K
R431 1K
R433 1K
R434 1K
DNI

3P3V_ANALOG
R428 1K

5V_SUPPORT
L402 1UH
L401 1UH
L407 1UH
L408 1UH

THESE RLCS ARE PLACE HOLDERS... PLACE CORRECT VALUES & COMPONENTS...

R410 0 DNI
C415 1200PF DNI
L403 120NH DNI
L405 120NH DNI
AMP_OUT_B-
R412 150 DNI
C441 0.1UF DNI
R443 150 DNI
C417 2.7PF DNI
C418 22PF DNI
R411 0 DNI
C416 1200PF DNI
L404 120NH DNI
L406 120NH DNI
AMP_OUT_B+

THESE RLCS ARE PLACE HOLDERS... PLACE CORRECT VALUES & COMPONENTS...

R414 0 DNI
C421 1200PF DNI
L409 120NH DNI
L411 120NH DNI
AMP_OUT_A-
R426 150 DNI
C442 0.1UF DNI
R444 150 DNI
C423 2.7PF DNI
C424 22PF DNI
R415 0 DNI
C422 1200PF DNI
L410 120NH DNI
L412 120NH DNI
AMP_OUT_A+

R439 0 ADL5202_CSA
R440 0 ADL5202_CSB
R441 0 FPGA_SCLK
R442 0 FPGA_SDIO

3P3V_ANALOG
R416 10K
R417 10K
R418 10K
R419 10K
R420 10K
R413 10K
A0 A1 A2 A3 A4 A5

3P3V_ANALOG
R421 10K
R422 10K
R423 10K
R424 10K
R425 10K
R409 10K
B0 B1 B2 B3 B4 B5

ANALOG DEVICES

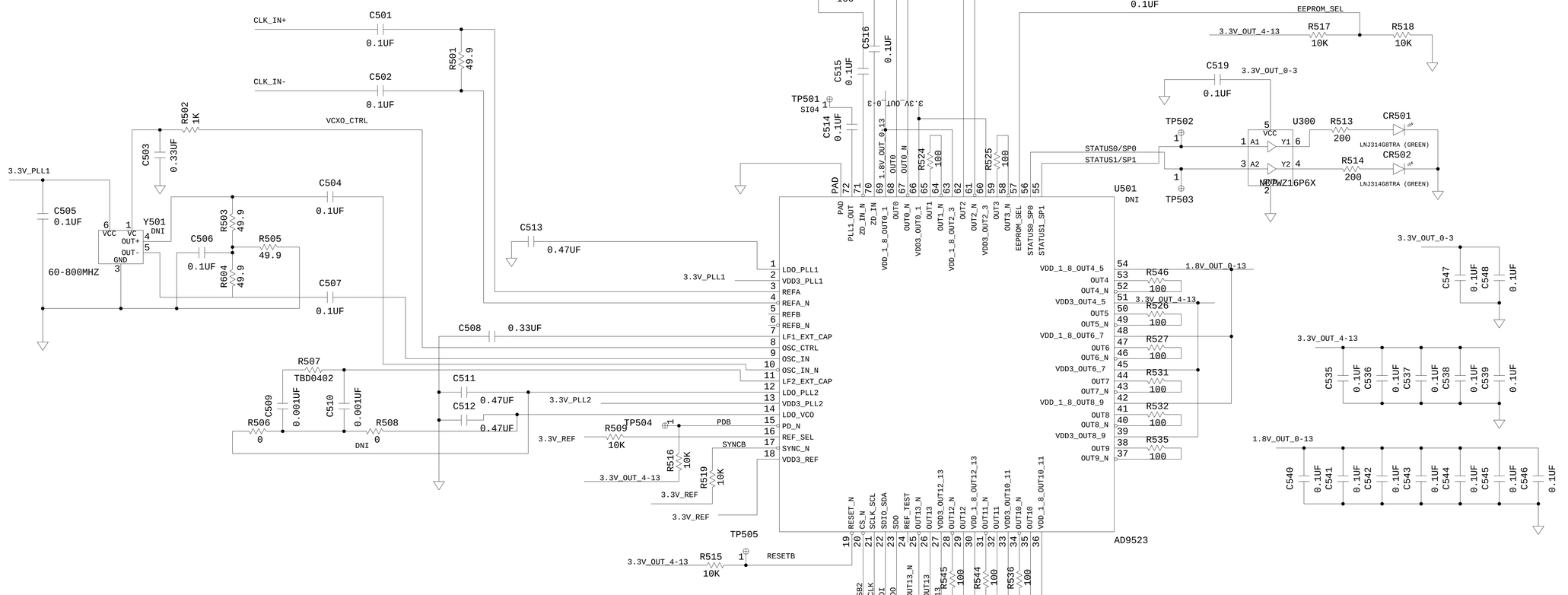
SCHEMATIC

9643 & 6649 ENGINEERING EVAL. PCB
AD9643
Engineering Board

DESIGN VIEW <DESIGN_VIEW>
DRAWING NO. 9643EE01
REV B
PTD ENGINEER <PTD_ENGINEER>
SIZE D
SCALE NONE
SHEET 4 OF 6

ACTIVE CLOCK PATH

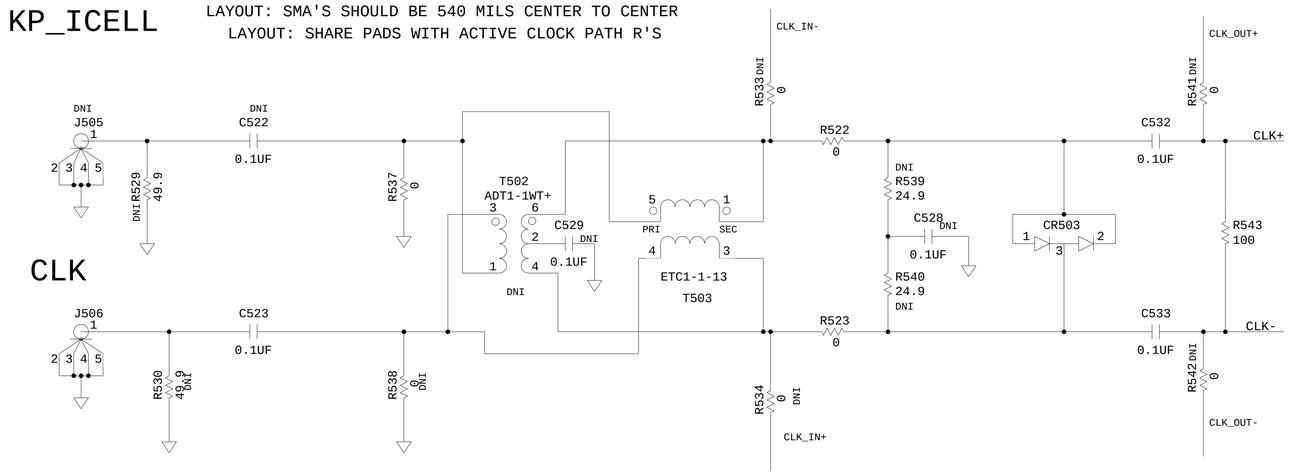
PECL/CML/LVDS CLK CIRCUITRY

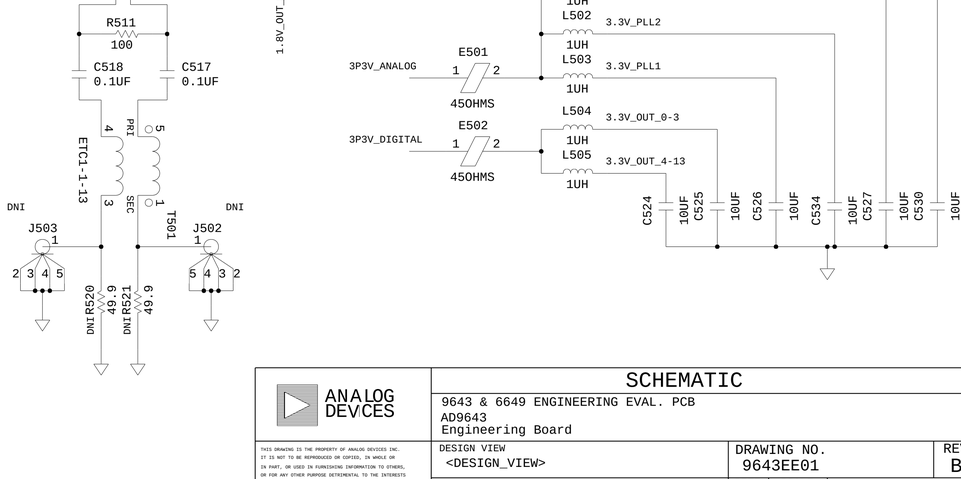


PASSIVE CLOCK

KP_ICELL

LAYOUT: SMA'S SHOULD BE 540 MILS CENTER TO CENTER
LAYOUT: SHARE PADS WITH ACTIVE CLOCK PATH R'S





REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

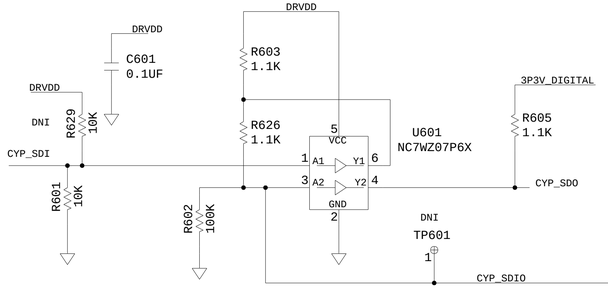
ANALOG DEVICES

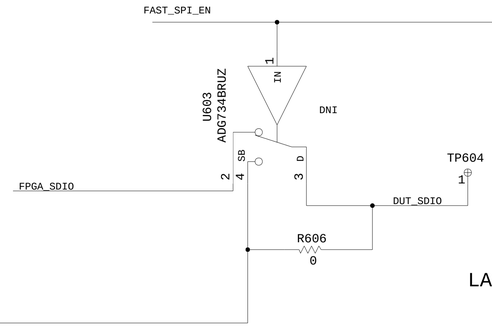
SCHEMATIC

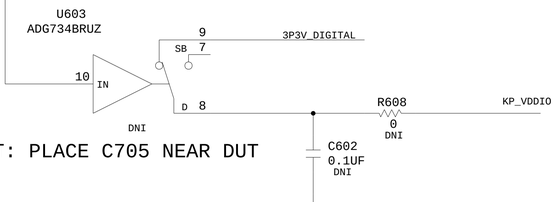
9643 & 6649 ENGINEERING EVAL. PCB
AD9643
Engineering Board

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	9643EE01	B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE NONE	SHEET 5 OF 6

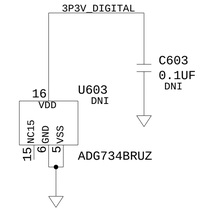
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



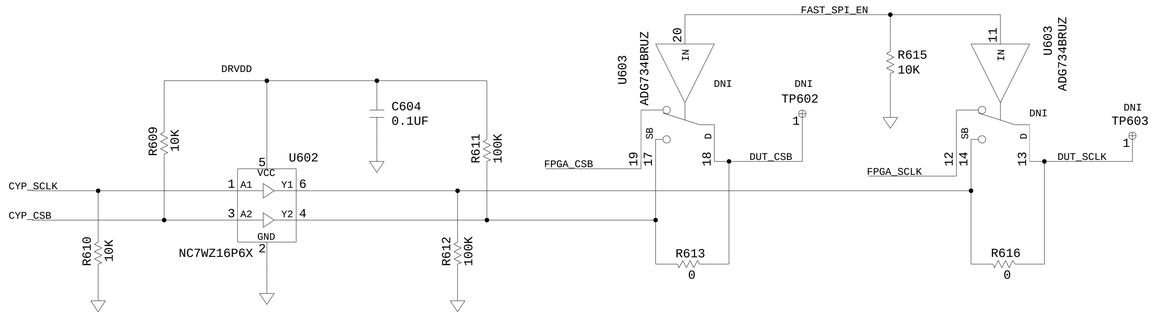




LAYOUT: PLACE C705 NEAR DUT

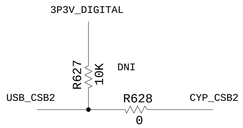


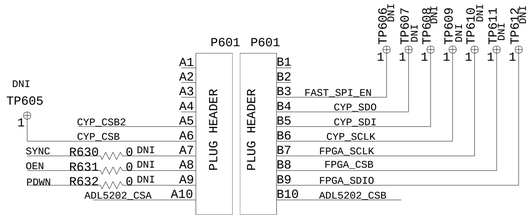
NOTE: THIS SYMBOL IS DRAWN GIVEN INPUT 1 LOGIC



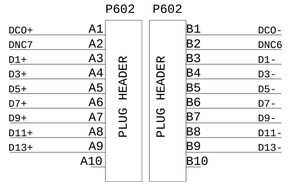
SPI & FPGA CONN.

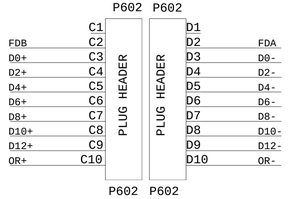
LAYOUT: ROUTE ALL TRACES TO THE TYCO CONN ON TOP OF BOARD

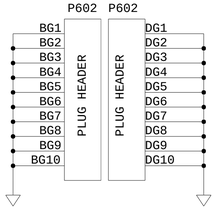




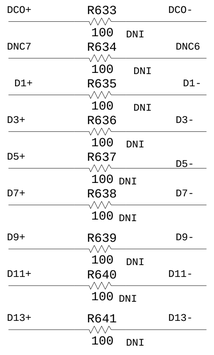
BRINGING SYNC, OEN AND PDWN TO FPGA
PLACE 0R RESISTORS NEAR THE DUT

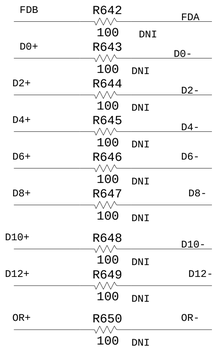






USING FIFO5





ANALOG DEVICES

SCHEMATIC

9643 & 6649 ENGINEERING EVAL. PCB
AD9643
Engineering Board

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	9643EE01	B
PTD ENGINEER	SIZE / SCALE	SHEET 6 OF 6
<PTD_ENGINEER>	D / NONE	